Lecture 11

- Last time:
  - pn junctions: thermal equilibrium
  - pn junctions: charge-voltage characteristic
- Today :
  - pn junction *small-signal* capacitance (attention: this concept is difficult)

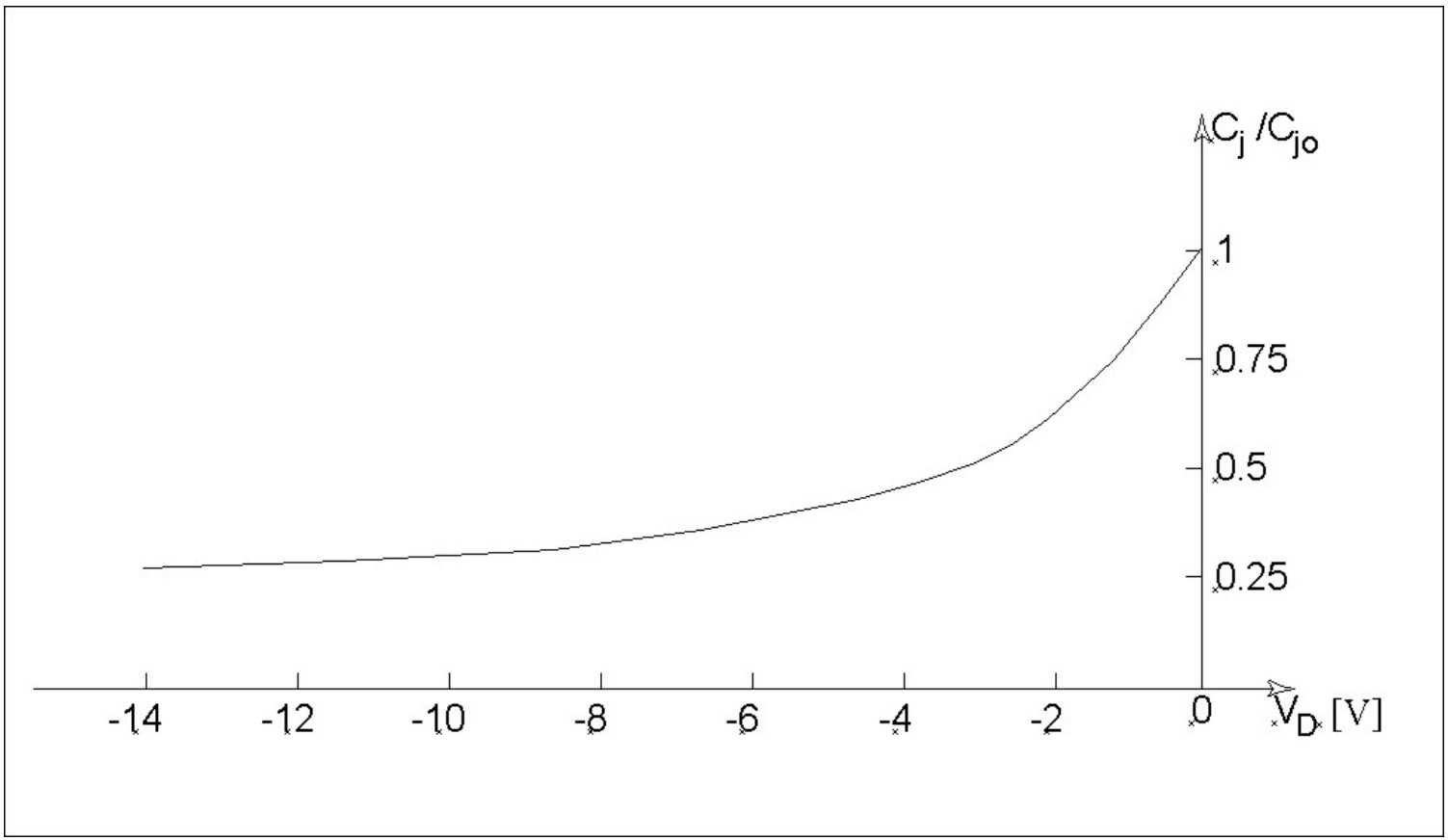
Junction Capacitance C_j

- Slope of charge-voltage plot is the ratio of the small-signal charge to the small-signal voltage

$$slope = \left.\frac{dq_J}{dv_D}\right|_{V_D} = \frac{q_j}{v_d}$$

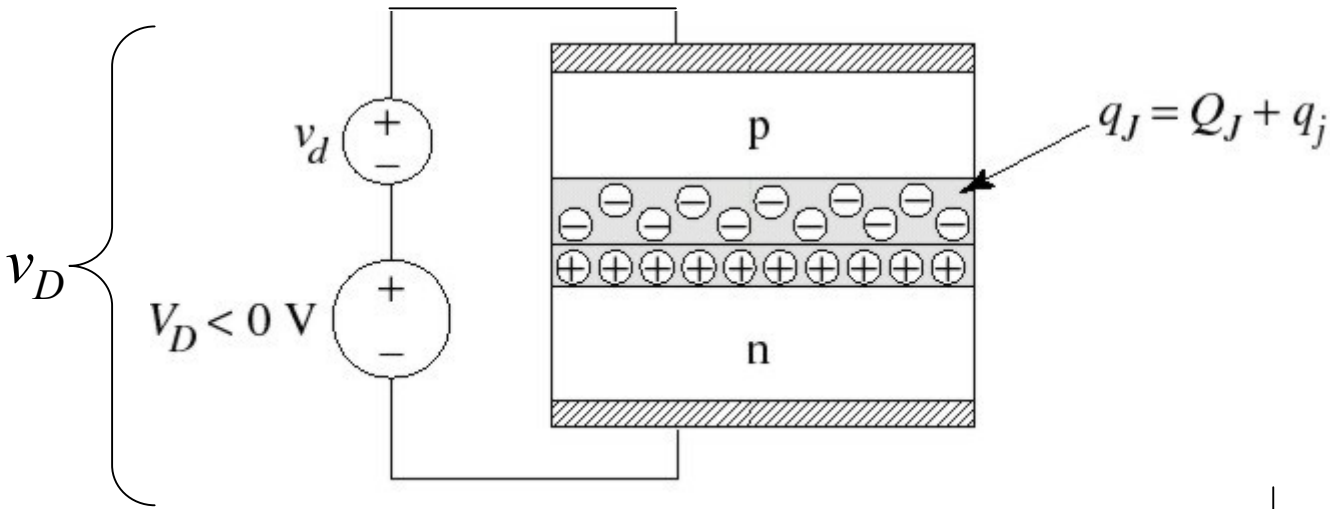
- Define the slope (units: C/V = F) to be the *junction capacitance* C_j

Junction Capacitance vs. DC Bias

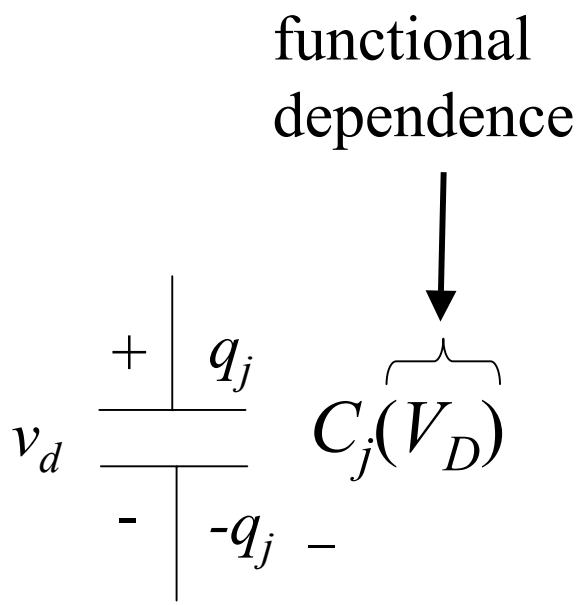


Small-Signal Circuit Model

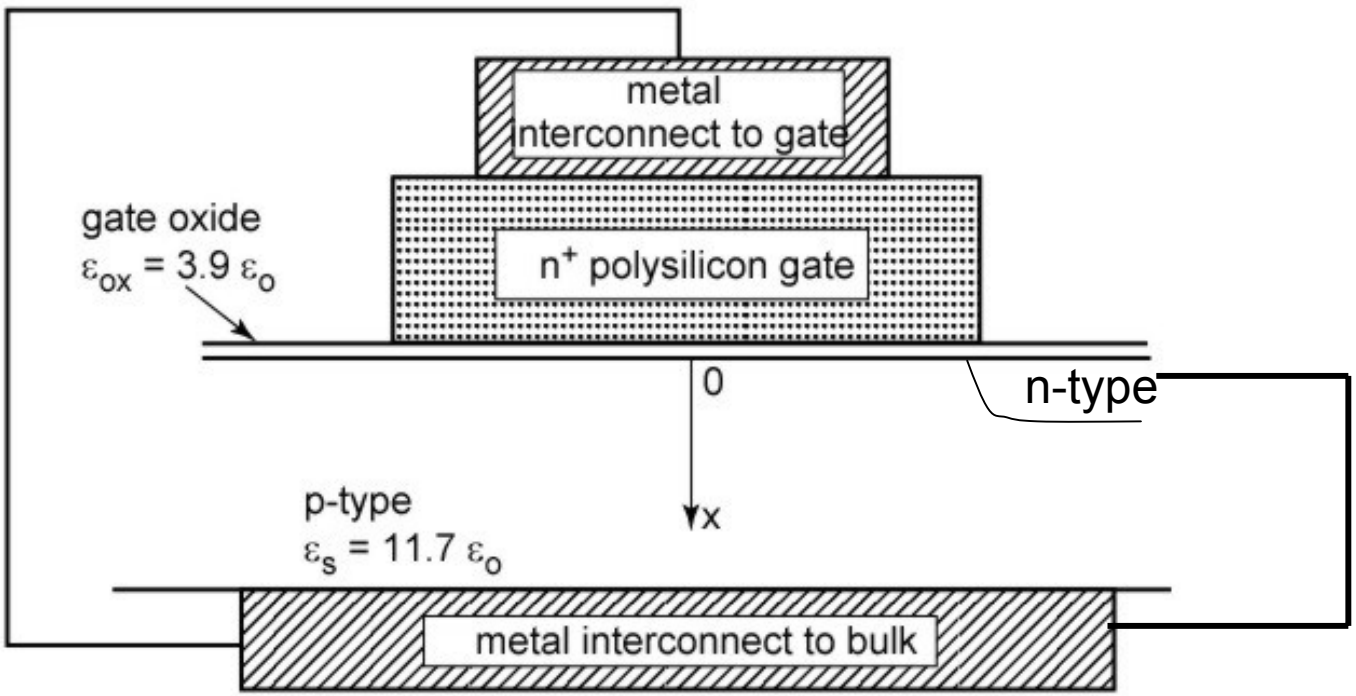
- total voltage and total charge:



- small-signal variables *only* →

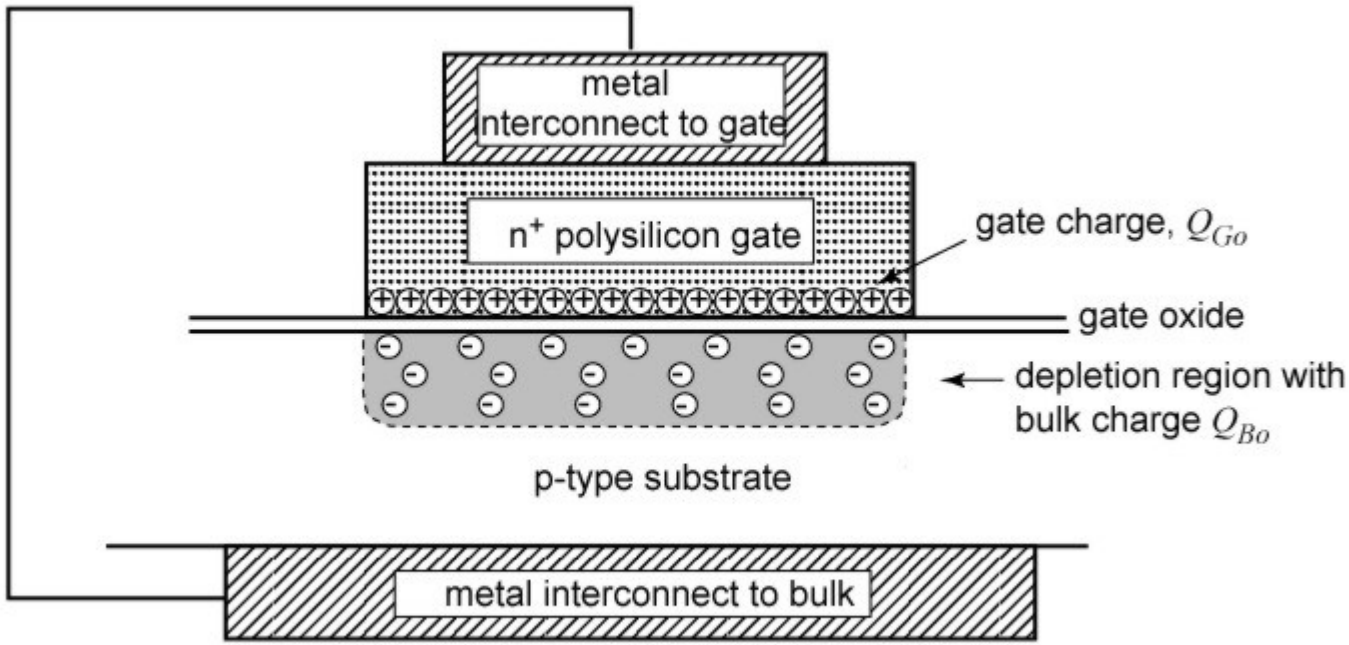


MOS Structure



Thermal Equilibrium

Charged bi-layer forms: + charges on gate, - in substrate
Built-in voltage between gate and substrate



Applying a DC Voltage V_{GB}

Goal: find out how the gate charge Q_G varies as a function of the applied voltage V_{GB}

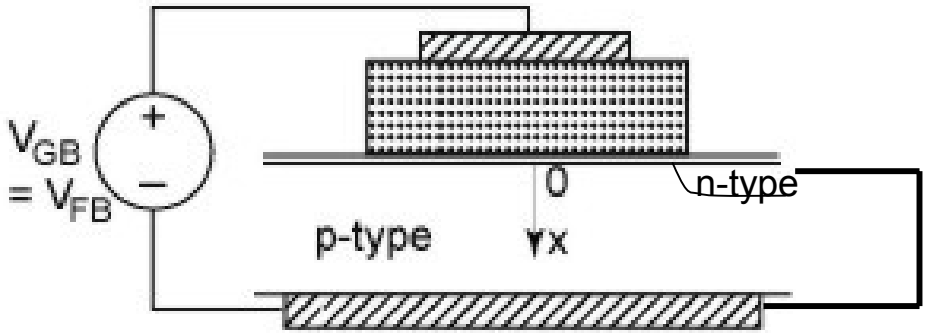
Procedure: start at thermal equilibrium

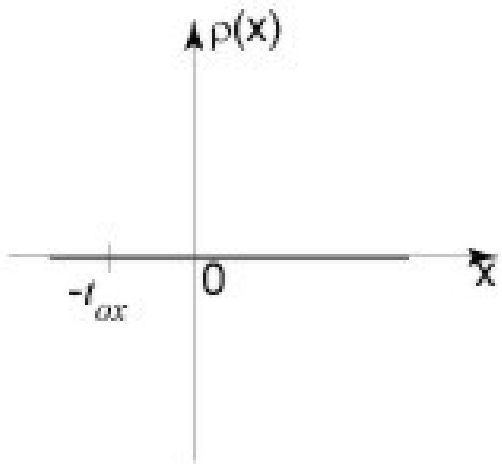
(i) go negative until built-in charge is cancelled
(ii) keep going until charge on gate is negative
(iii) go positive from thermal equilibrium
(iv) keep increasing V_{GB} until …

☞IMPORTANT: IDENTIFY CHARGE IN SUBSTRATE

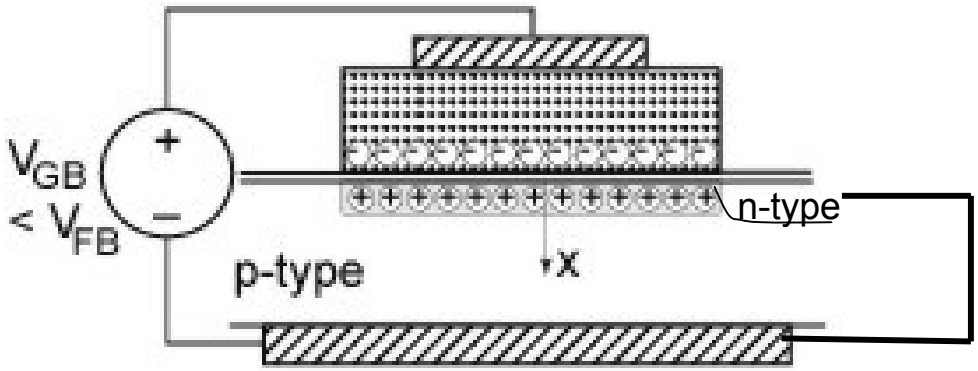
Cancel the Built-in Voltage

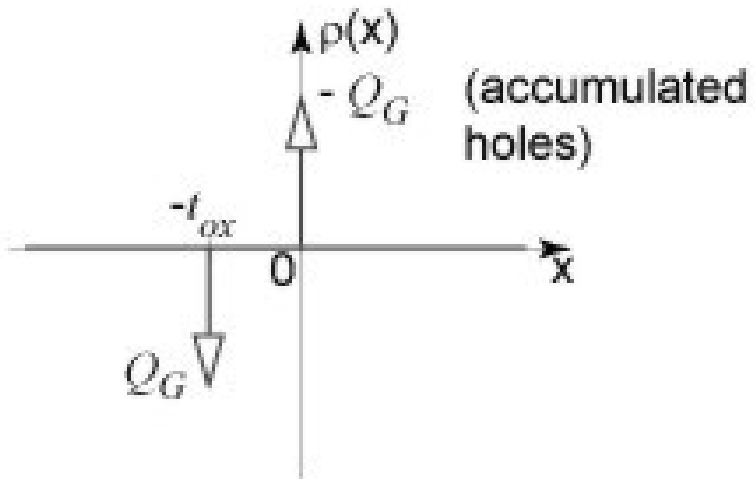
Apply V_{FB} to "zero" the built-in voltage





Accumulation





Depletion: $V_{GB} > V_{FB}$