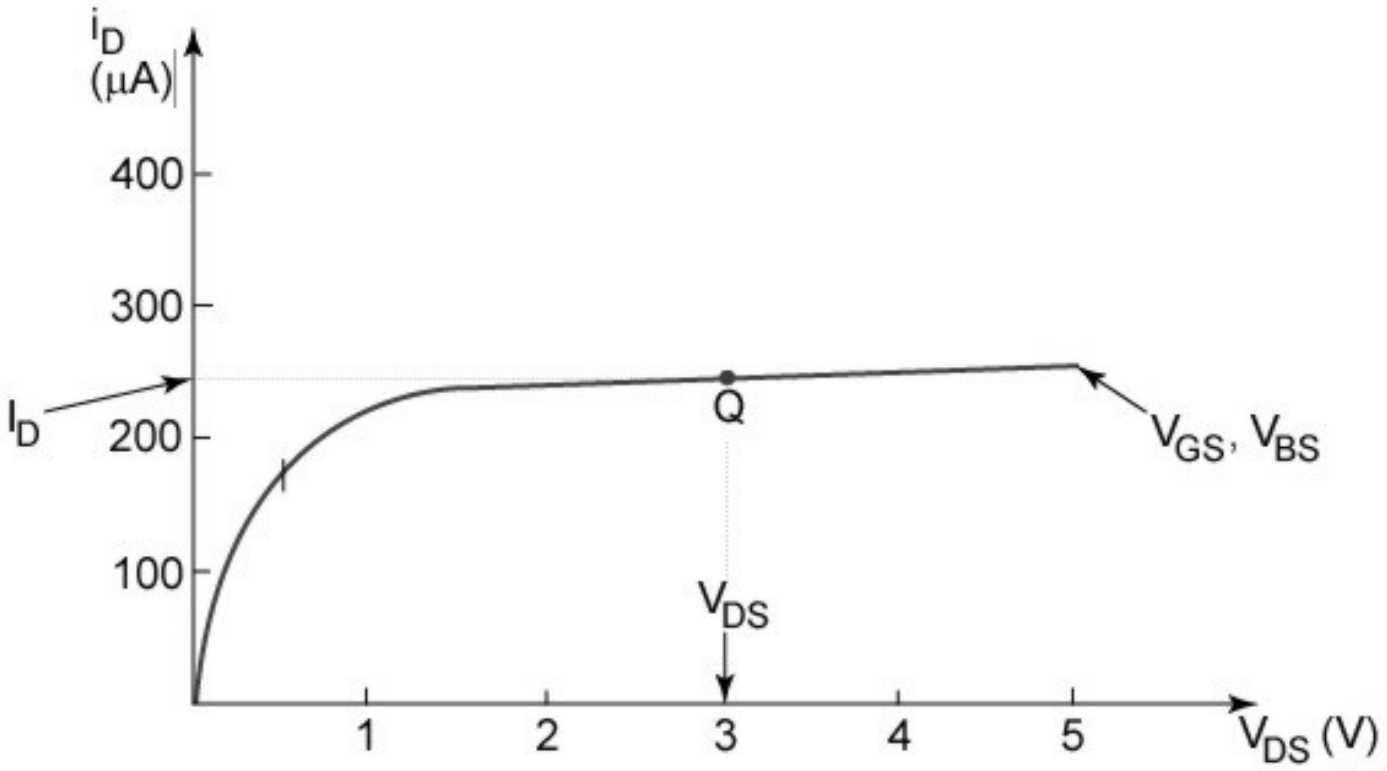
Lecture 16

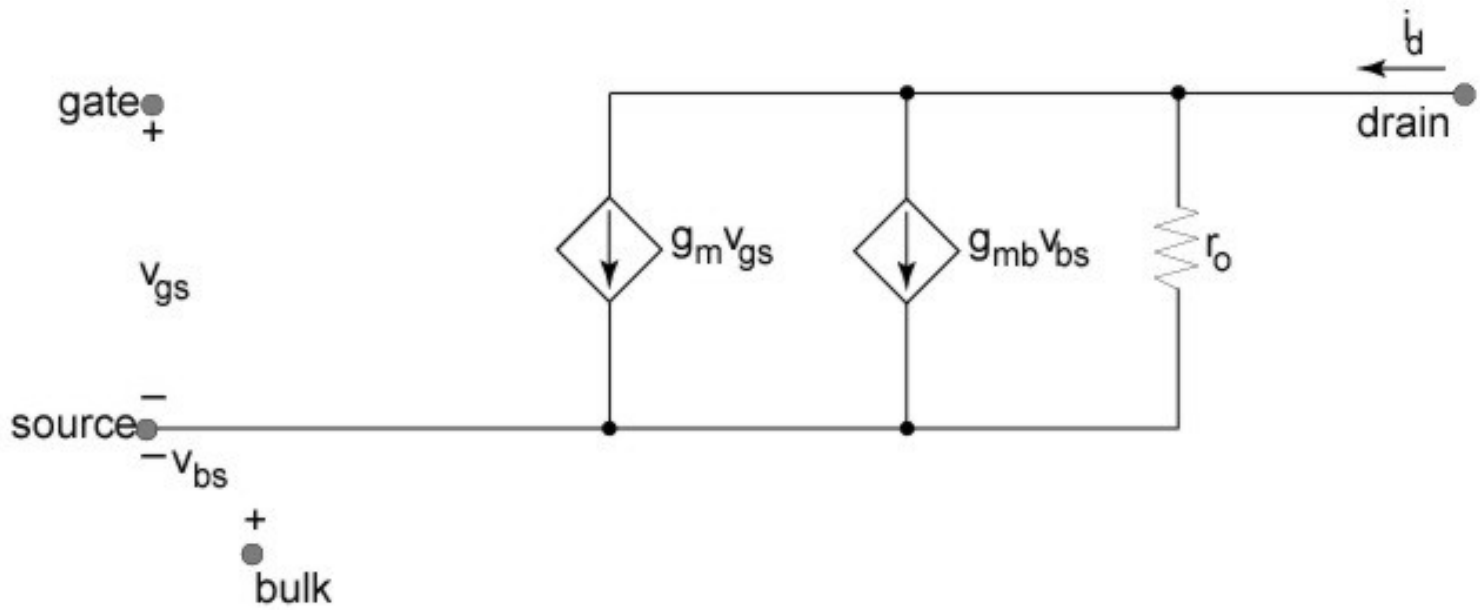
- Last time:
  - MOSFET small-signal model (g_m, r_o)
- Today :
  - Complete small-signal model: add capacitors
  - P-channel MOSFET
  - MOSFET Spice Model

Backgate Transconductance



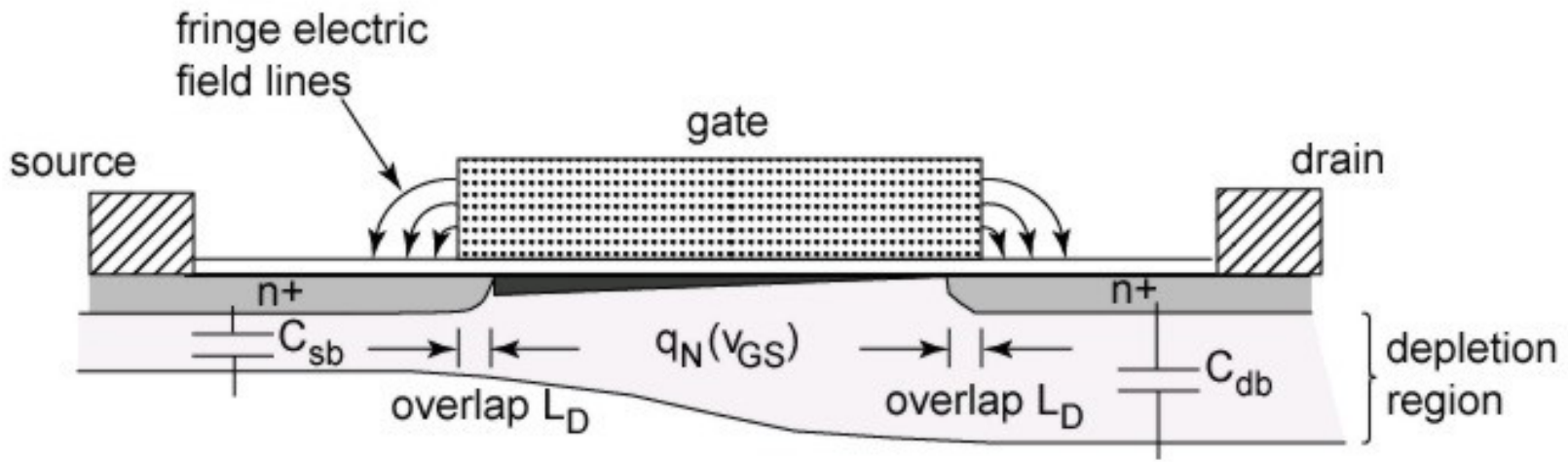
Result: $$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \left.\frac{\partial i_D}{\partial V_{Tn}}\right|_Q \left.\frac{\partial V_{Tn}}{\partial v_{BS}}\right|_Q =$$

Four-Terminal Small-Signal Model



MOSFET Capacitances in Saturation

Gate-source capacitance: channel charge is not controlled by drain in saturation.



Gate-Source Capacitance C_{gs}

Wedge-shaped charge in saturation → effective area is $(2/3)WL$ (see H&S 4.5.4 for details)

$$C_{gs} = (2/3)WLC_{ox} + C_{ov}$$

Overlap capacitance along source edge of gate →

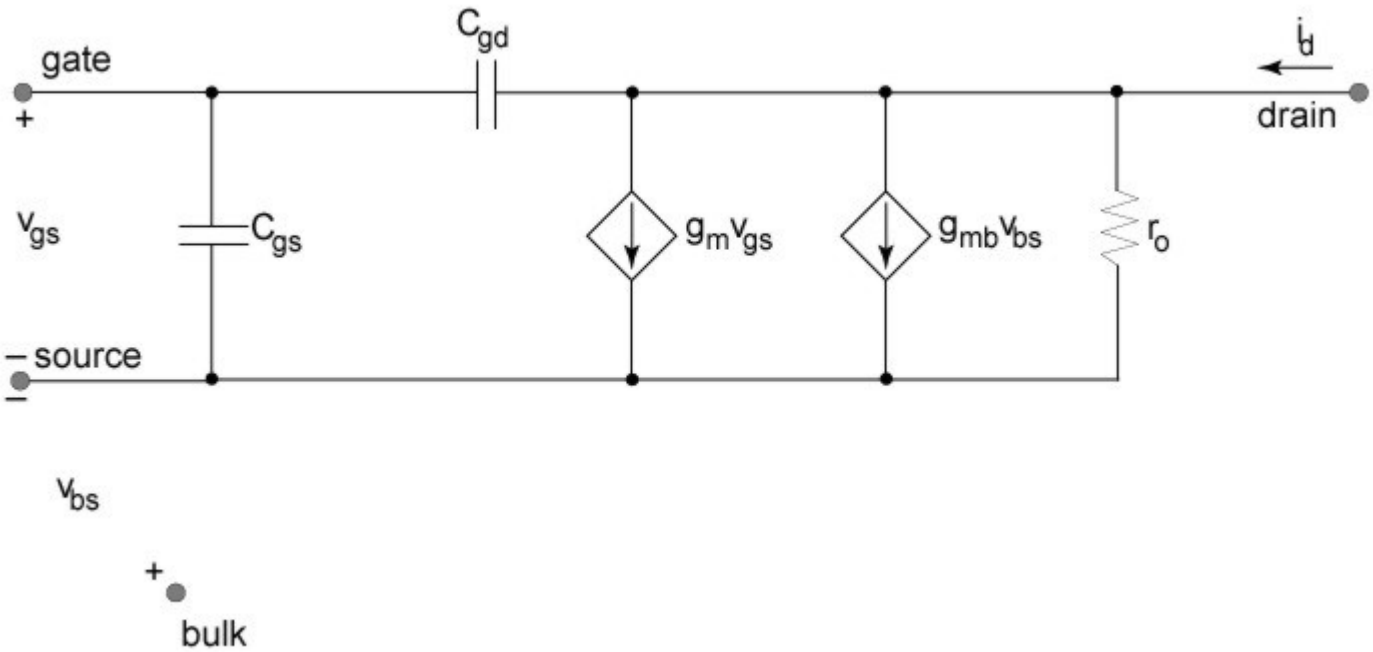
$$C_{ov} = L_D W C_{ox}$$

(Underestimate due to fringing fields)

Gate-Drain Capacitance C_{gd}

Not due to change in inversion charge in channel

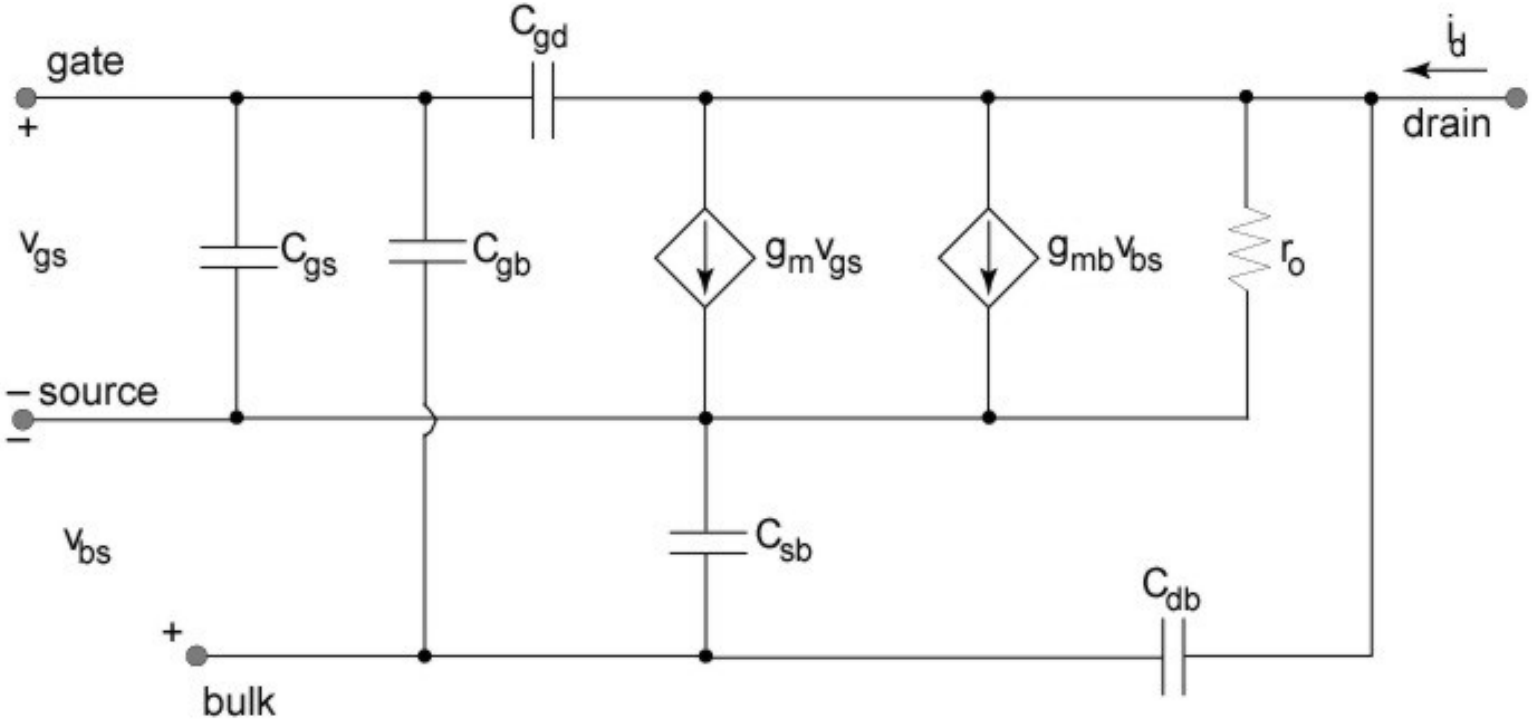
Overlap capacitance C_{ov} between drain and source is C_{gd}



Junction Capacitances

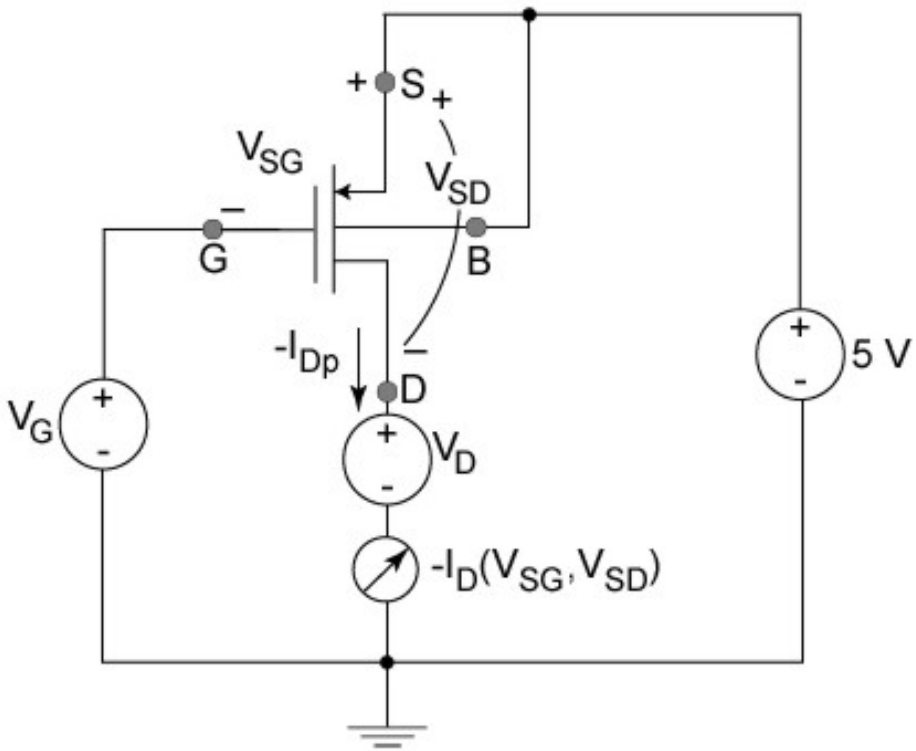
Drain and source diffusions have (different) junction capacitances since V_{SB} and $V_{DB} = V_{SB} + V_{DS}$ aren't the same

Complete model (without interconnects)

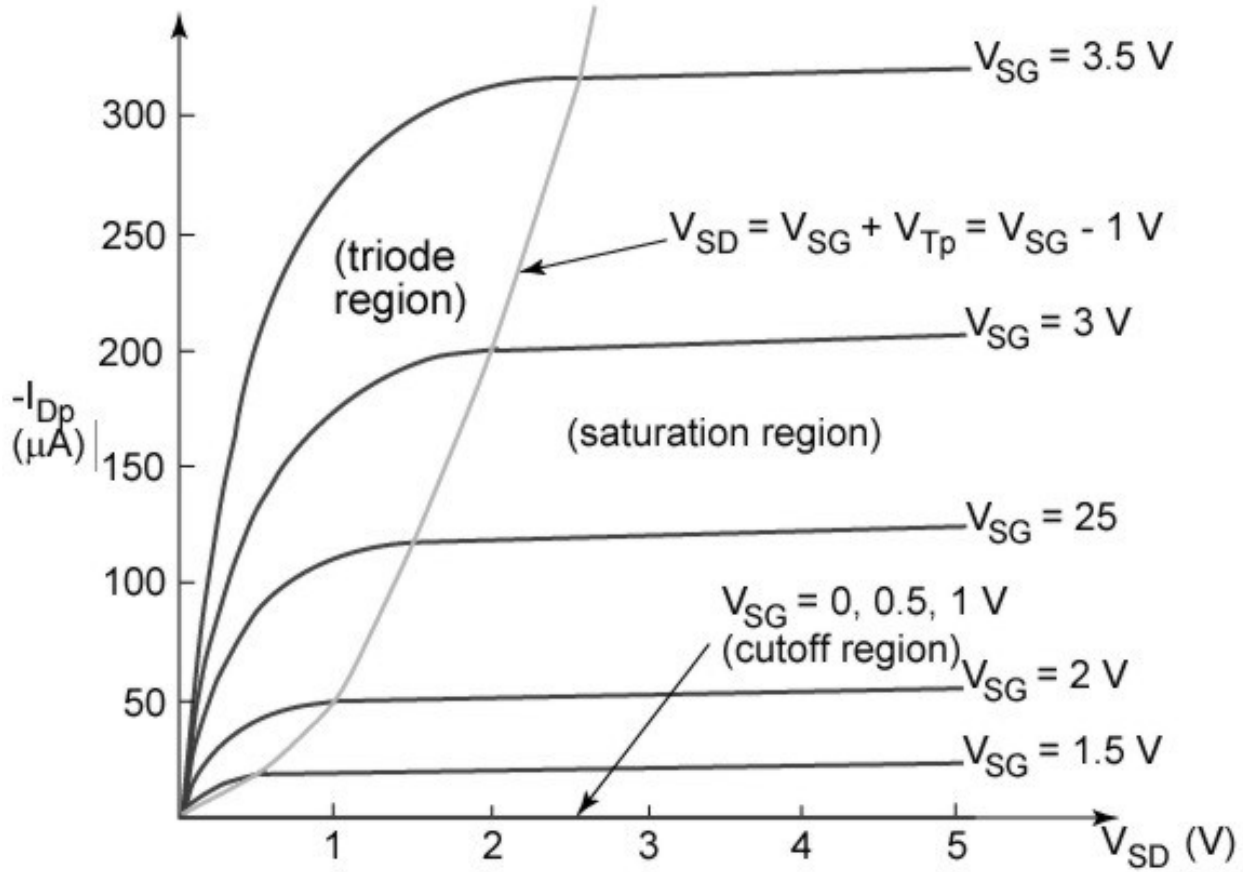


P-Channel MOSFET

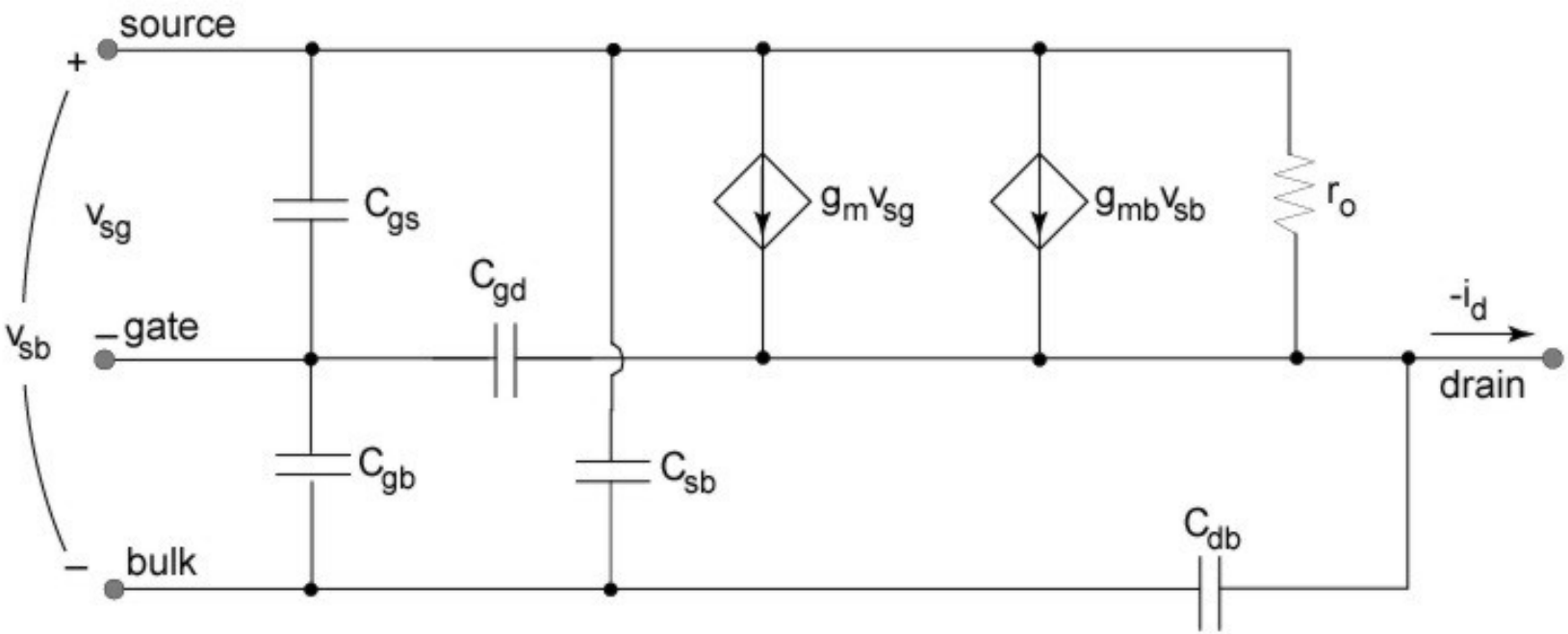
Measurement of $-I_{Dp}$ versus V_{SD}, with V_{SG} as a parameter:



Square-Law PMOS Characteristics



Small-Signal PMOS Model



MOSFET SPICE Model

Many "levels" … we will use the square-law "Level 1" model

See H&S 4.6 + Spice refs. on reserve for details.

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.MODEL MODN NMOS LEVEL = 1 VTO = 1 KP = 50U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 1E-4 CJSW = 5E-10
+ MJ = 0.5 PB = 0.95
.MODEL MODP PMOS LEVEL = 1 VTO = -1 KP = 25U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 3E-4 CJSW = 3.5E-10
+ MJ = 0.5 PB = 0.95
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