## Lecture 22

- Last time:
- Small-signal model of the npn bipolar transistor
- Today :
- Introduction to amplifiers: a common-source MOS single-stage amplifier


## An MOS Amplifier

Dictionary definition: amplify $=$


## Selecting the Output Bias Point

$V_{B I A S}$ is selected so that $V_{O U T}$ is centered between $+V_{S U P}$ and $-V_{S U P}$ (why?)

$$
V_{O U T}=0 \mathrm{~V} \ldots \text { NOT } v_{\text {OUT }}=0 \mathrm{~V}!
$$

Constraint on the DC drain current:

$$
I_{\mathrm{RD}}=\left(V_{\mathrm{SUP}}-V_{\mathrm{OUT}}\right) / R_{\mathrm{D}}=V_{\mathrm{SUP}} / R_{\mathrm{D}}
$$

$I_{\mathrm{RD}}=I_{\mathrm{D}}=I_{D, S A T} \ldots$ verify that MOSFET is saturated after finding $V_{\text {BIAS }}$

## Finding the Input Bias Voltage

Hand calculation: neglect "fudge factor" in $I_{D, S A T}$

$$
I_{D, S A T}=(W / 2 L) \mu_{n} C_{o x}\left(V_{G S}-V_{T n}\right)^{2}
$$

Typical numbers: $\quad W=40 \mu \mathrm{~m}, L=2 \mu \mathrm{~m}, R_{D}=25 \mathrm{k} \Omega$

$$
\begin{aligned}
& \mu_{\mathrm{n}} C_{o x}=100 \mu \mathrm{~A} / \mathrm{V}^{2}, V_{T n}=1 \mathrm{~V}, \\
& V_{S U P}=2.5 \mathrm{~V}
\end{aligned}
$$

$$
I_{R D}=\frac{V_{S U P}}{R_{D}}=I_{D, S A T}=10 \cdot 100 \cdot\left(V_{G S}-1\right)^{2}
$$

## Applying the Small-Signal Voltage

Approach 1. Just use $v_{I N}$ in the equation for the total drain current $i_{D}$ and find $v_{\text {OUT }}$
$v_{I N}=V_{B I A S}+v_{s} \quad v_{G S}=v_{I N}-\left(-V_{S U P}\right)=\left[V_{B I A S}+v_{S}+V_{S U P}\right]$
$v_{S}(t)=\hat{v}_{S} \cos (\omega t)$
Result:

$$
v_{O U T}=V_{S U P}-R_{D} i_{D} \cong V_{S U P}-R_{D}\left(\mu_{n} C_{o x}\right)\left(\frac{W}{2 L}\right)\left(V_{G S}+v_{S}-V_{T n}\right)^{2}
$$

## Solving for the Output Voltage $v_{\text {OUT }}$

$$
\begin{gathered}
v_{O U T}=V_{S U P}-R_{I_{D}} \underbrace{V_{O U T}}_{V_{S U P}\left(\mu_{n} C_{o x}\right)\left(\frac{W}{2 L}\right)\left(V_{G S}-V_{T n}\right)^{2}}=V_{S U P}-R_{D} I_{D}\left(1+\frac{v_{S}}{\left(V_{G S}-V_{T n}\right)}\right)^{2} \\
\left.v^{\left(V_{G S}-V_{T n}\right)}\right)^{2}
\end{gathered}
$$

## Small-Signal Case

Linearize the output voltage for the s.s. case

Expand $(1+x)^{2}=1+2 x+x^{2} \ldots$ last term can be dropped when $x \ll 1$

$$
\left(1+\frac{v_{s}}{V_{G S}-V_{T n}}\right)^{2}=1+\frac{2 v_{s}}{V_{G S}-V_{T n}}+\left(\frac{v_{s}}{V_{G S}-V_{T n}}\right)^{2}
$$

## Linearized Output Voltage

For this case, the total output voltage is
$v_{O U T} \cong V_{S U P}-R_{D} I_{D}\left(1+\frac{2 v_{s}}{\left(V_{G S}-V_{T n}\right)}\right)=V / U P-V / U P-\frac{2 R_{D} I_{D} v_{s}}{\left(V_{G S}-V_{T n}\right)}$

The average output voltage $V_{O U T}=0 \mathrm{~V}$ so the total output voltage is the small-signal voltage in this special case:
$v_{\text {OUT }}=v_{\text {out }}=-\left[\frac{}{\left(V_{G S}-V_{T n}\right)}\right] v_{s}=-\left[\overline{\left(V_{G S}-V_{T n}\right)}\right] v_{s}=A_{v} v_{s}$

## Plot of Output Waveform

Numbers: $2 I_{D} R_{D} /\left(V_{G S}-V_{T_{n}}\right)=(2 \times 2.5) / 0.31=16.1$


## Is there a Better Way?

What's missing: no inclusion of fudge factor term or of charge storage effects

Approach 2. Do problem in two steps.

1. DC voltages and currents (ignore small signals sources): set bias point of the MOSFET ... we had to do this to pick $V_{B I A S}$ already
2. Substitute the small-signal model of the MOSFET and the small-signal models of the other circuit elements ...
