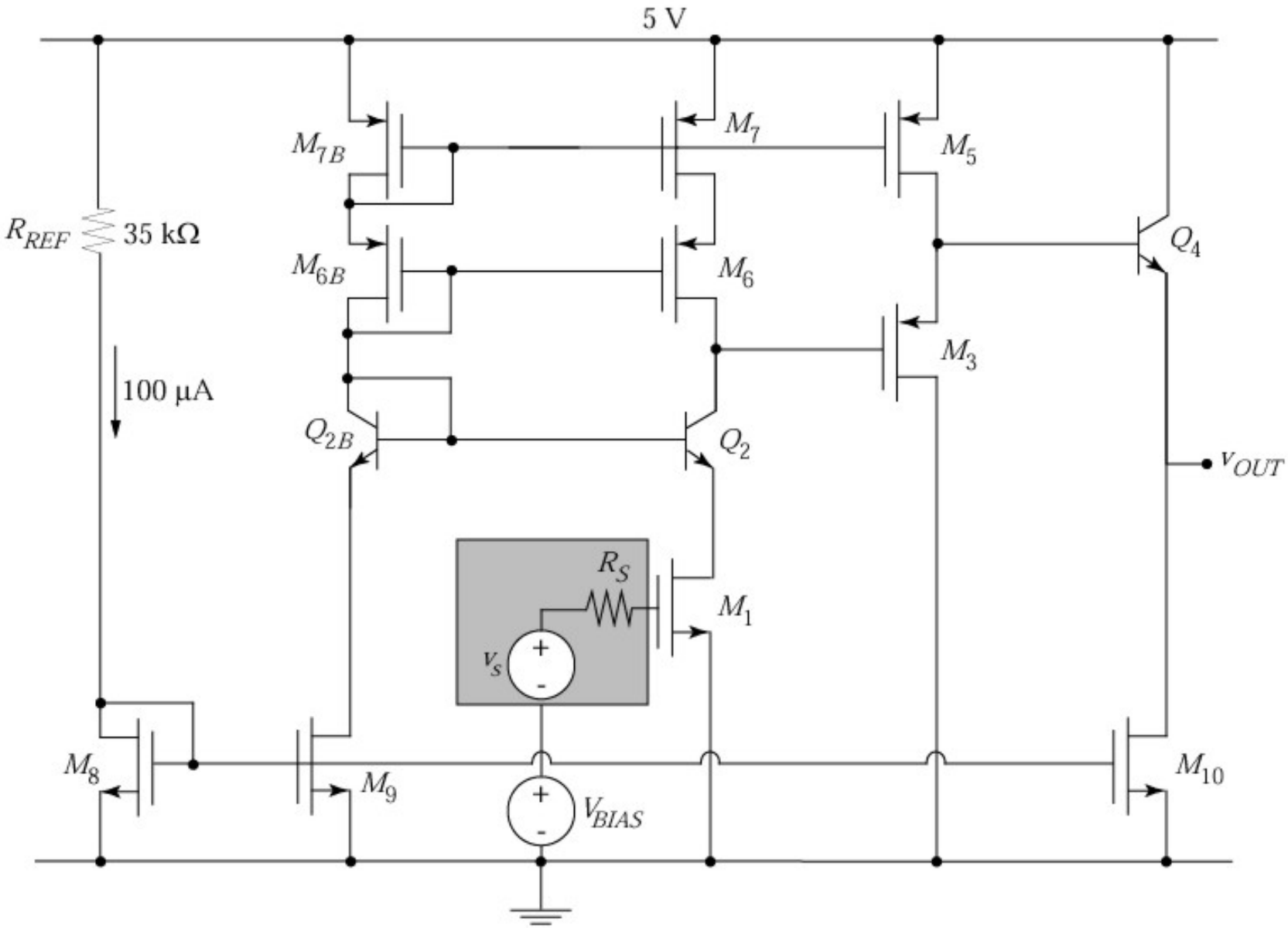
Lecture 38

- Last time:
  - CMOS cascode transconductance amplifier design example
- Today :
  - BiCMOS voltage amplifier: example of "dissection" technique for a complicated circuit

Multi-Stage Voltage Amplifier



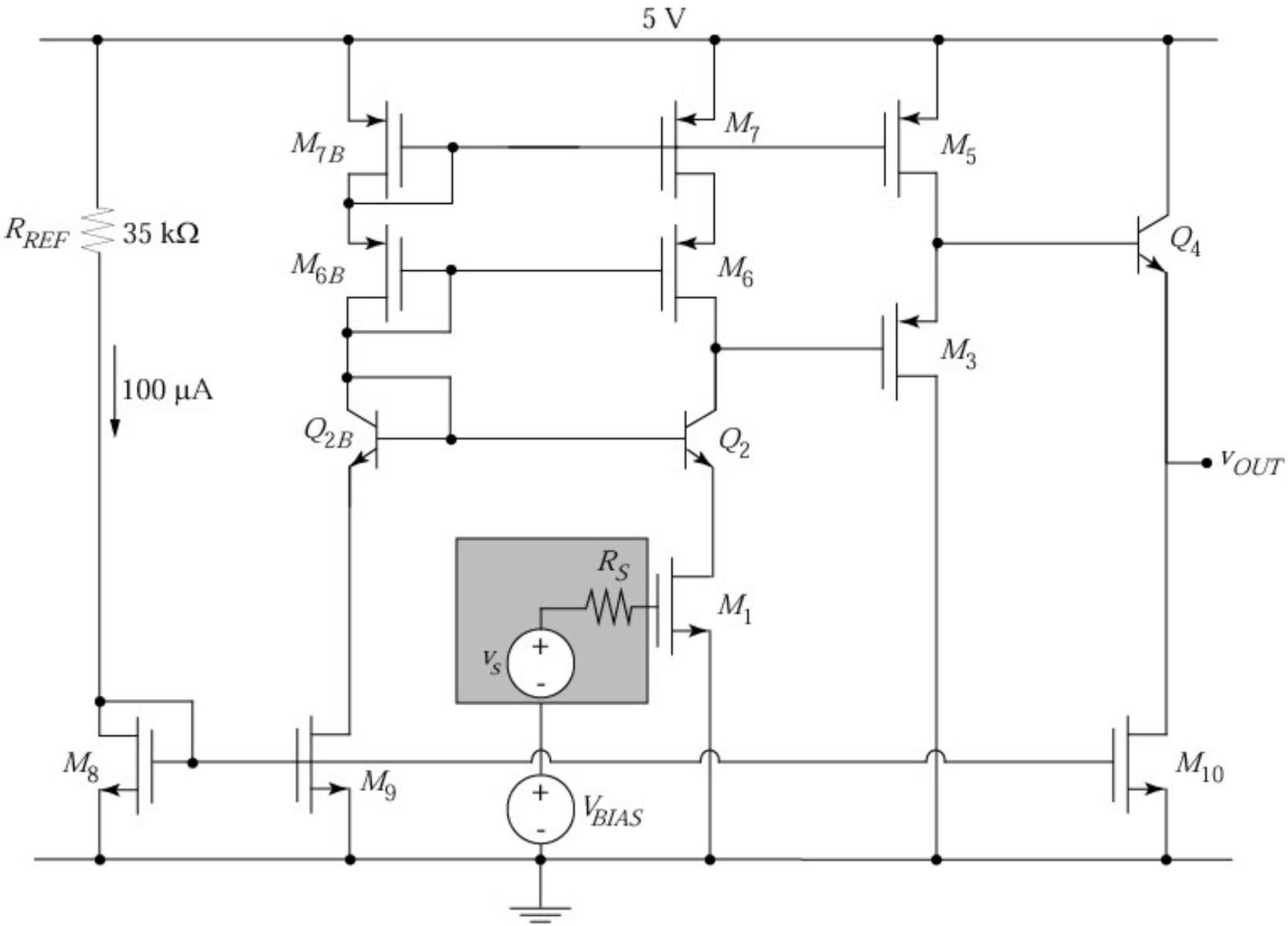
Cutting Through the Complexity

Two Approaches:

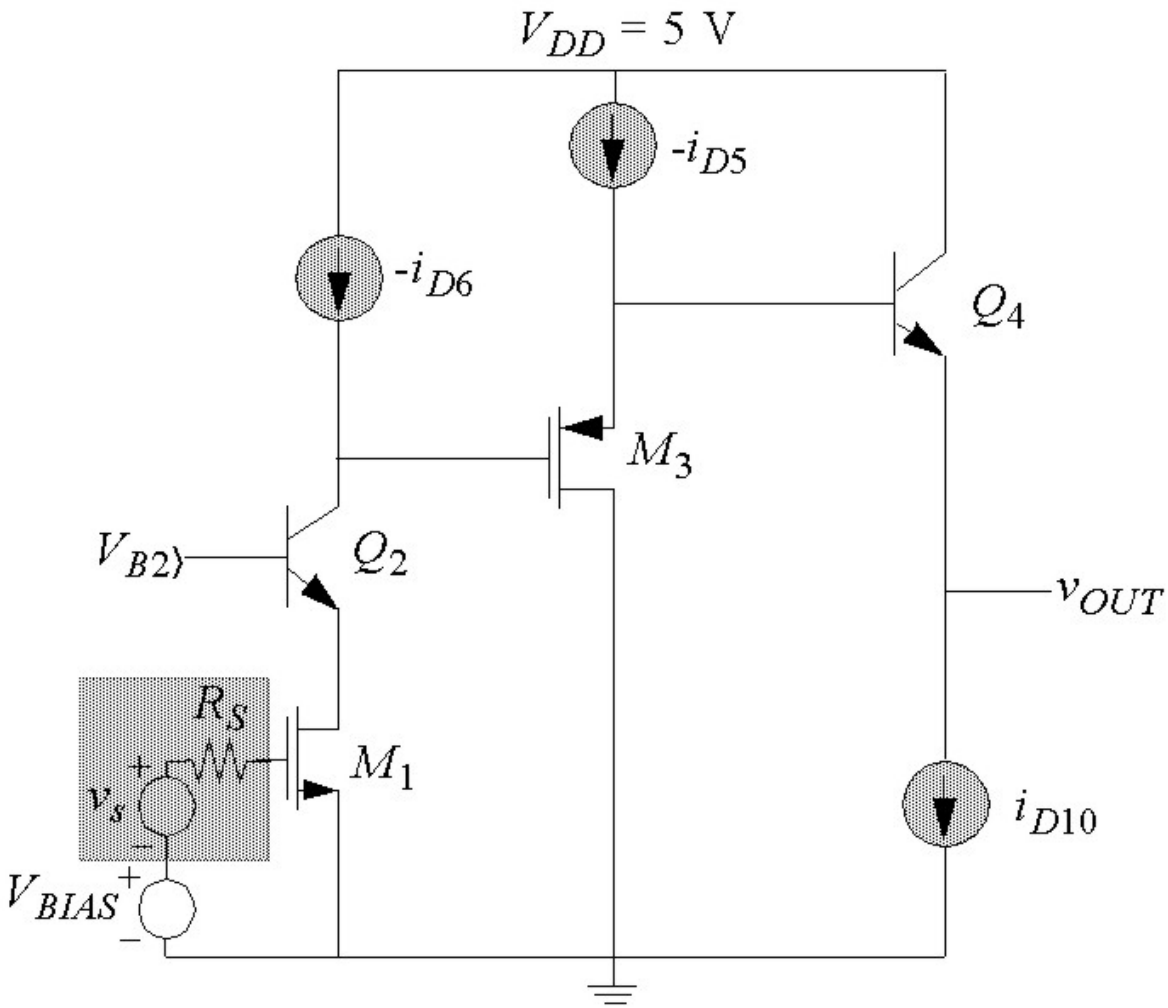
1. Eliminate "background" transistors to reduce clutter

2. Identify the "signal path" between the input and output

First Approach: Find *I* & *V* Sources

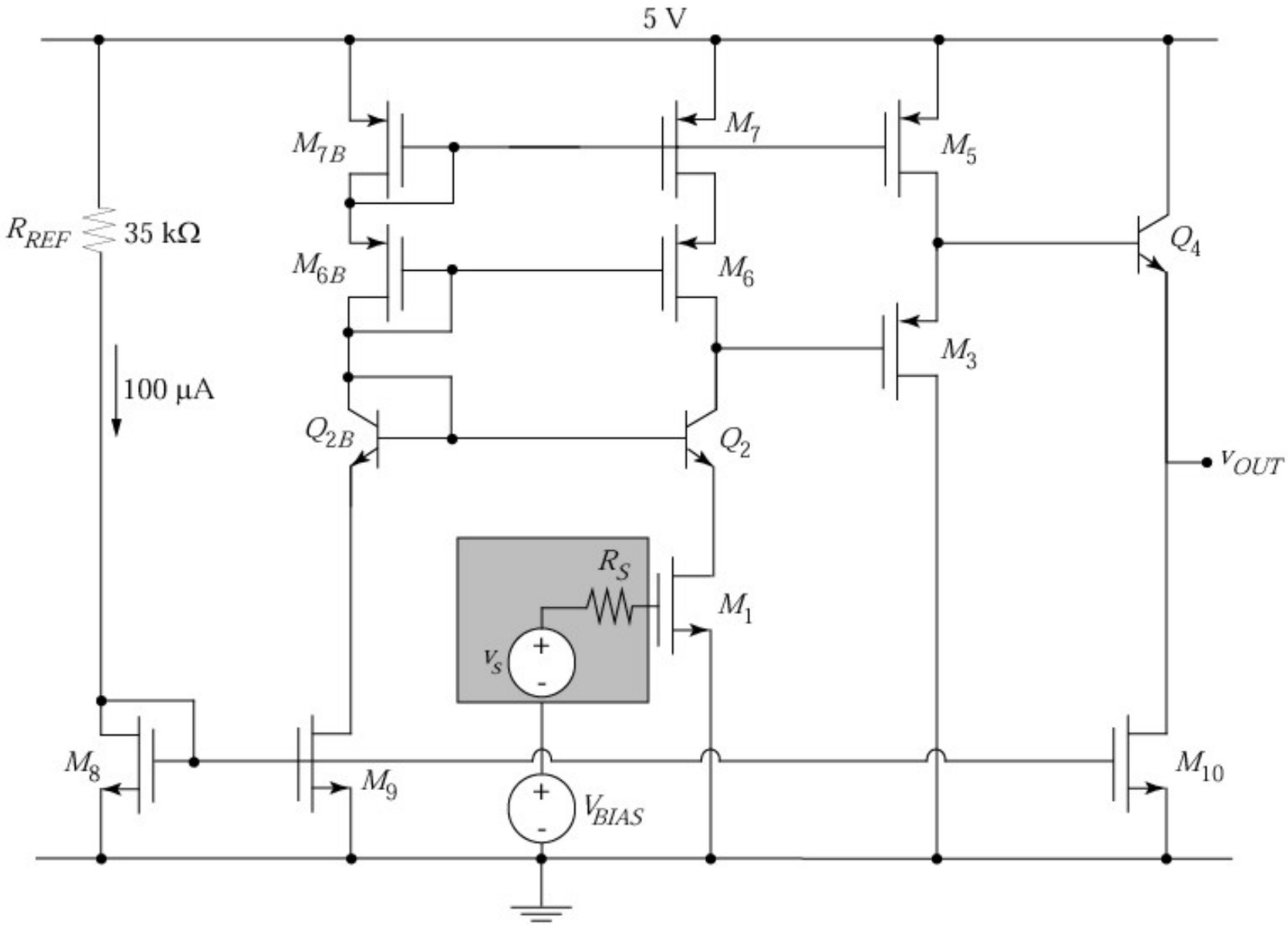


What's Left?



Voltage at base of Q_2 is set by totem pole

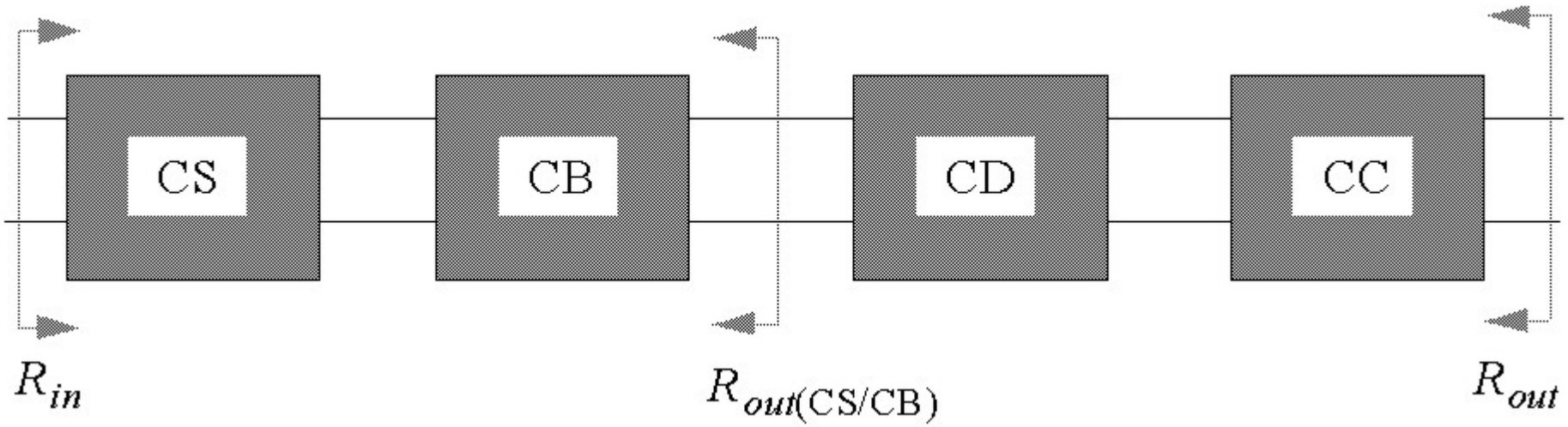
Second Approach: Find Signal Path



Identifying the Stages

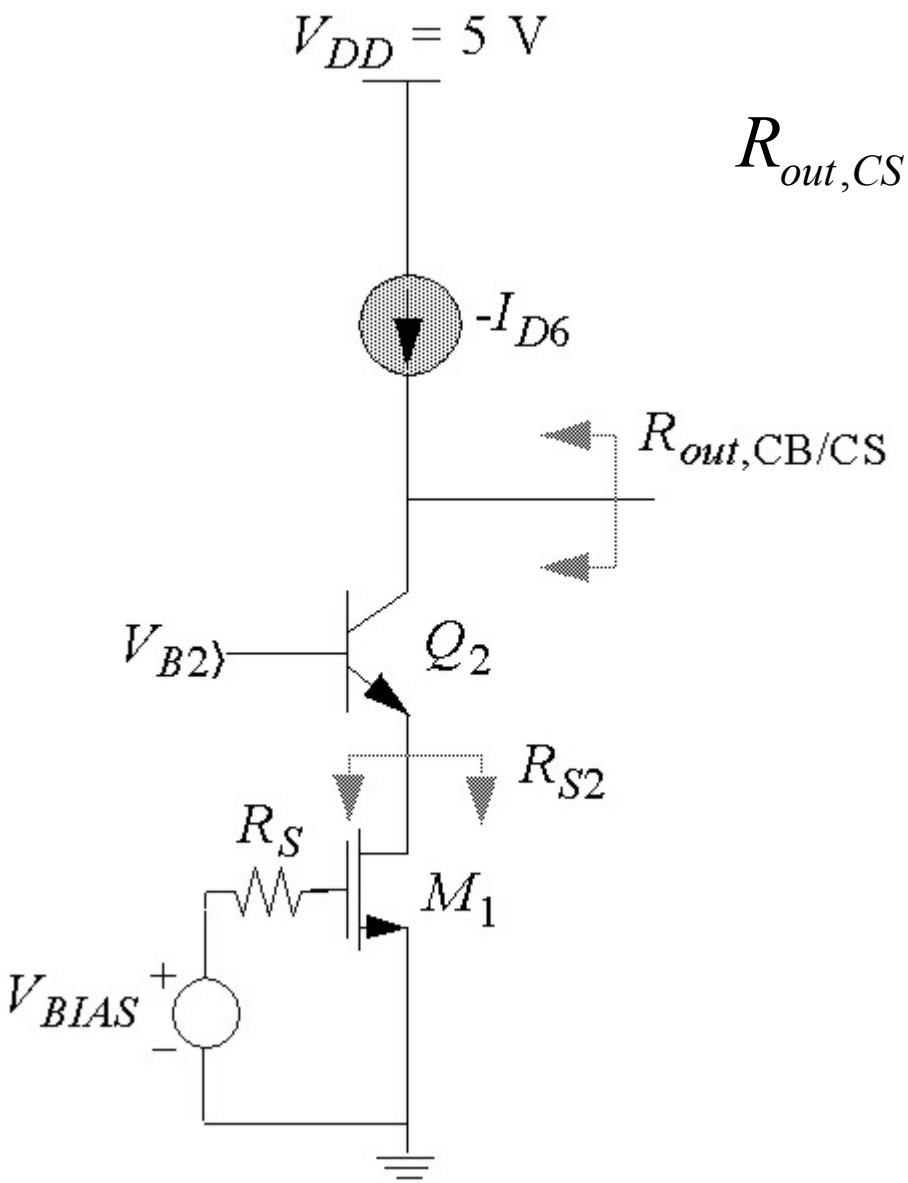
First stage (or two stages): CS/CB cascode

Second stage (or two stages): CD/CC voltage buffer



Why does this make sense for a voltage amplifier?

Find Key Two-Port Parameters

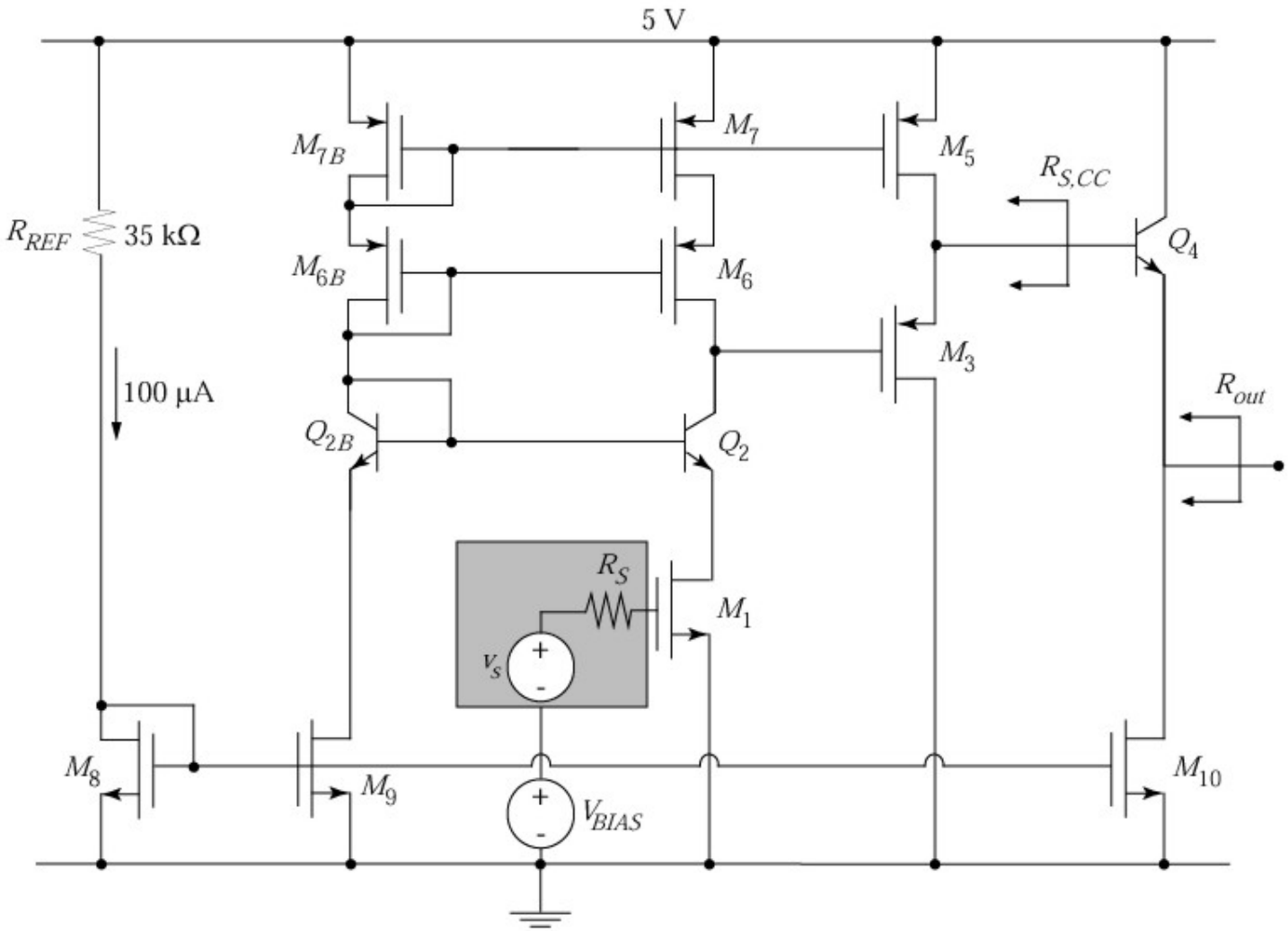


Output resistance of cascode:

$$R_{out,CS/CB} = r_{oc} \,||\, \{r_{o2}(1 + g_{m2}(r_{\pi 2} \,||\, R_{S2})\}$$

$$r_{oc} = R_{up} = r_{o6}(1 + g_{m6}R_{S6})$$

Two-Port Parameters (Cont.)



Output Resistance and Voltage Gain

Source resistance of the CC stage is the output resistance of the CD stage (small)

$$R_{out} = R_{out,CC} = \frac{1}{g_{m4}} + \frac{R_{S,CC}}{\beta_o} = \frac{1}{g_{m4}} + \frac{1}{g_{m3}\beta_o} \approx \frac{1}{g_{m4}}$$

Open-circuit voltage gain A_v (last two stages have nearly unity gain):

$$A_v = -g_{m1}\left(\beta_o r_{o2} \,\|\, r_{o6}\left(1 + g_{m6} r_{o7}\right)\right)$$