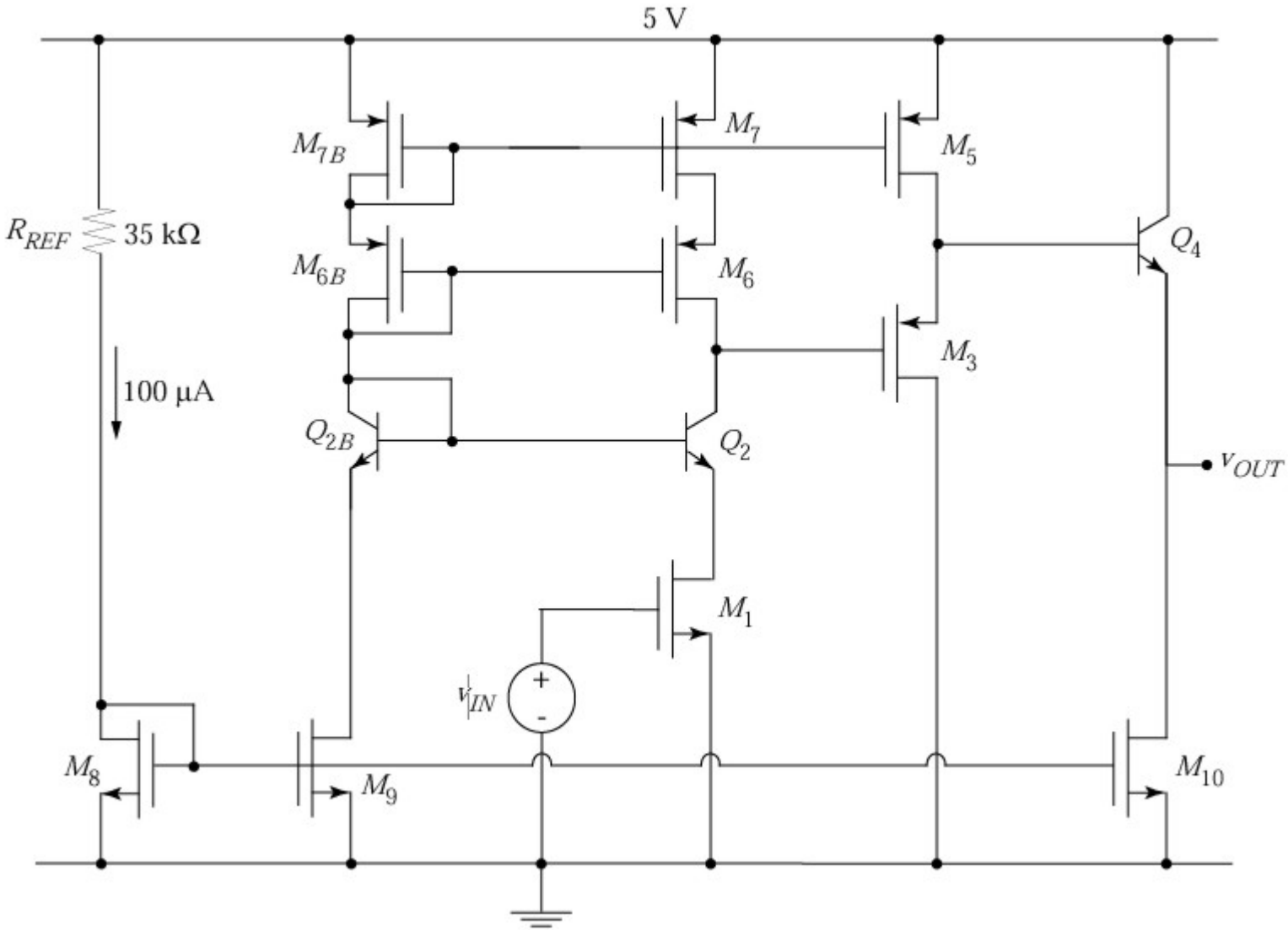
Lecture 39

- Last time:
  - BiCMOS voltage amplifier: example of "dissection" technique for a complicated circuit
- Today :
  - Bias and output swing for BiCMOS voltage amp
  - Start open-circuit time constant analysis (back to Chapter 10)

DC Bias


5 V
M_{7B}
M_7
M_5
R_{REF}
35 kΩ
M_{6B}
M_6
Q_4
M_3
100 μA
Q_{2B}
Q_2
v_{OUT}
M_1
v_{IN}
M_8
M_9
M_{10}

DC Bias (Cont.)

Simplifying assumption: $V_{GSn} = 1.5V = V_{SGp}$

Cascode current supply and totem pole:

diode connected devices set both source-gate and source-drain voltages

select input bias voltage such that $I_{D1} = I_{D9}$

devices M_1, Q_2, M_6, and M_7 must have same $|V_{DS}|$ or V_{CE} as M_9, Q_{2B}, M_{6B}, and M_{7B} (2^{nd} order effect) → sometimes called "replica biasing"

Output Swing: $V_{OUT,MIN}$

Minimum output voltage: M_{10}, M_3 , and Q_2 are "suspects"

M_{10} goes into triode when $V_{OUT} = \underline{0.5\ \text{V}}$

M_3 goes into triode when $V_{SD3} = 0.5$ V →

$V_{OUT} = 0.5\ \text{V} - 0.7\ \text{V} = \underline{-0.2\ \text{V}}$

Q_2 goes into saturation when $V_{CE2} = 0.1$ V

or $V_{BC2} = 0.6$ V

$V_{OUT} = V_{B2} - V_{BC2} + V_{SG3} - V_{BE4}$

$= 2\ \text{V} - 0.6\ \text{V} + 1.5\ \text{V} - 0.7\ \text{V}$

$V_{OUT} = \underline{2.2\ \text{V}}$

Output Swing: $V_{OUT,MAX}$

Maximum output voltage: Q_4, M_5, and M_6 are "suspects"

Q_4 goes into saturation when $V_{CE4} = 0.1$ V → $V_{OUT} = \underline{4.9\text{ V}}$

M_5 goes triode when $V_{SD5} = 0.5$ V → $V_{OUT} = \underline{3.8\text{ V}}$

M_6 goes triode when $V_{SD6} = 0.5$ V →

$$V_{OUT} = V_{S6} - 0.5\text{ V} + V_{SG3} - V_{BE4}$$
$$= 3.5 - 0.5 + 1.5 - 0.7\text{ V} = \underline{3.8\text{ V}}$$

Frequency Response of Multistage Amplifiers

We need a *systematic technique* rather than a bunch of qualitative results (e.g., CS suffers from Miller effect, CD and CG are wideband stages …)

Disappointing news: our analytical technique is capable of estimating only the dominant (lowest) pole … for a restricted class of amplifiers.

The Special Case

The transfer function can have *no zeroes* and must have a *dominant* pole $\omega_1 << \omega_2, \omega_3, \ldots, \omega_n$

$$H(j\omega) = \frac{H_o}{\left(1 + j\omega b_1 + (j\omega)^2 b_2 + (j\omega)^3 b_3 + \ldots\right)}$$

Factor denominator:

$$H(j\omega) = \frac{H_o}{\left(1 + j\omega/\omega_1\right)\left(1 + j\omega/\omega_2\right)\ldots\left(1 + j\omega/\omega_n\right)}$$

Approximating the Transfer Function

Multiply out denominator:

$$H(j\omega) = \frac{H_o}{(1+j\omega/\omega_1)(1+j\omega/\omega_2)\ldots(1+j\omega/\omega_n)} \approx$$

$$\frac{H_o}{1+j\omega\left(\frac{1}{\omega_1}+\frac{1}{\omega_2}+\ldots+\frac{1}{\omega_n}\right)}$$

Since $\omega_1 << \omega_2, \omega_3, \ldots, \omega_n \rightarrow$

$$b_1 = \frac{1}{\omega_1}+\frac{1}{\omega_2}+\ldots+\frac{1}{\omega_n} \approx \frac{1}{\omega_1}$$

How to Find b_1?

See P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits* (EE 140) for derivation

Result: b_1 is the sum of *open-circuit time constants* τ_i which can be found by considering each capacitor C_i in the amplifier separately and finding its Thévenin resistance R_{Ti} →

$$\tau_i = R_{Ti} C_i$$

$$b_1 = \sum_{i=1}^{n} R_{Ti} C_i \longrightarrow \boxed{\omega_1 \approx \frac{1}{\sum_{i=1}^{n} R_{Ti} C_i}}$$

Finding the Thévenin Resistance

1. Open-circuit all capacitors (i.e.; remove them)

2. For capacitor C_i, find the resistance R_{Ti} across its terminals with all independent sources removed (voltages shorted, currents opened) … might need to apply a test voltage and find the current in some cases.

Insight for design: the bandwidth of the amplifier will be limited by the capacitor that contributes the largest $\tau_i = R_{Ti} C_i$ → not necessarily the largest C_i