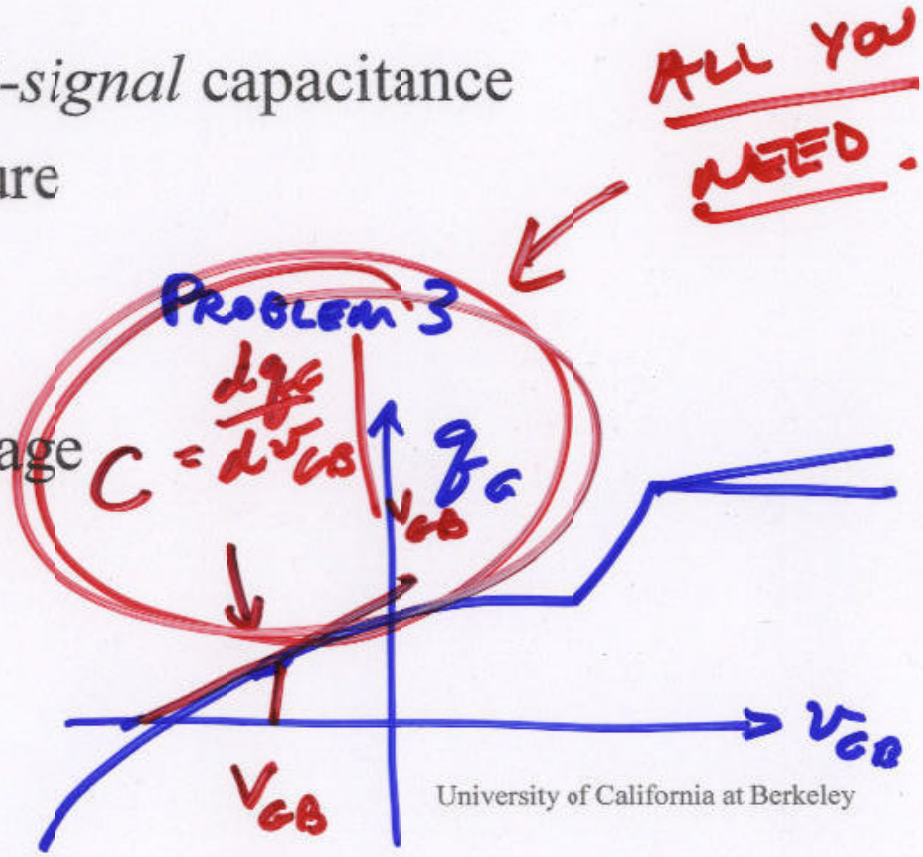
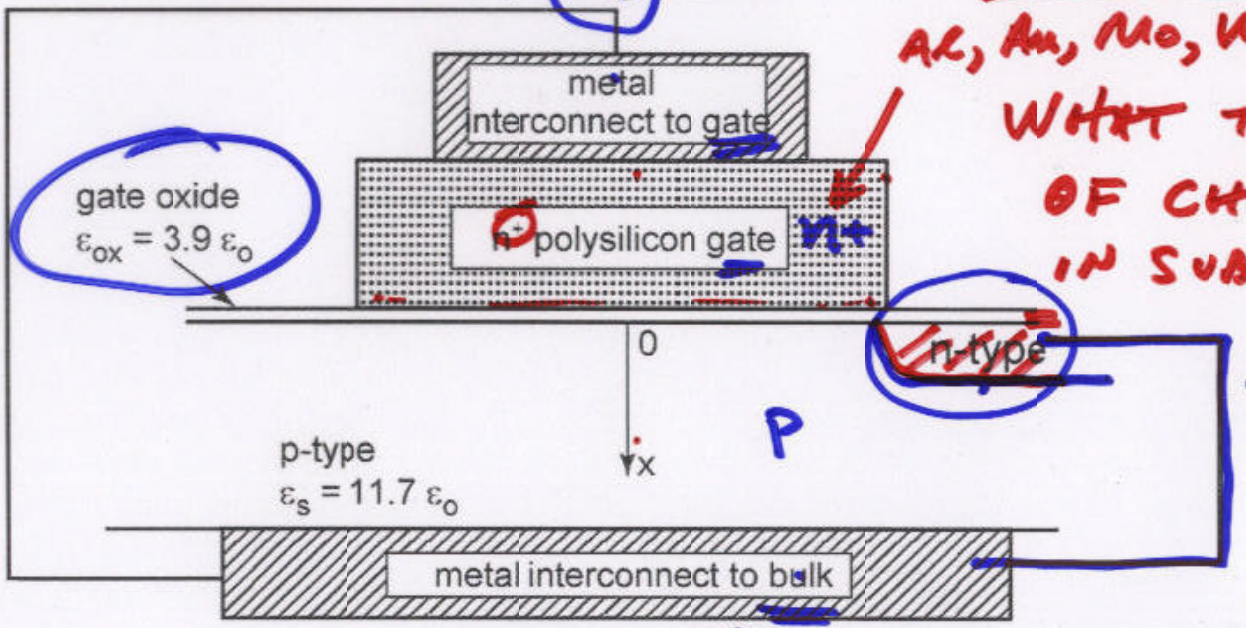
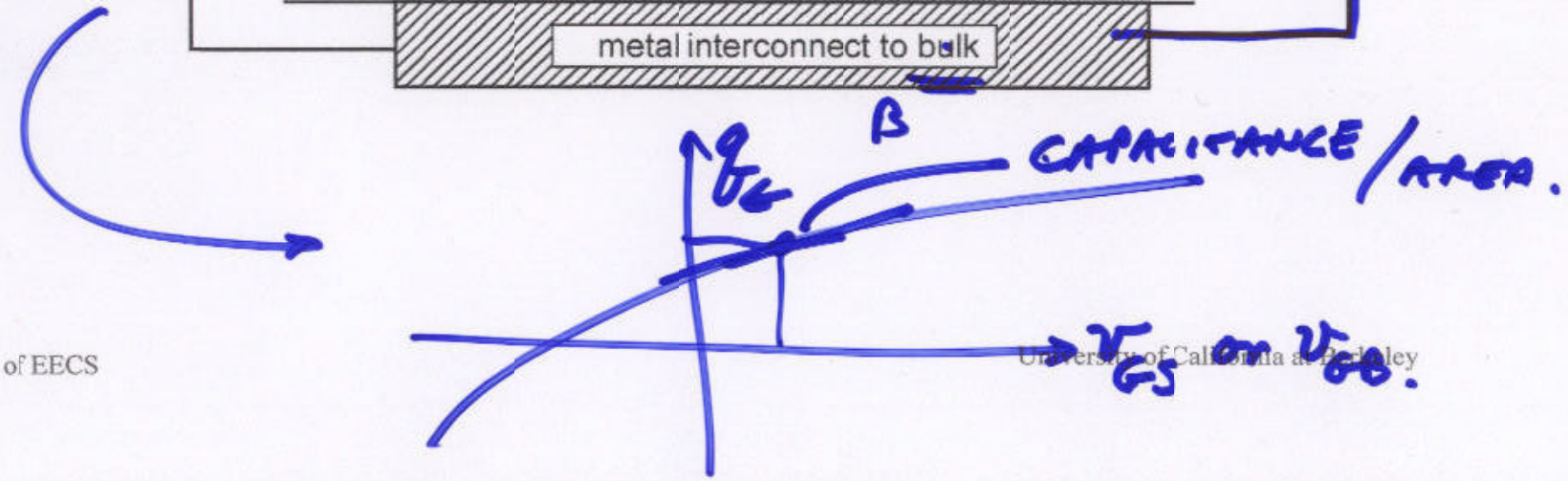
Lecture 12

- Last time:
  - pn junction *small-signal* capacitance
  - start MOS structure
- Today :
  - MOS charge storage
  - MOS capacitor



MOS Structure

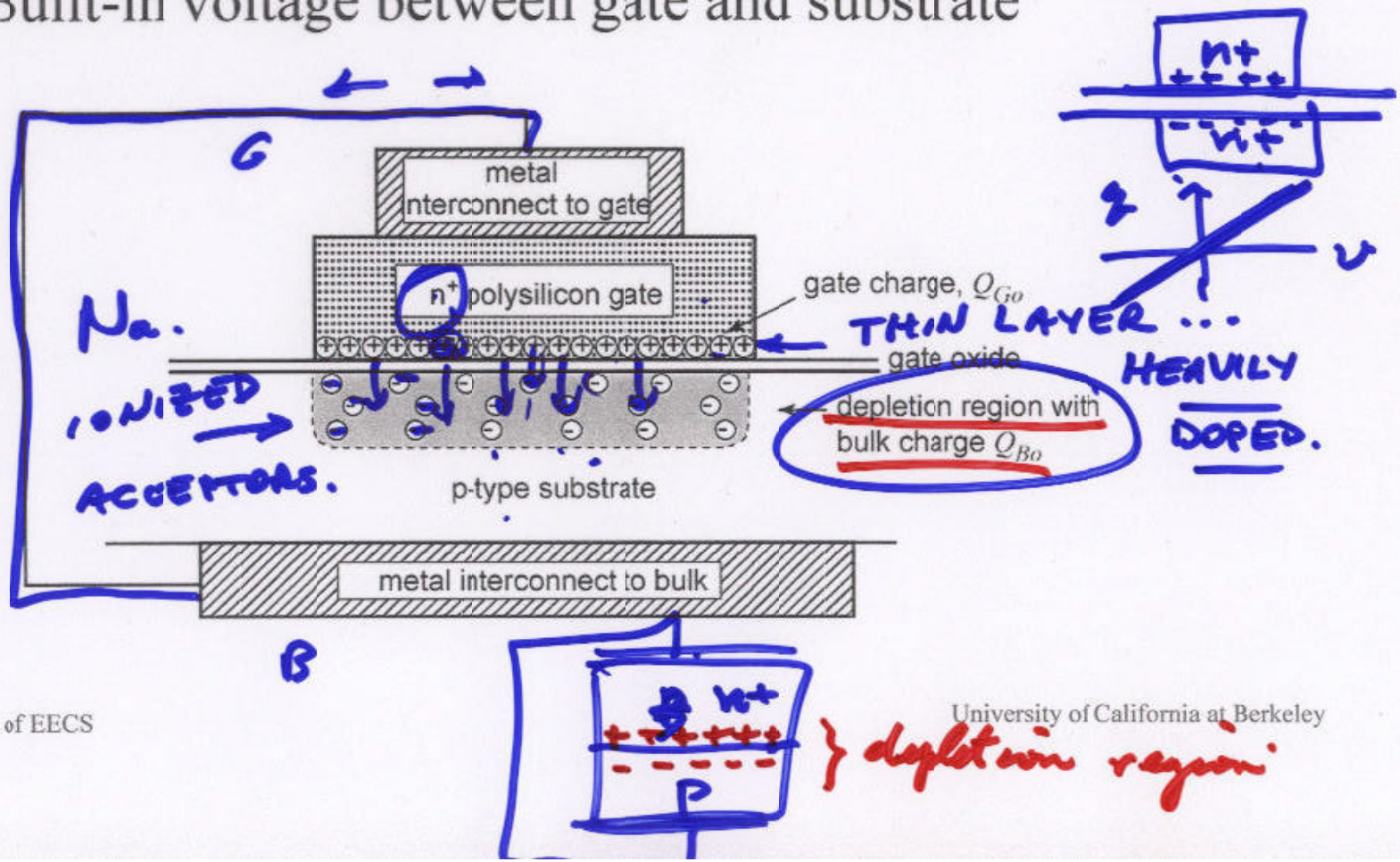




Thermal Equilibrium.

Charged bi-layer forms: + charges on gate, - in substrate

Built-in voltage between gate and substrate



Applying a DC Voltage V_{GB}

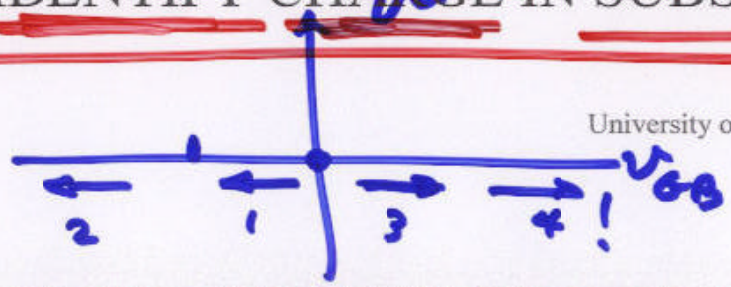
Goal: find out how the gate charge Q_G varies as a function of the applied voltage V_{GB}

Procedure: start at thermal equilibrium. $V_{GB} = 0$ V.

(i) go negative until built-in charge is cancelled.
(ii) keep going until charge on gate is negative
(iii) go positive from thermal equilibrium
(iv) keep increasing V_{GB} until …

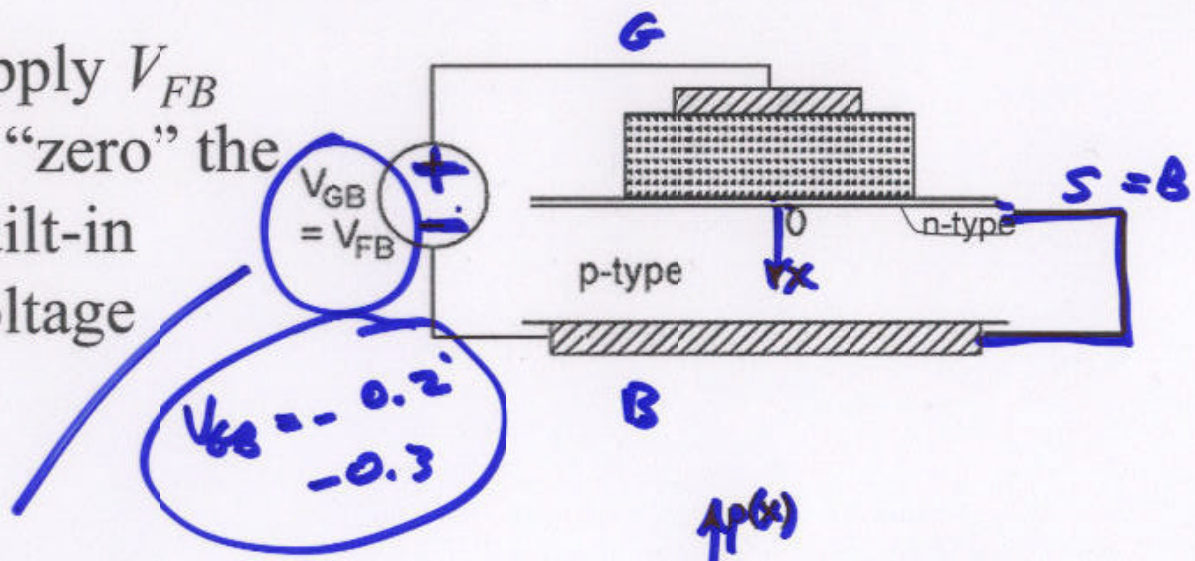
WHAT ARE THEY?

☞IMPORTANT: IDENTIFY CHARGE IN SUBSTRATE



Cancel the Built-in Voltage

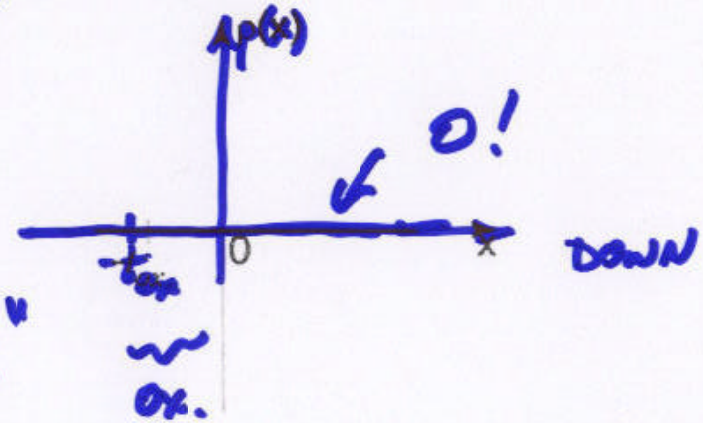
Apply V_{FB} to "zero" the built-in voltage



THERMAL EQUIL.

$V_{GB} = -0.2$ -0.3

$V_{GB} < 0$.



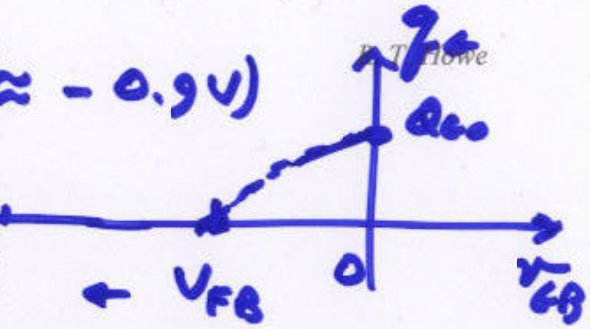
V_{FB} = "flat band" voltage.

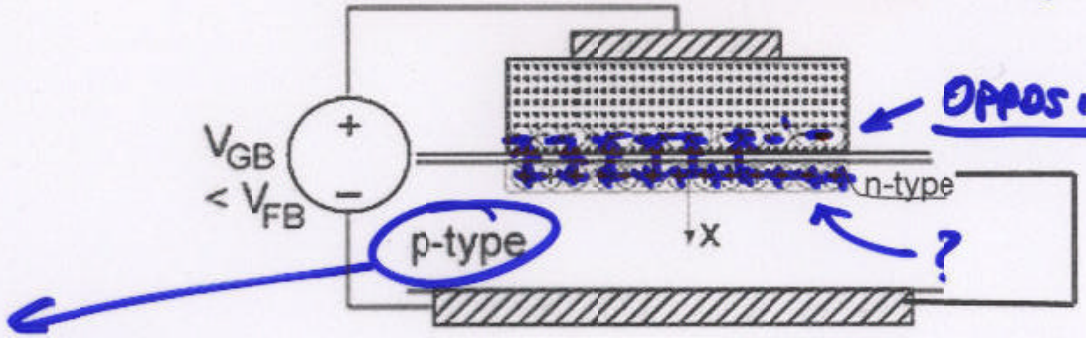
$= -0.9$ V.

(1)

Accumulation

$V_{GB} < V_{FB}$ (≈ -0.9 V)



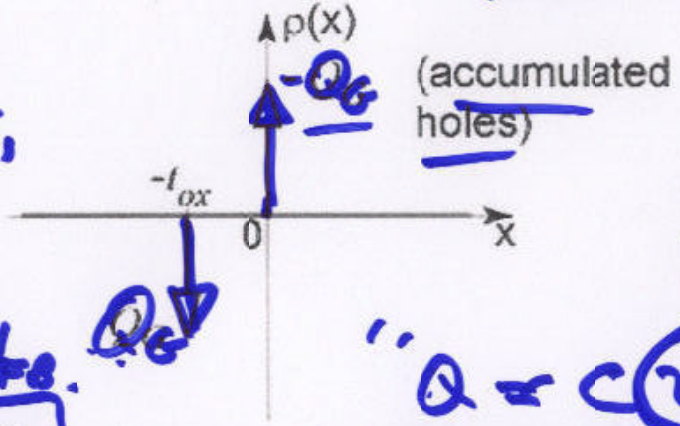


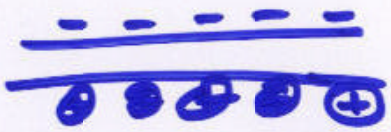
OPPOSITES ATTRACT:

- DOPED WITH B... NEGATIVE CHARGE...

HOLES! MOBILE, + CHARGE.

"METAL-METAL CAP."





$V_{GB} < V_{FB}$.

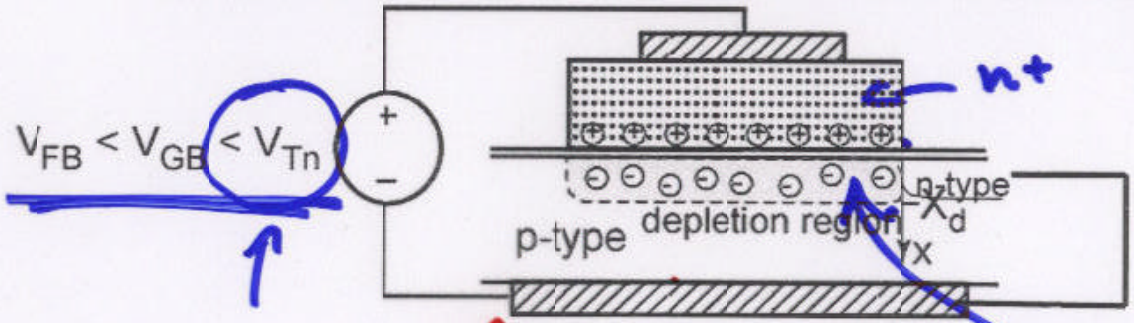
"$Q = CV$" ← TRUE FOR $V_{GB} < V_{FB}$

$$Q_G = C_{ox}(V_{GB} - V_{FB}) \qquad C = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \rightarrow \approx \frac{4\epsilon_0}{11.3\epsilon_0}$$

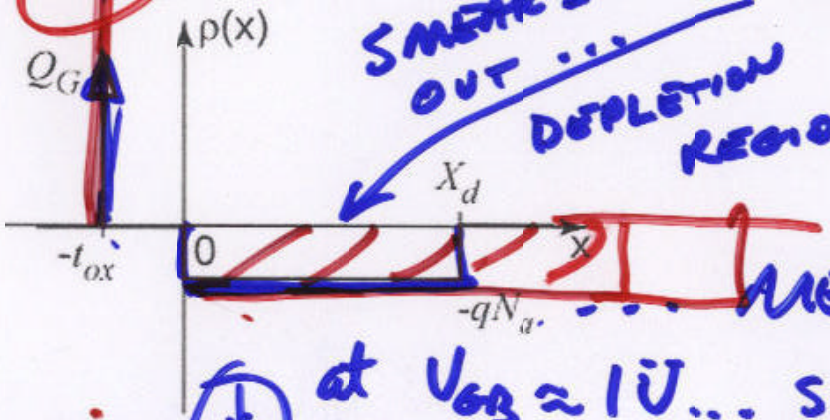
$0 > V_{FB} \approx -0.8\,V$

3 Depletion: $V_{GB} > V_{FB}$

[SAME AS THERMAL EQUIL!



IONIZED ACCEPTORS.



SMEARED OUT ... DEPLETION REGION.

$\times$ [$Q_G = f(V_{GB})$ FOR $V_{GB} > V_{FB}$]

... MESS!

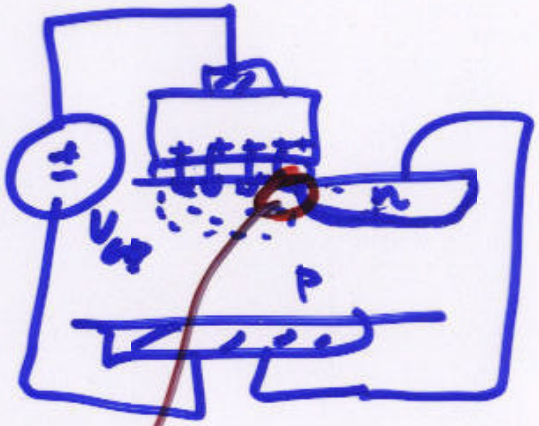
at $V_{GB} \approx 1V$ ... SURPRISE!

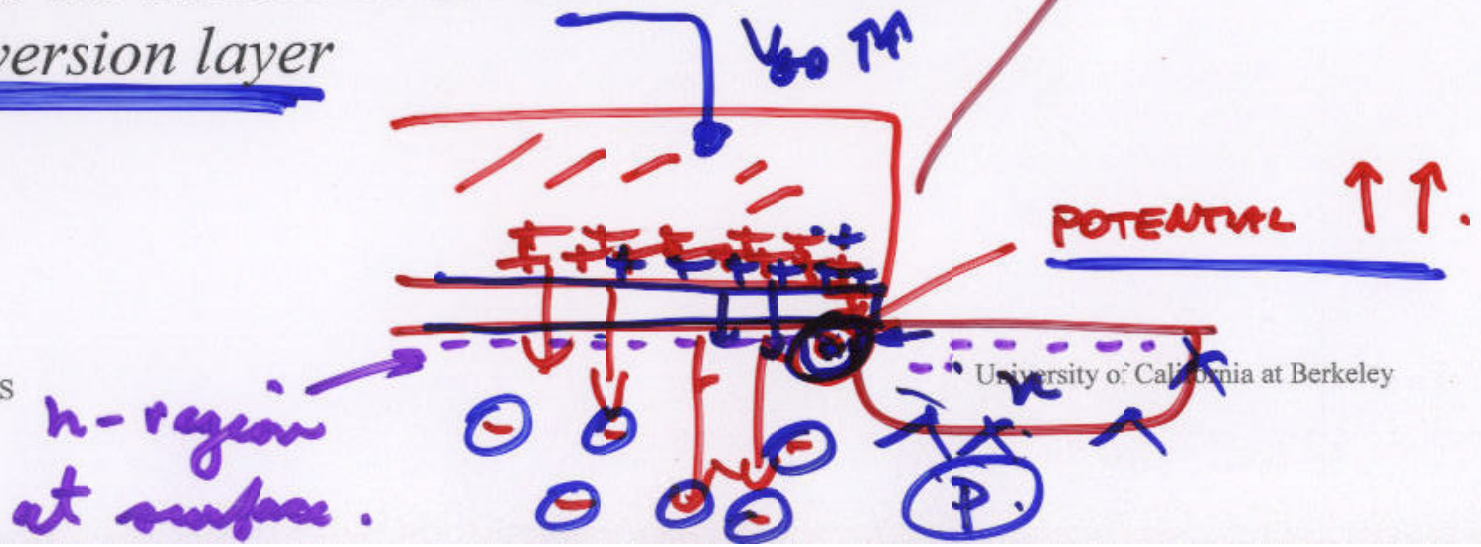
$V_{GB} = 0,\ 0.5,\ 1,\ 1.5,\ 2,\ \ldots\ 20V$

What Happens as V_{GB} Increases?

Vertical E field increases at the surface, lowering the barrier between the n-type region next to the gate and the channel underneath it …

eventually (at $V_{GB} = V_{Tn}$), electrons flood in and the surface of the substrate has an *inversion layer*

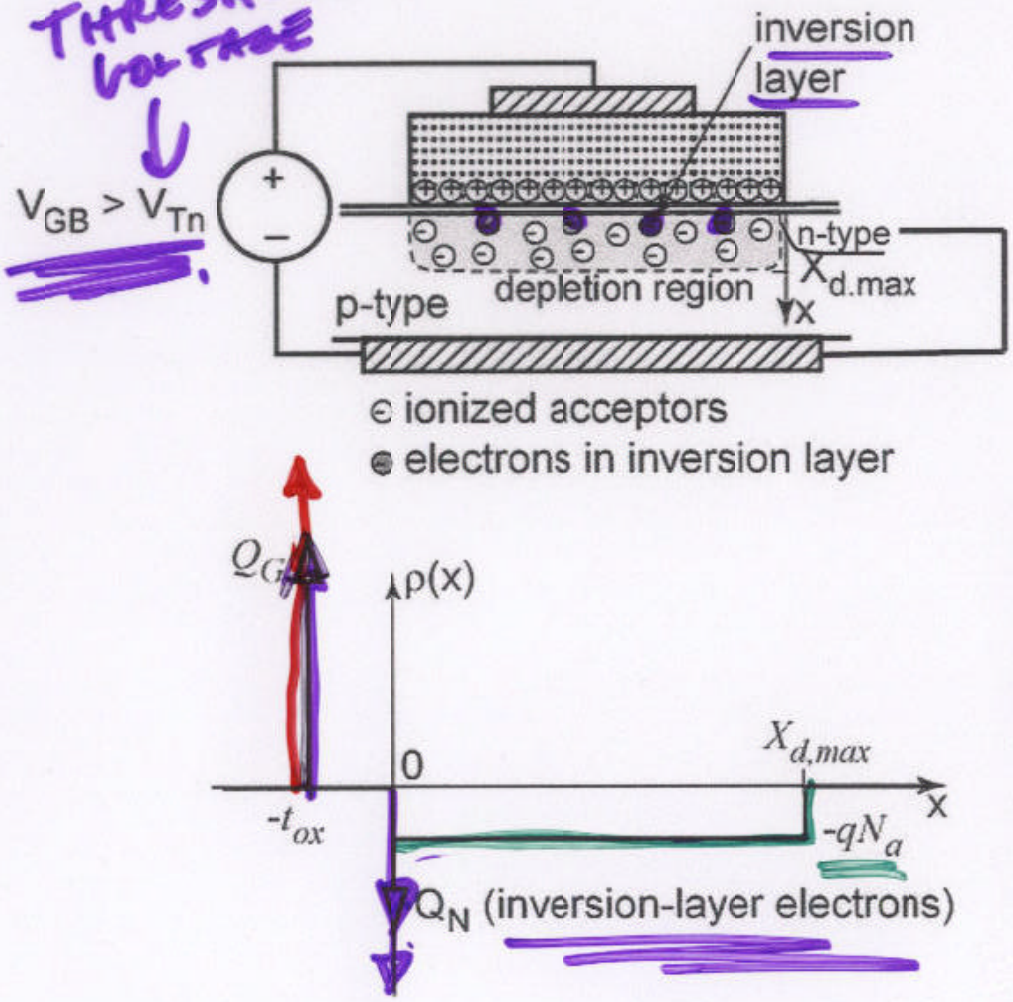




MOS Capacitor in Inversion

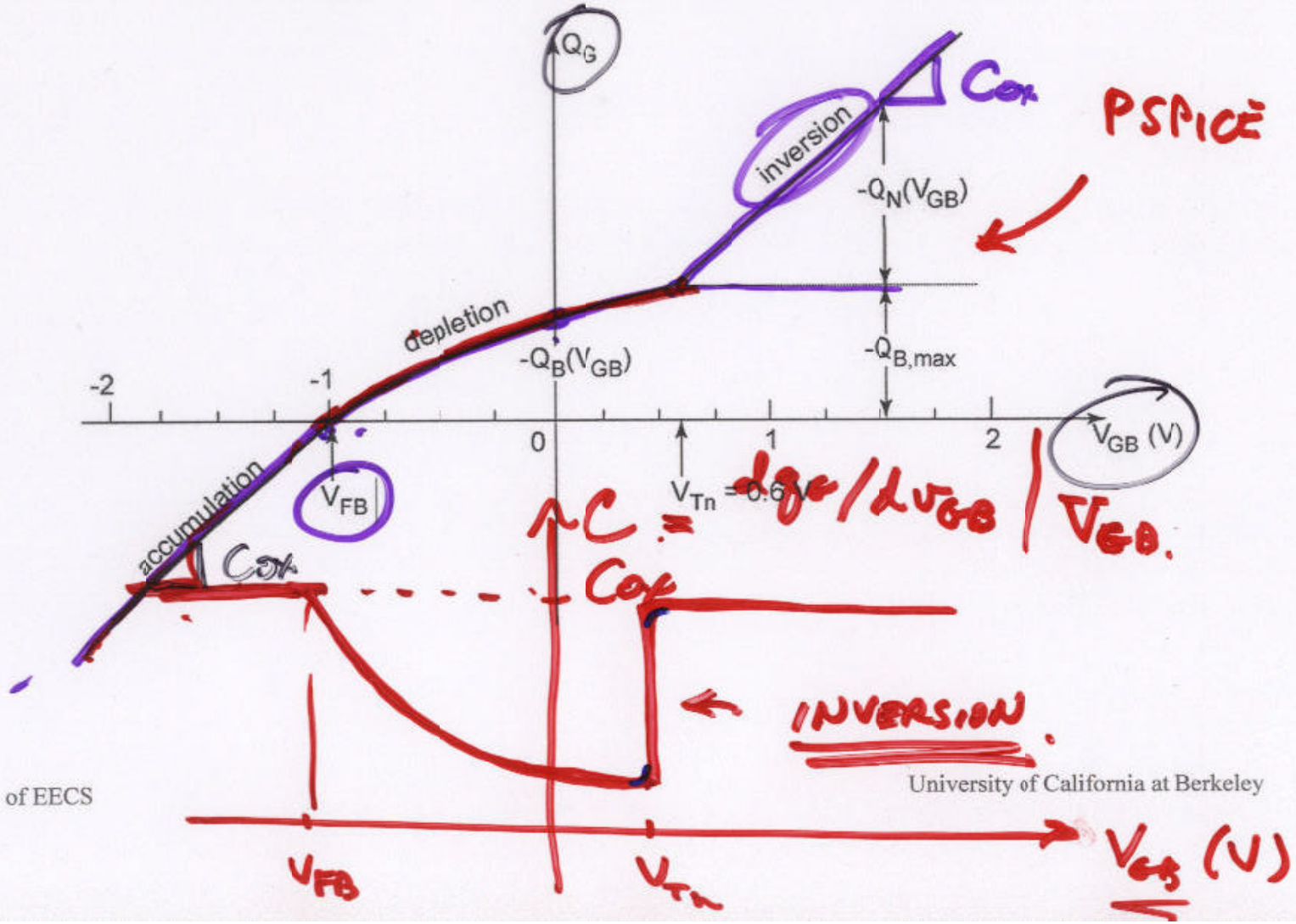
THRESHOLD VOLTAGE

$V_{GB} > V_{Tn}$



Increasing voltage → additional charge stored in inversion layer

Charge vs. Voltage Curve



DERIVATIVE OF Q_s vs. V_{GB}.

MOS Capacitance vs. Voltage