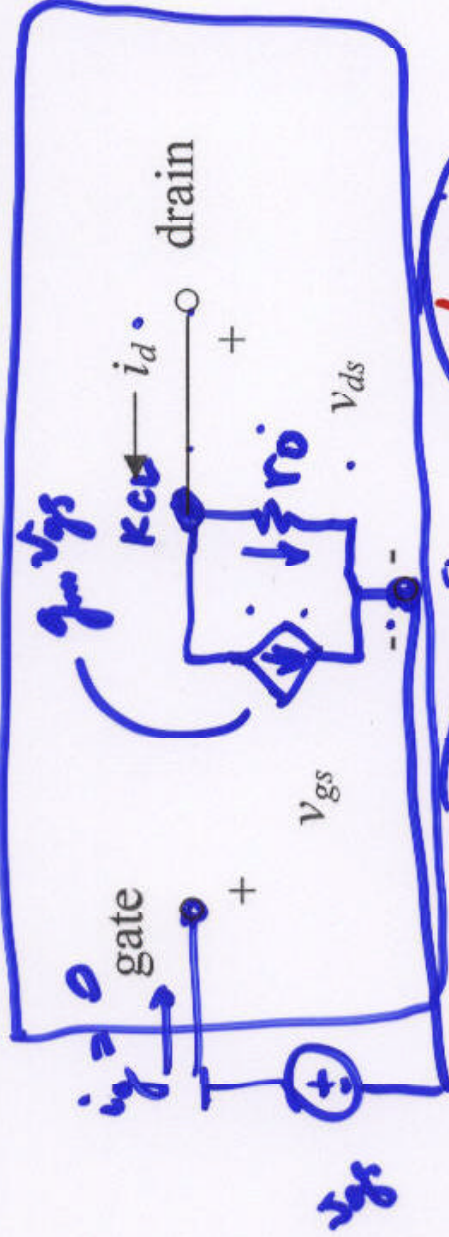


Lecture 16

- Last time:
 - MOSFET small-signal model (g_m , r_o) ✓ ✓
- Today : *Nmos.*
 - Complete small-signal model: add capacitors
 - P-channel MOSFET μ_p, λ_p
 - MOSFET Spice Model

HARD.

Putting Together a Circuit Model



$i_d = \frac{dI_D}{dt} = \frac{\partial I_D}{\partial v_{gs}} \Delta v_{gs} + \frac{\partial I_D}{\partial v_{ds}} \Delta v_{ds} + \dots$ (LOTS OF STUFF)

$$y_o = \left. \frac{\Delta v_{ds}}{\Delta i_o} \right|_Q = \frac{v_{ds}}{i_d}$$
 YES!!

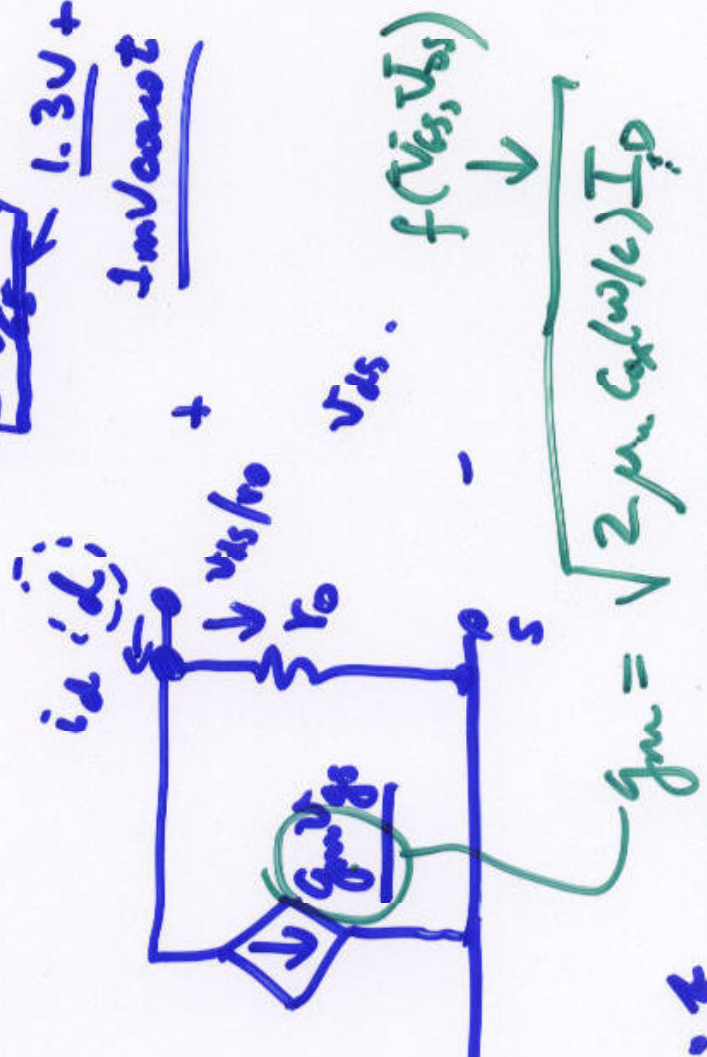
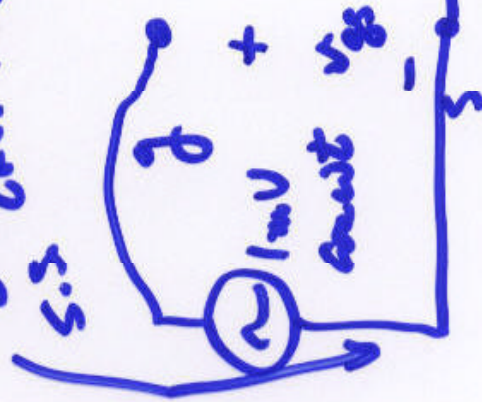
MATH 53

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o} + \frac{\partial i_D}{\partial v_{gs}} \Delta v_{gs}$$

$$\Delta i_D = \frac{\partial i_D}{\partial v_{gs}} \Delta v_{gs} + \frac{\partial i_D}{\partial v_{ds}} \Delta v_{ds}$$

(v_{gs}, v_{ds})

NO DC IN SOURCE Ckt. KCL



• 2

4th TERMINAL.

Role of the Substrate Potential

- Need not be the source potential, but $V_B < V_S$

$$V_{S1} = \phi$$

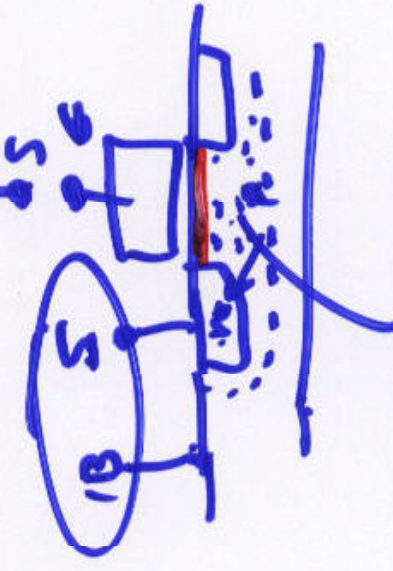
$$V_B = V_S \text{ (common).}$$

Effect: changes threshold voltage, which changes the drain current ... substrate acts like a "backgate" \rightarrow "BOTTOM GATE" LEVEL



$$g_{mb} = \frac{\Delta i_D}{\Delta V_{BS}} \bigg|_Q = \frac{\partial i_D}{\partial V_{BS}} \bigg|_Q$$

$$Q = (V_{GS}, V_{DS}, V_{BS})$$



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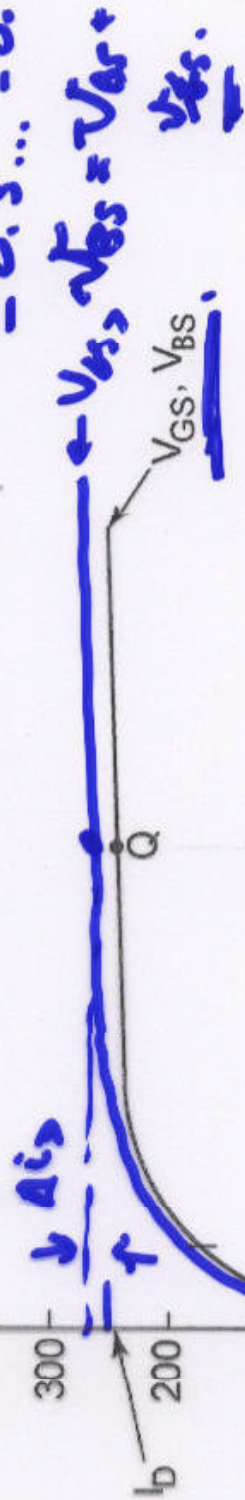
DEPLETION CAPACITANCE BETWEEN B AND CHANNEL

$$I_{D0} = \mu_n C_{ox} (\omega/2L) (v_{gs} - V_{tn})^2 (1 + \lambda_n V_{DS})$$

Backgate Transconductance

$$V_{tn} = V_{t0} + \gamma_n \left\{ \sqrt{V_{DS} - 2\phi_F} - \sqrt{-2\phi_F} \right\}$$

- 0.3... - 0.4



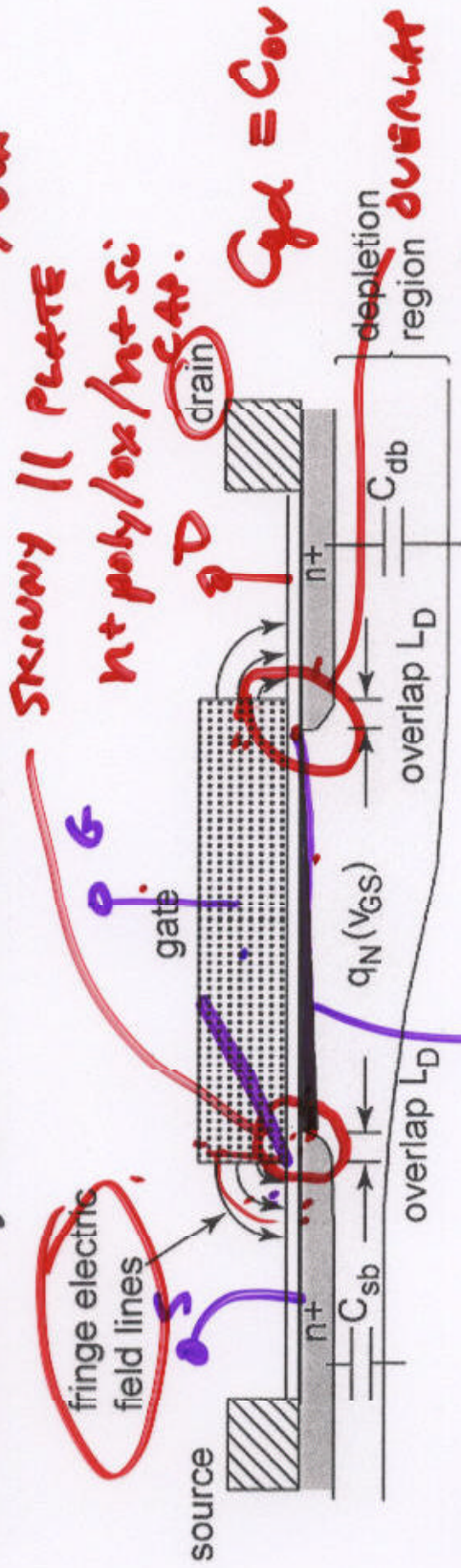
$$\text{Result: } g_{mb} = \frac{\partial i_D}{\partial v_{BS}} \Big|_Q = \frac{\partial i_D}{\partial V_{Tn}} \Big|_Q \frac{\partial V_{Tn}}{\partial v_{BS}} \Big|_Q$$

$$= \frac{\gamma_n g_m}{2\sqrt{-2\phi_F - V_{DS}}} = \frac{\gamma_n g_m}{2\sqrt{-2\phi_F - V_{DS}}}$$

MOSFET Capacitances in Saturation

Gate-source capacitance: channel charge is not controlled by drain in saturation.

$$C_{gs} = \frac{Q_{ch}}{V_{gs}}$$



$$\frac{\partial I_{ds}}{\partial V_{gs}} = g_m$$

$$I_{ds}(V_{ds}) = C_{ox}(V_{ds} - V_{th})$$

(FOR $V_{ds} \text{ SATURATED} \dots$)

FOR SATURATION, IT'S A WEDGE

Gate-Source Capacitance C_{gs}

Wedge-shaped charge in saturation \rightarrow effective area is $(2/3)WL$
 (see H&S 4.5.4 for details)

$$C_{gs} = \underbrace{(2/3)WL}_{\text{Area}} \underbrace{C_{ox}/t_{ox}}_{\text{ff}(\mu\text{m}^2)} + C_{ov}$$

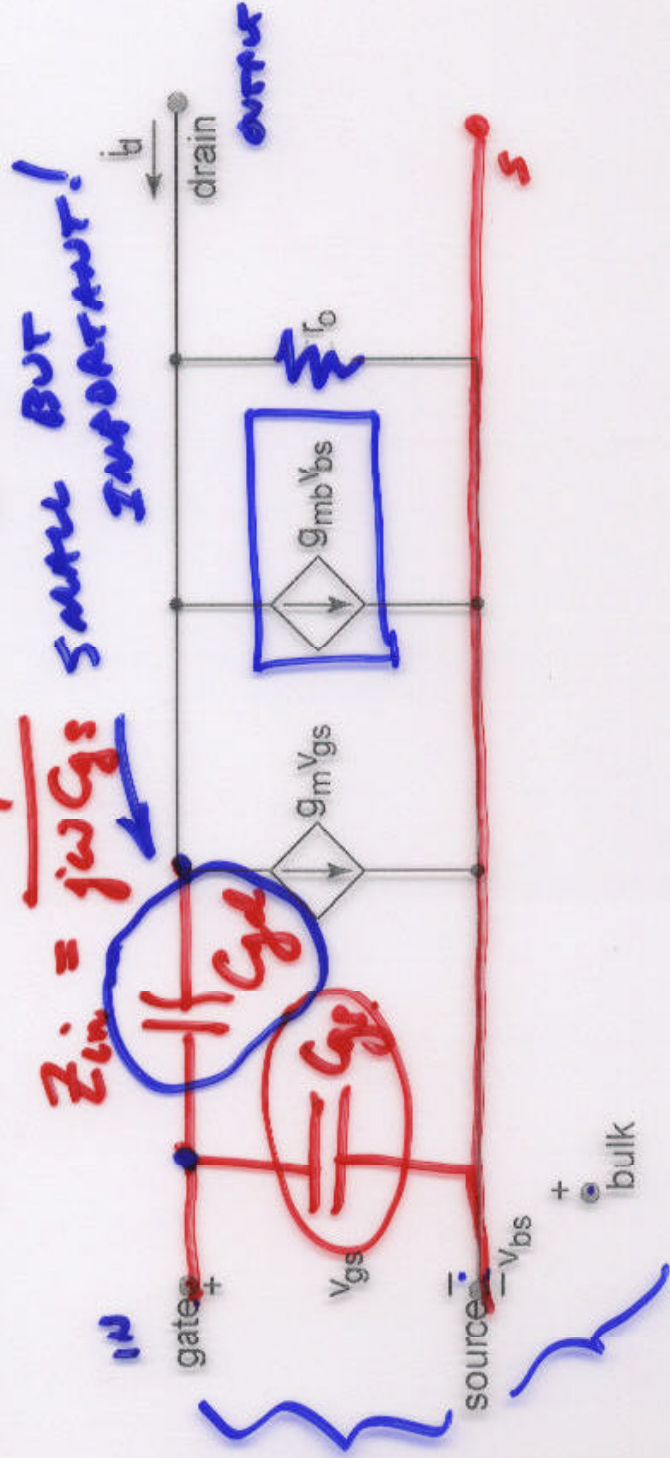
Overlap capacitance along source edge of gate \rightarrow

$$C_{ov} = L_D WC_{ox}$$

(Underestimate due to fringing fields)



Four-Terminal Small-Signal Model



CHANGE = f(VOLTAGE)

$\approx G-S$
 $G-D$
 $D-A$
 $S-D$

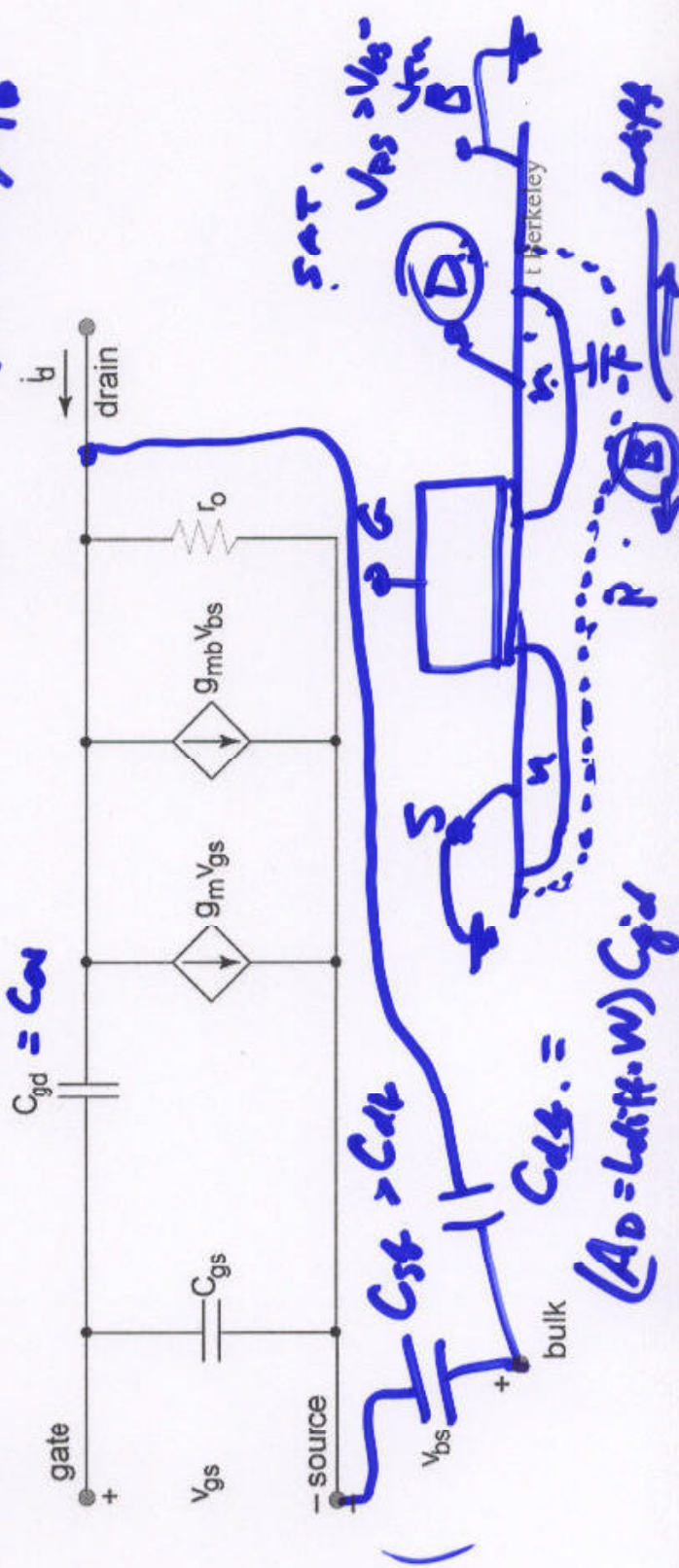
Gate-Drain Capacitance C_{gd}

Not due to change in inversion charge in channel

Overlap capacitance C_{ov} between drain and source

is C_{gd}

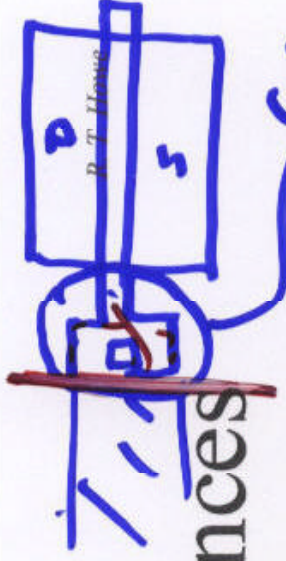
$$C_{gd} = \frac{C_{j0}}{\sqrt{1 + V_{ds}/\phi_0}}$$



C_w

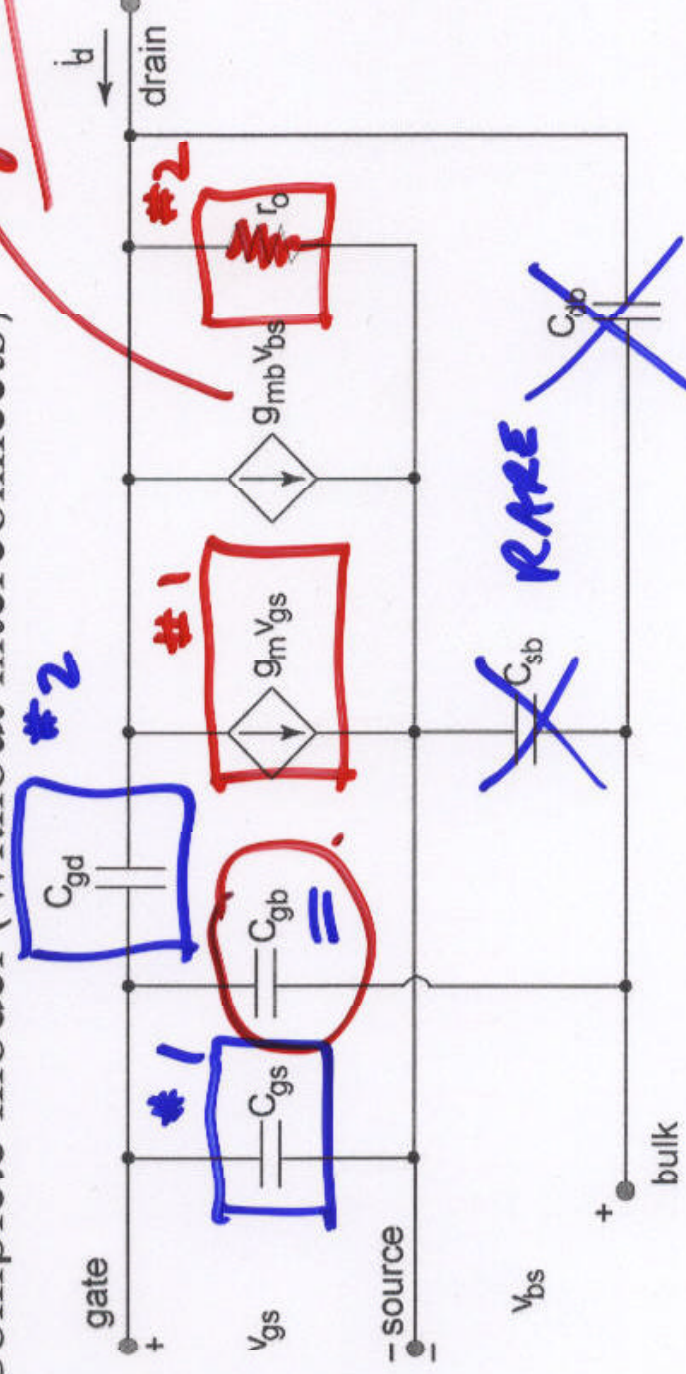
Junction Capacitances

Drain and source diffusions have (different) junction capacitances since V_{SB} and $V_{DB} = V_{SB} + V_{DS}$ aren't the same



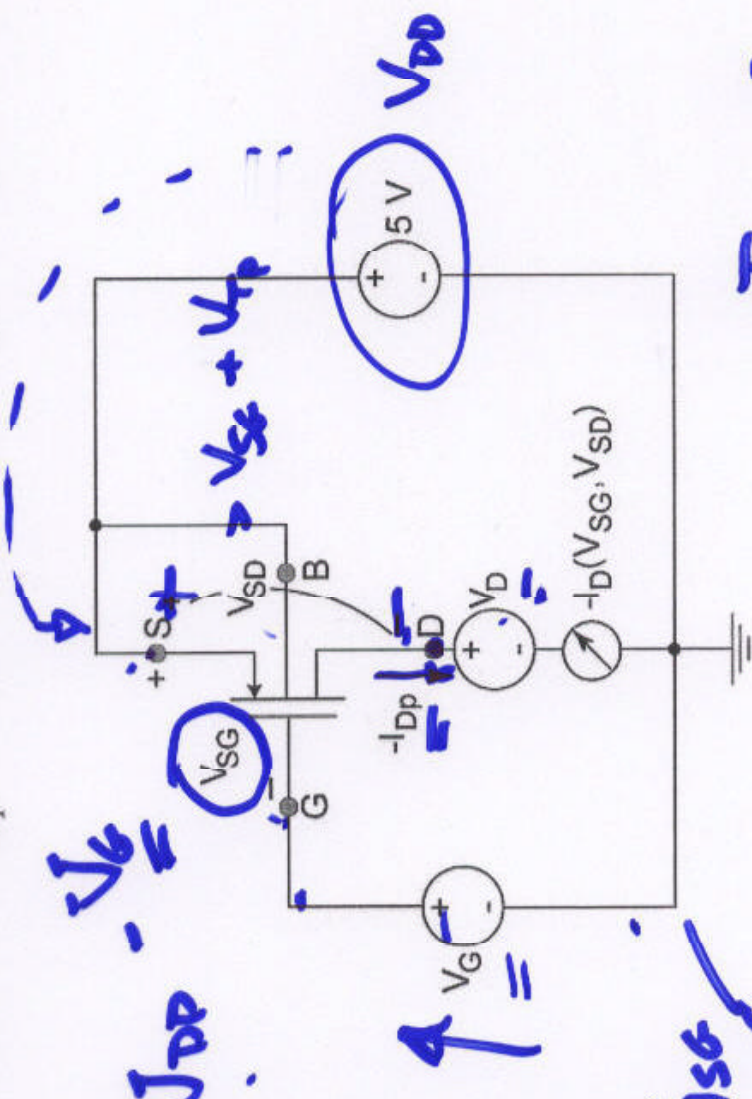
Complete model (without interconnects)

gmb ≈ 0.1 gm



P-Channel MOSFET

Measurement of $-I_{Dp}$ versus V_{SD} , with V_{SG} as a parameter:



$V_{SG} = V_{DD} - V_G = V_{SG}$

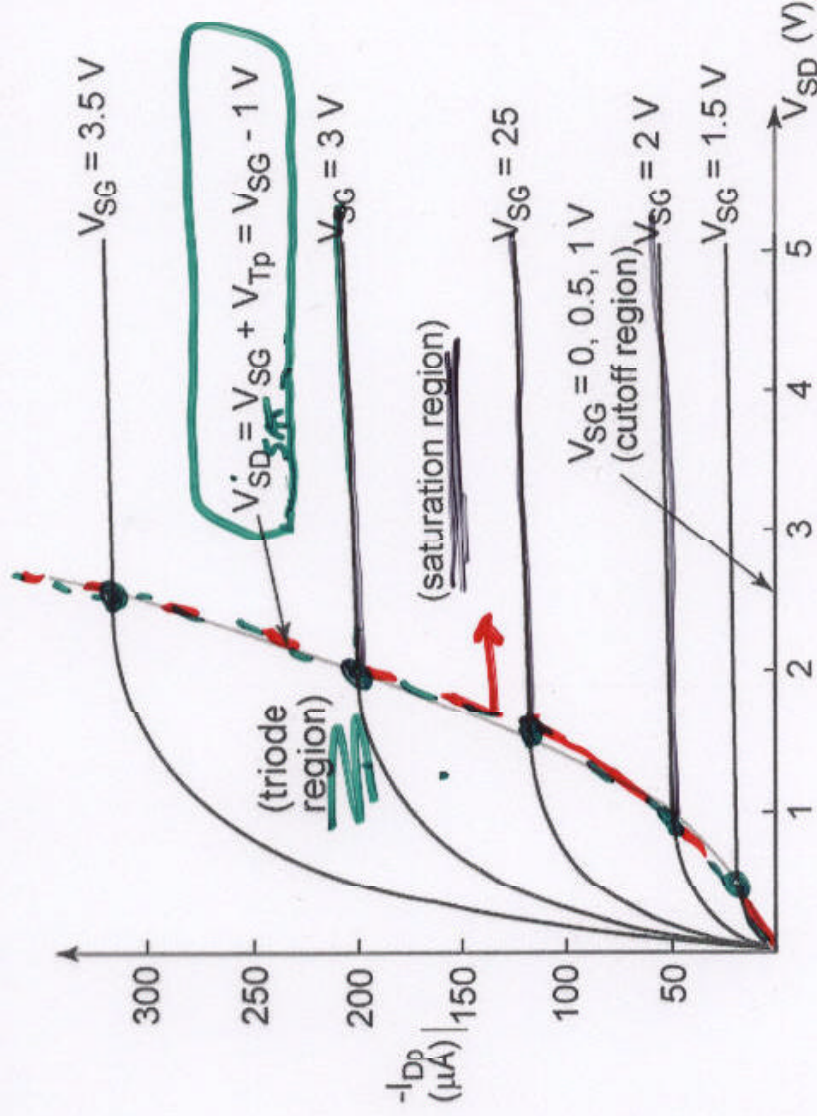
$V_{SG} = V_{SD} + V_{TP}$

PLOT vs. V_{SD}

$-I_{Dp}$ vs. V_{SD}
 $V_{SD} \dots V_{TP} = -1V$

$-I_{Dp} > 0$

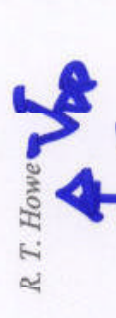
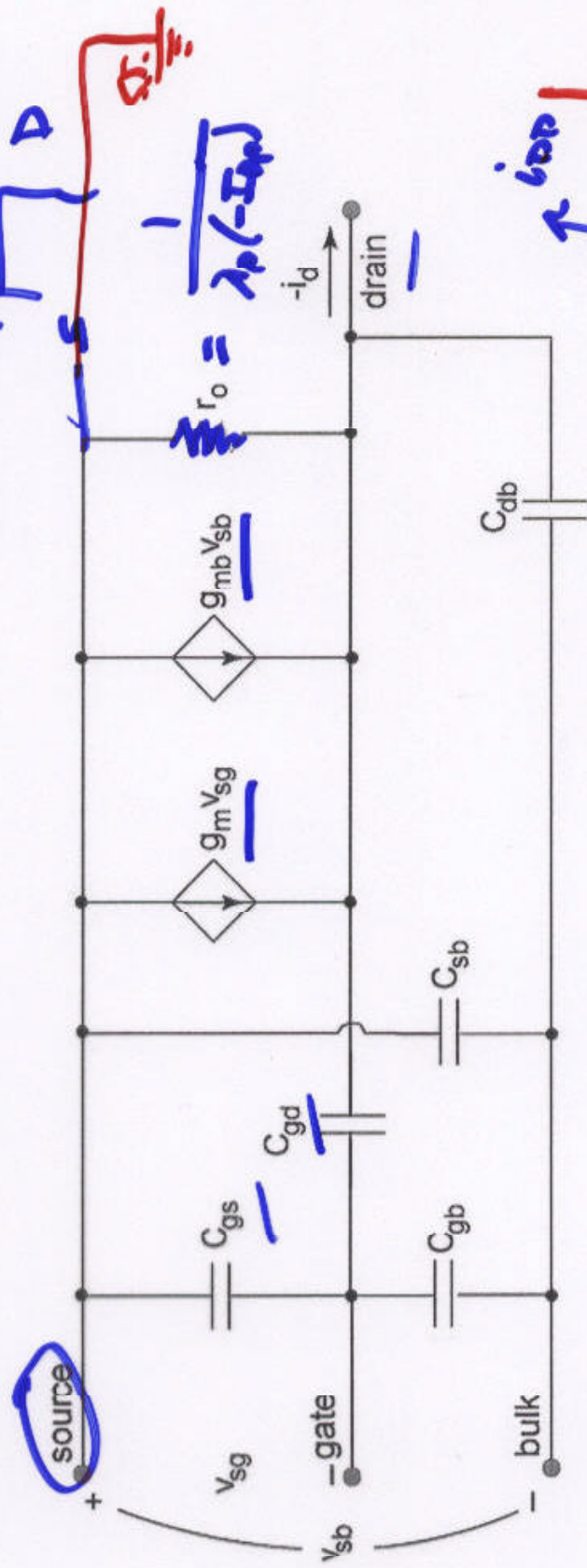
Square-Law PMOS Characteristics



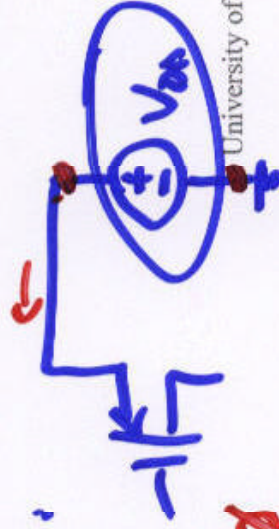
$$-I_{Dp,sat} = \frac{\mu_p C_{ox}}{2L} (V_{SG} + V_{Tp})^2 (1 + \lambda V_{SD})$$

$$V_{SD} \geq V_{SG} + V_{Tp}; V_{SD} \leq -V_{Tp} < 0$$

Small-Signal PMOS Model



Small-signal model:



$$r_{out} = \left(\frac{\partial i_{out}}{\partial v_{out}} \right) = \phi$$

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$$\frac{\partial v_{out}}{\partial v_{in}} = \infty$$

MOSFET SPICE Model

- Many “levels” ... we will use the square-law EE 231
 - “Level 1” model BSIM, EE 140/240.
- See H&S 4.6 + Spice refs. on reserve for details.

240 MODEL MODN NMOS LEVEL=1 VTO = 1 KP = 50U LAMEDA = .033 GAMMA = .6
 + PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 1E-4 CJSW = 5E-10
 + MJ = 0.5 PB = 0.95

MODEL MODP PMOS LEVEL=1 VTO = -1 KP = 25U LAMBDA = .033 GAMMA = .6
 + PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 3E-4 CJSW = 3.5E-10
 + MJ = 0.5 PB = 0.95