R. T. Howe

MY OH TUES: ~~10:30-12~~ 2 → 3 PM.

Lecture 19

EXAMS: PICK UP IN 497 CORY FROM ROBIN

REGRADES: DROP OFF ~~IN 497~~ WITH ROBIN.

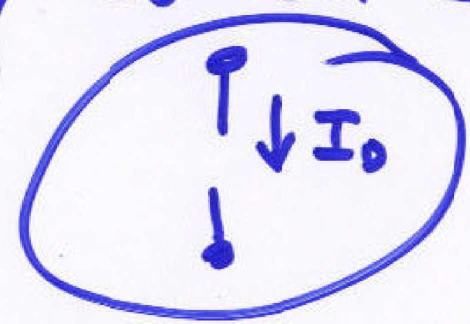
- Last time:
  - DC and small-signal model of the forward-biased diode (FINISH)
- Today :
  - the npn bipolar junction transistor (BJT): large-signal characteristics (BJT)

BIPOLAR TRANSISTOR LAB.

READ! pp. 391-395
413-416 (EBERS-MOLL)

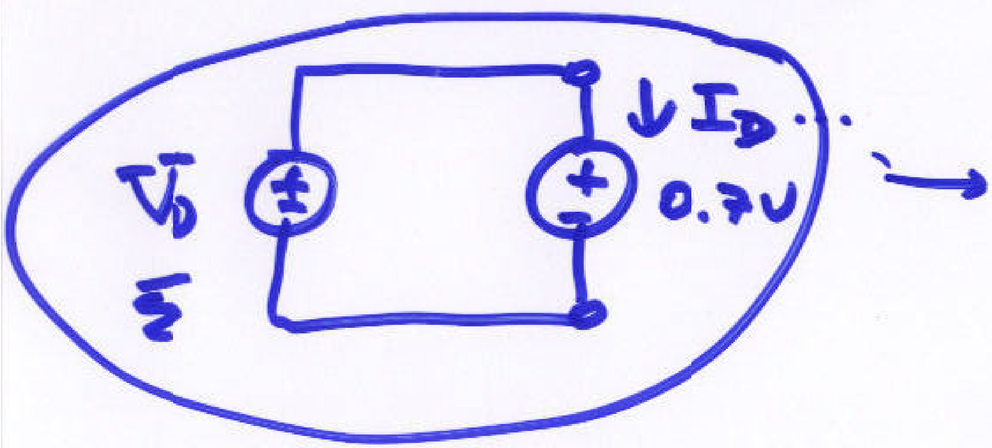
CRUDE DC/LARGE SIGNAL MODEL

OFF $\begin{cases} V_D < 0.7V \Rightarrow \\ V_D > V_{BD}\ (-19.5V) \end{cases}$ $I_D \approx 0A \Rightarrow$

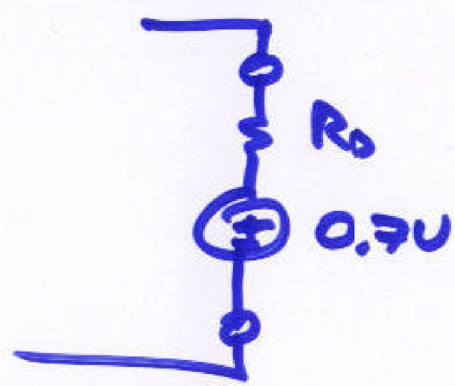


$V_D \gtrsim 0.7$ (ON)

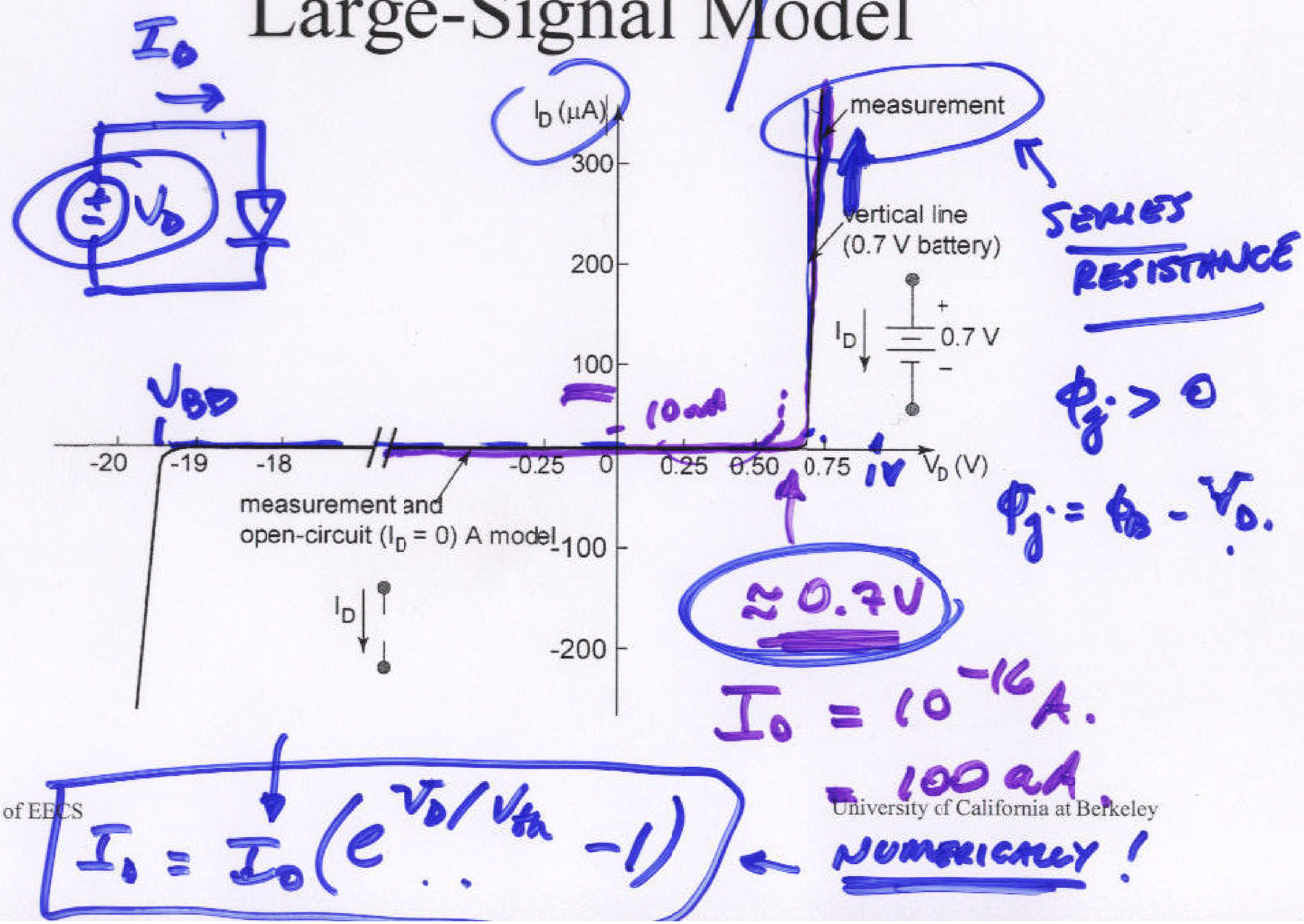
... VERTICAL LINE



"OIT" BETTER



Large-Signal Model



Small-Signal Model: r_d

Forward-bias assumed → $V_D = 0.7$ V (approx)

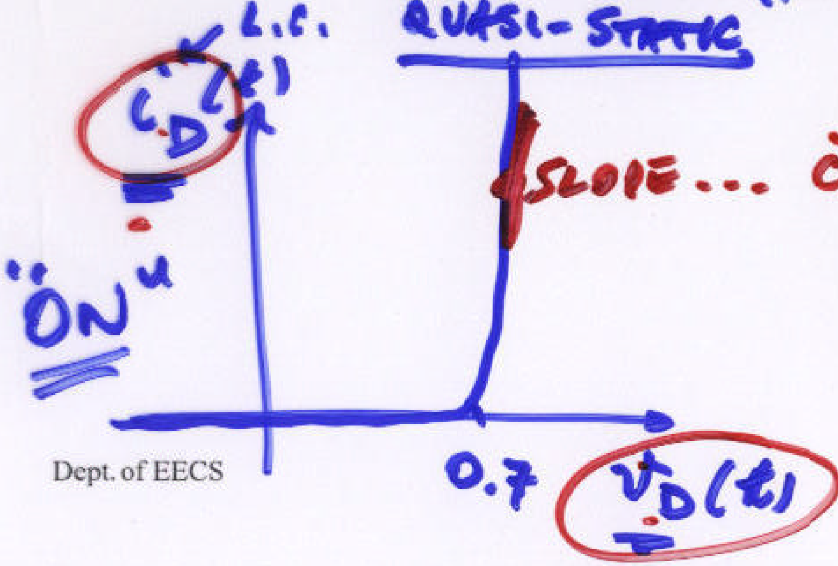
$$i_D(t) = I_O(e^{v_D(t)/V_{th}} - 1) \cong I_O e^{v_D(t)/V_{th}}$$

Substitute $v_D(t) = V_D + v_d(t)$:

ANALOG SPECIAL CASE

DROPPED −1

$i_D(t) = I_O e^{[V_D + v_d(t)]/V_{th}}$



r_d

$e^{0.7/0.026}$ = HUGE!!

$10^{0.7/0.06} = 10^{0.72/0.06} \approx 10^{12}$

$i_D(t) = I_O e^{[V_D + v_d]/V_{th}}$

$\frac{1}{20} = 0.05 = \frac{v_d}{2V_{th}} = \frac{v_d}{50\,mV}$

$v_d = \frac{50\,mV}{20} = 2.5\,mV$

Power Series Expansion

$$e^x = 1 + x + \frac{1}{2!}x^2 + \frac{1}{3!}x^3 + \ldots$$

x … SMALL

- Can quantify the limit of the linear approximation

$$e^x = 1 + \left(\frac{v_d}{V_{th}}\right) + \frac{1}{2}\left(\frac{v_d}{V_{th}}\right)^2 + \frac{1}{6}\left(\frac{v_d}{V_{th}}\right)^3$$

RATIO

5%:

$$\frac{\frac{1}{2}\left(\frac{v_d}{V_{th}}\right)^2}{\left(v_d/V_{th}\right)} = \text{error} = \frac{v_d}{2V_{th}}$$

$$i_D(t) = I_O e^{V_D/V_{th}} e^{v_d(t)/V_{th}} = I_D e^{v_d(t)/V_{th}}$$

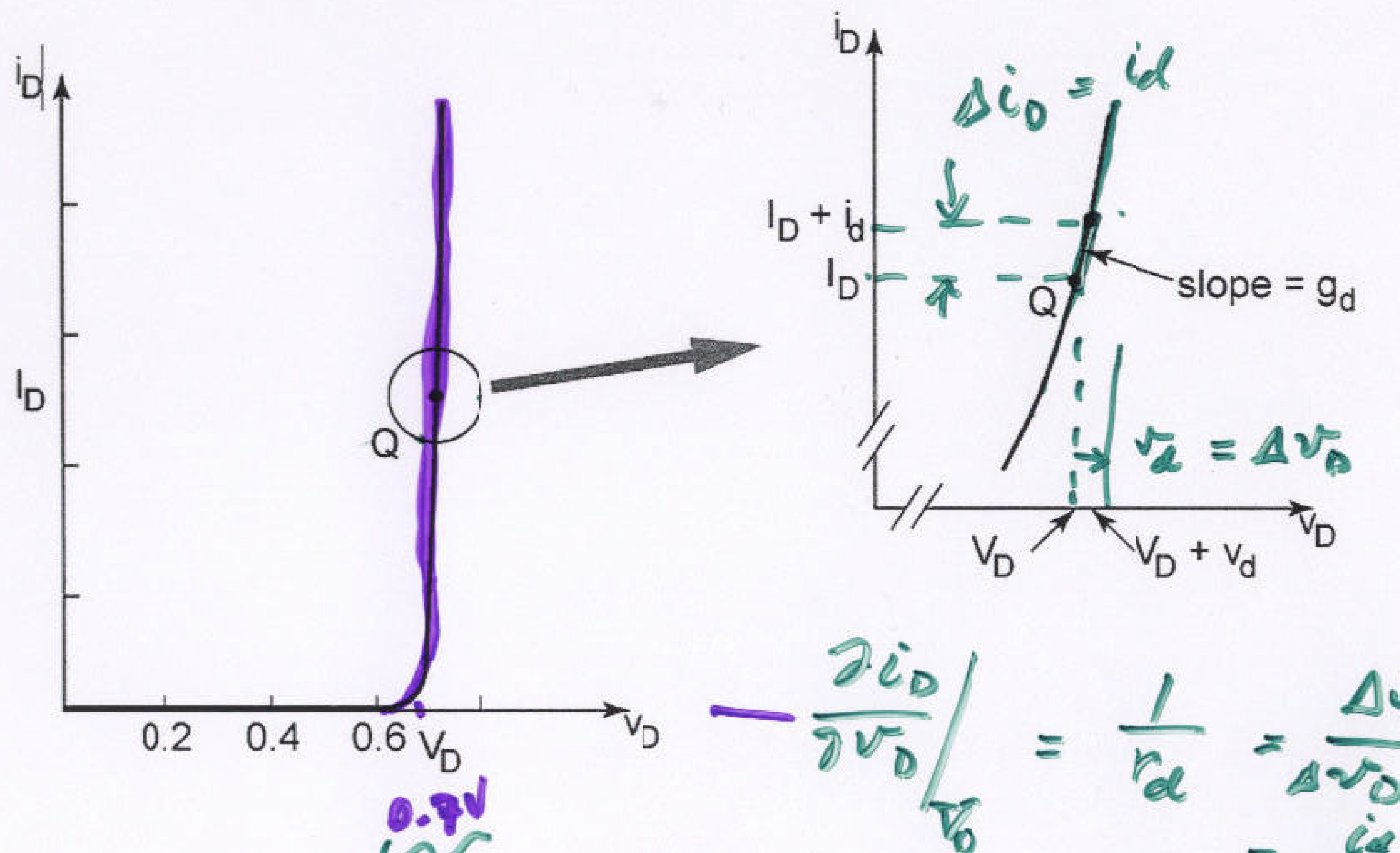
$\cong I_D$ ← D.C.

$= I_D e^x$

→ SMALL RESISTOR!

NOT QUITE ZERO.

Graphical Interpretation



$$\left.\frac{\partial i_D}{\partial v_D}\right|_{V_D} = \frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_D} = \frac{i_d}{v_d}$$

$$i_D = I_D e^{v_d/V_{th}} \cong I_D\left[1 + \frac{v_d}{V_{th}}\right].$$

$$i_D = I_D + \left(\frac{I_D}{V_{th}}\right) v_d$$

$$i_D = I_D + i_d$$

$$i_d = \left(\frac{I_D}{V_{th}}\right) v_d$$

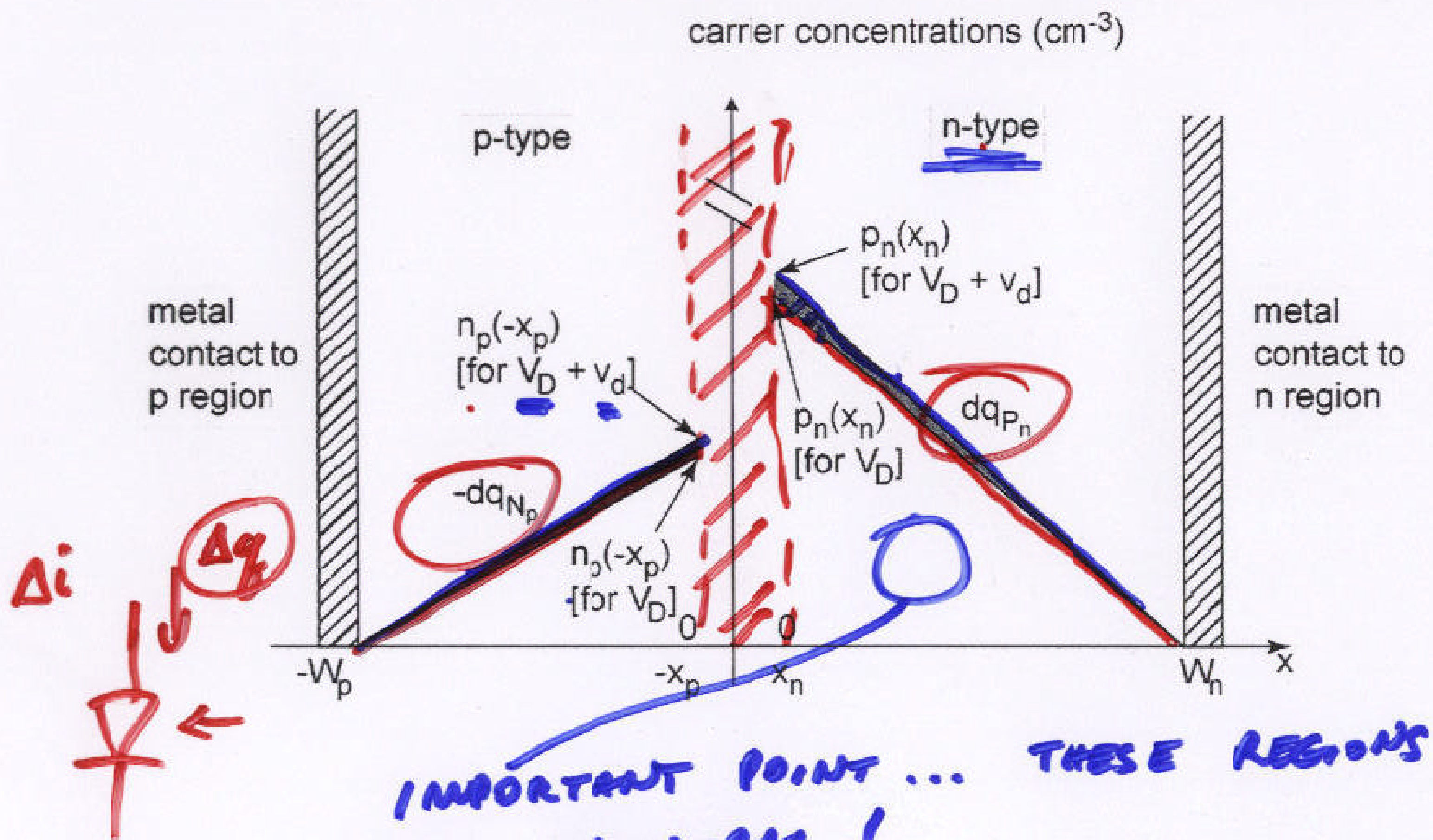
$$r_d = \frac{V_{th}}{I_D}$$

~~NOT $= \frac{V_D}{I_D}$~~

$$r_d = \frac{26\,mV}{100\,\mu A} = 260\,\Omega$$

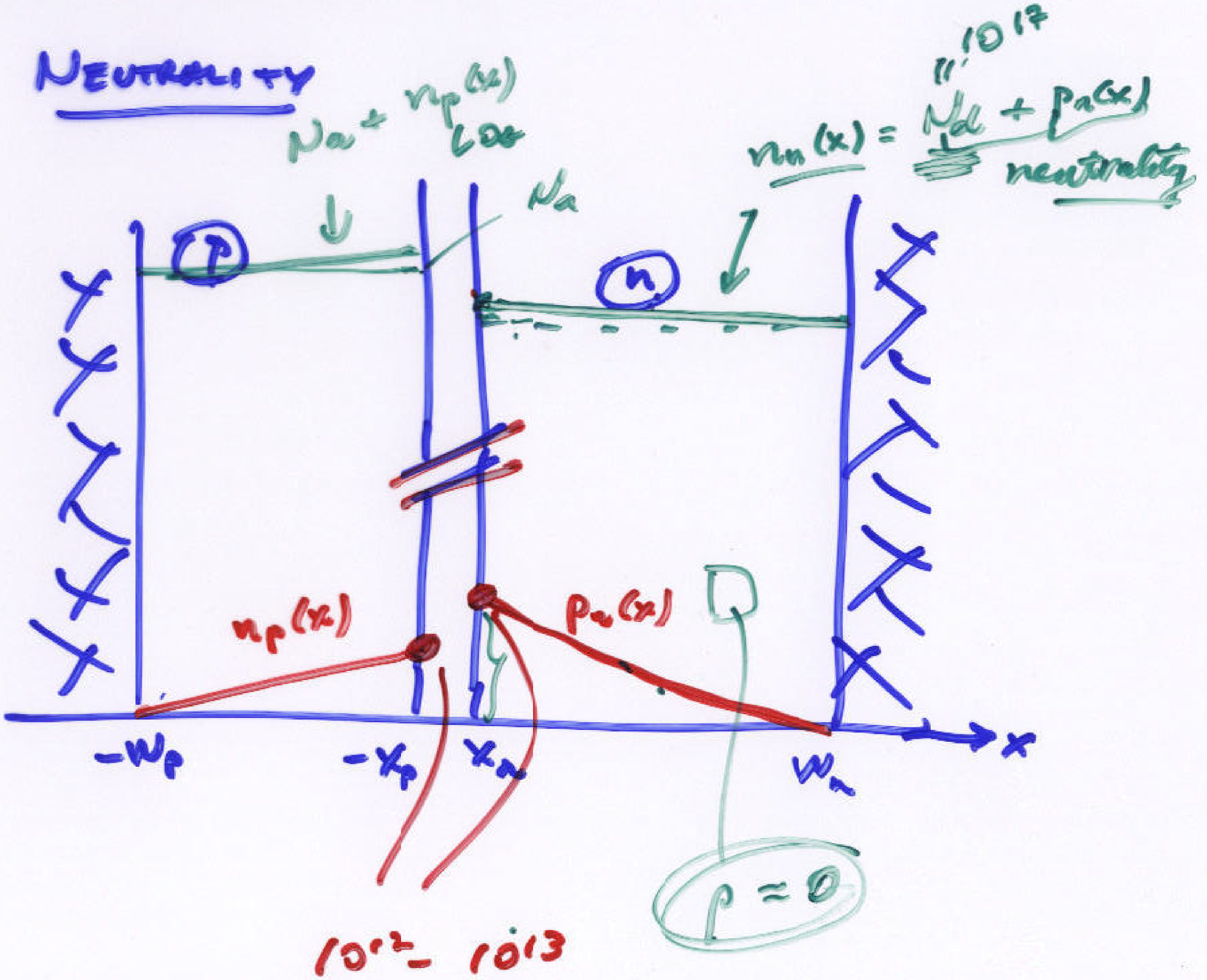
WEIRD!

Physics of Diffusion Capacitance



IMPORTANT POINT ... THESE REGIONS ARE NEUTRAL!

NEUTRALITY

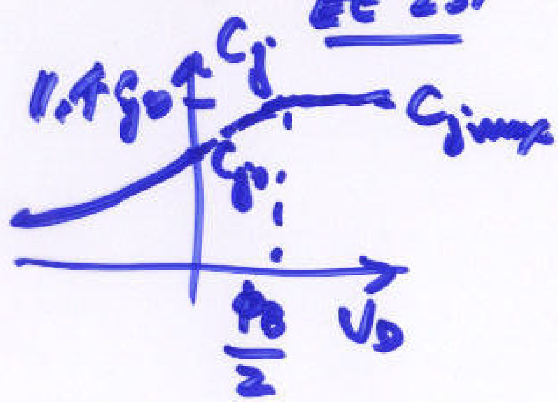


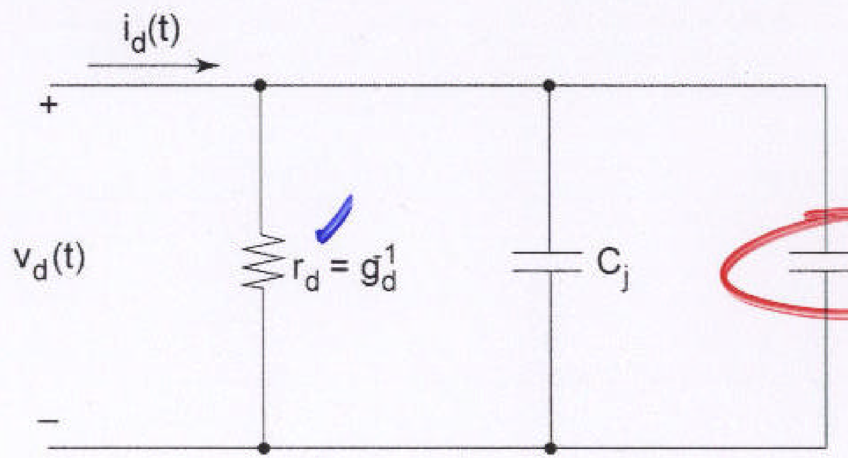
$N_a + n_p(x)$
Low
N_a
$n_n(x) = N_d + p_n(x)$
$\approx 10^{17}$
neutrality
p
n
$n_p(x)$
$p_n(x)$
$-W_p$
$-x_p$
x_n
W_n
x
$10^{12} - 10^{13}$
$\rho \approx 0$

Diffusion Capacitance

Depletion region narrows under forward bias, increasing capacitance to $C_j = 1.4\ C_{jo}$

Dominant capacitance is from storage of minority carriers in the diode's p and n regions: the *diffusion* capacitance





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Diffusion Capacitance

Minority carrier charge storage is proportional to the DC diode current:

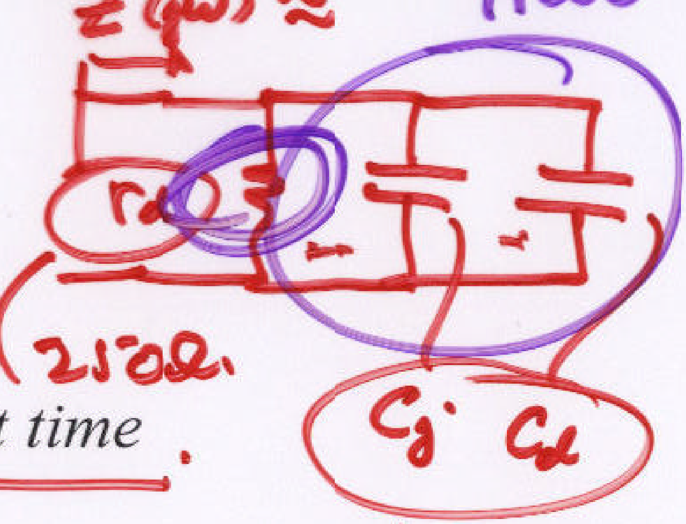
$$C_d = \left(\frac{I_D}{V_{th}}\right)\tau_T = g_d \tau_T$$

where τ_T is the diode's *transit time*.

SEE CHAP. 6 (SEE EE 130)

$\lesssim 1ps$

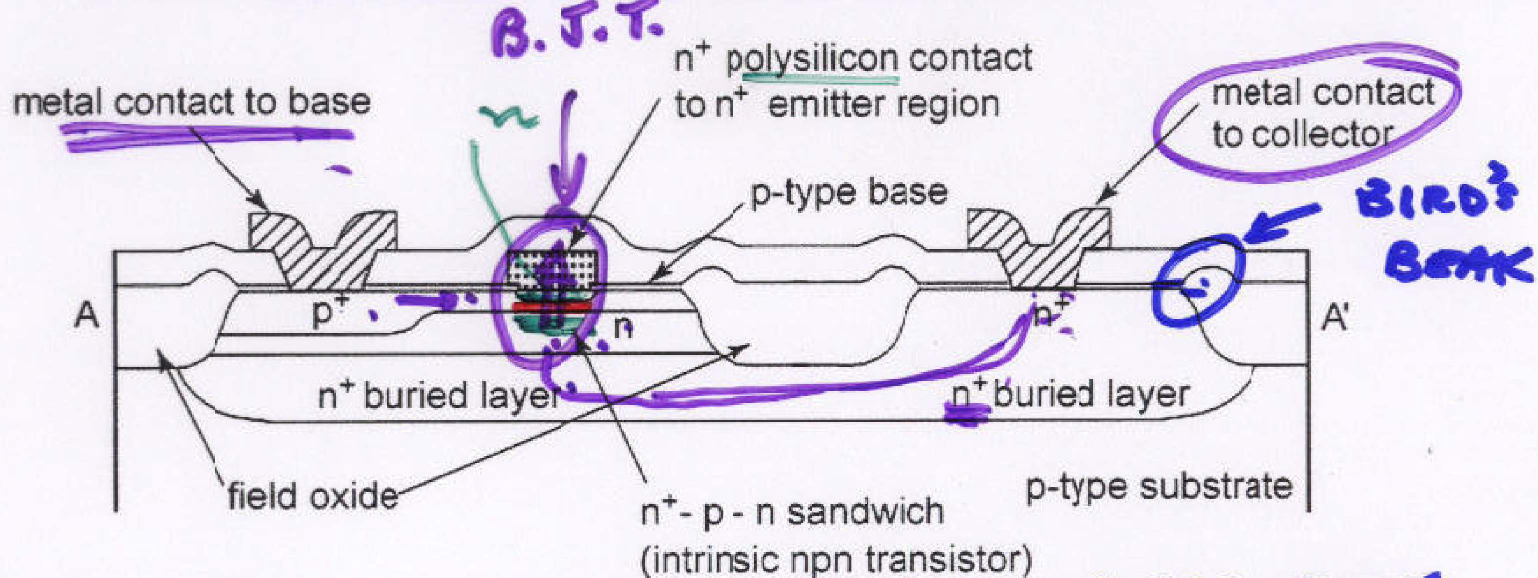
$Z(j\omega) \approx$ HUGE Z !!



$C_j + C_d = 50 fF$.

BUT C_d IS BIG! (RELATIVE TO C_j)

npn Bipolar Transistor Structure



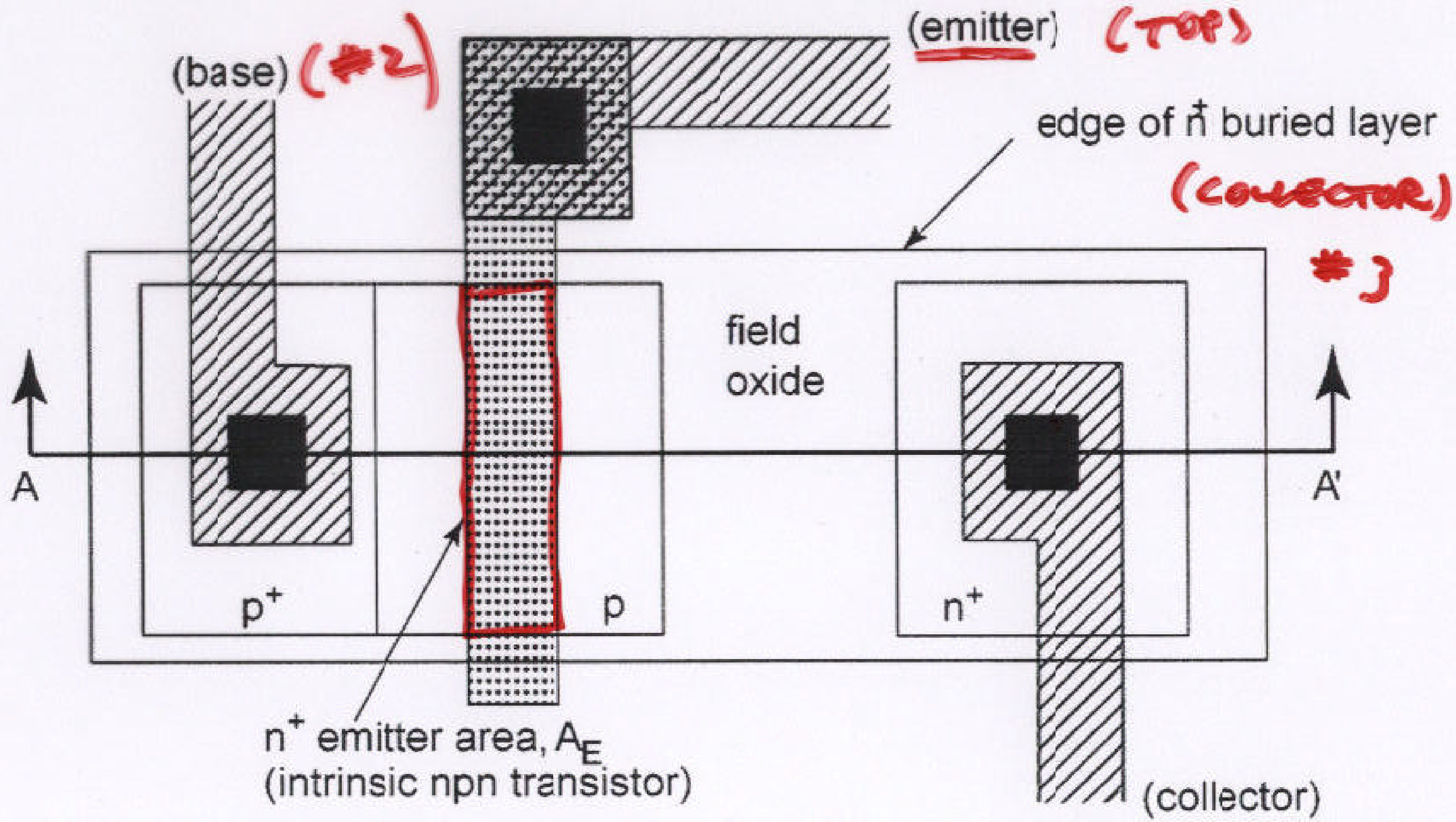
CIRCA 1992 (MICROLINEAR LAB CHIP)

CIRCA 2002 ← CIRCA 2005 B.J.T. ...

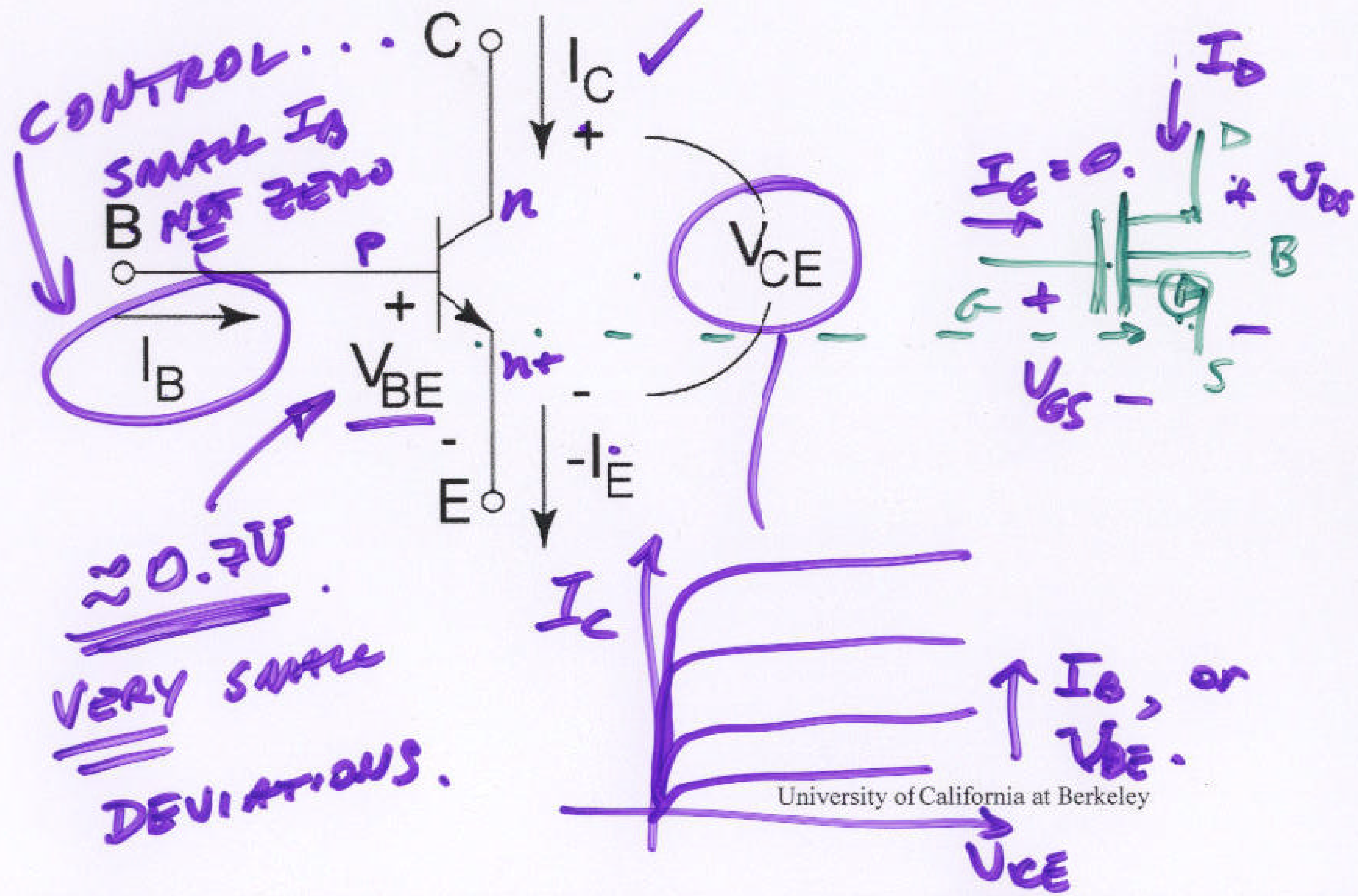
SiGe (NOT Si) + CMOS.

IBM. (npn only)

npn Bipolar Transistor Layout

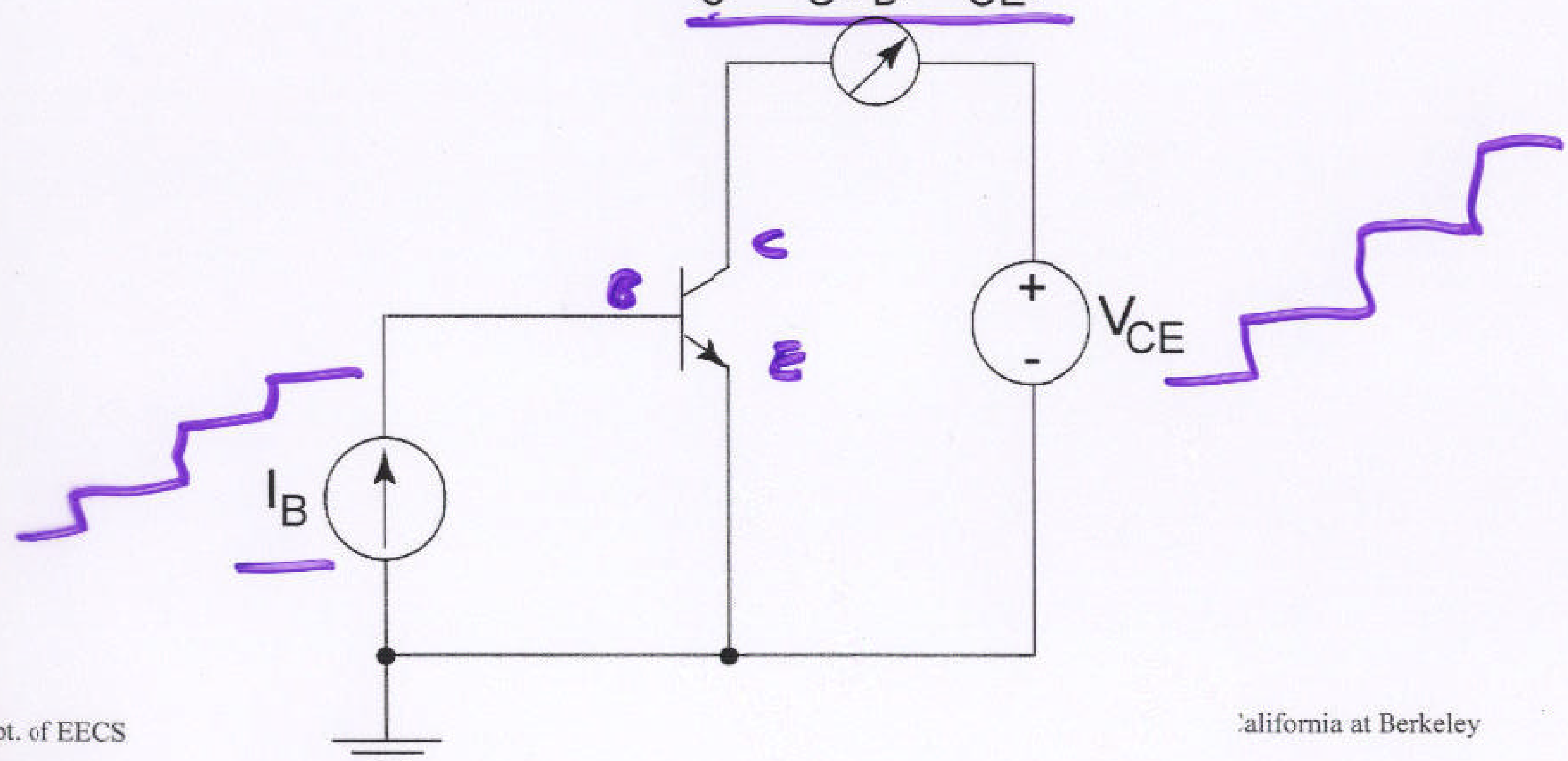


BJT Symbol



Measuring the BJT's Collector Characteristics

$I_C = I_C(I_B, V_{CE})$



Collector Characteristics