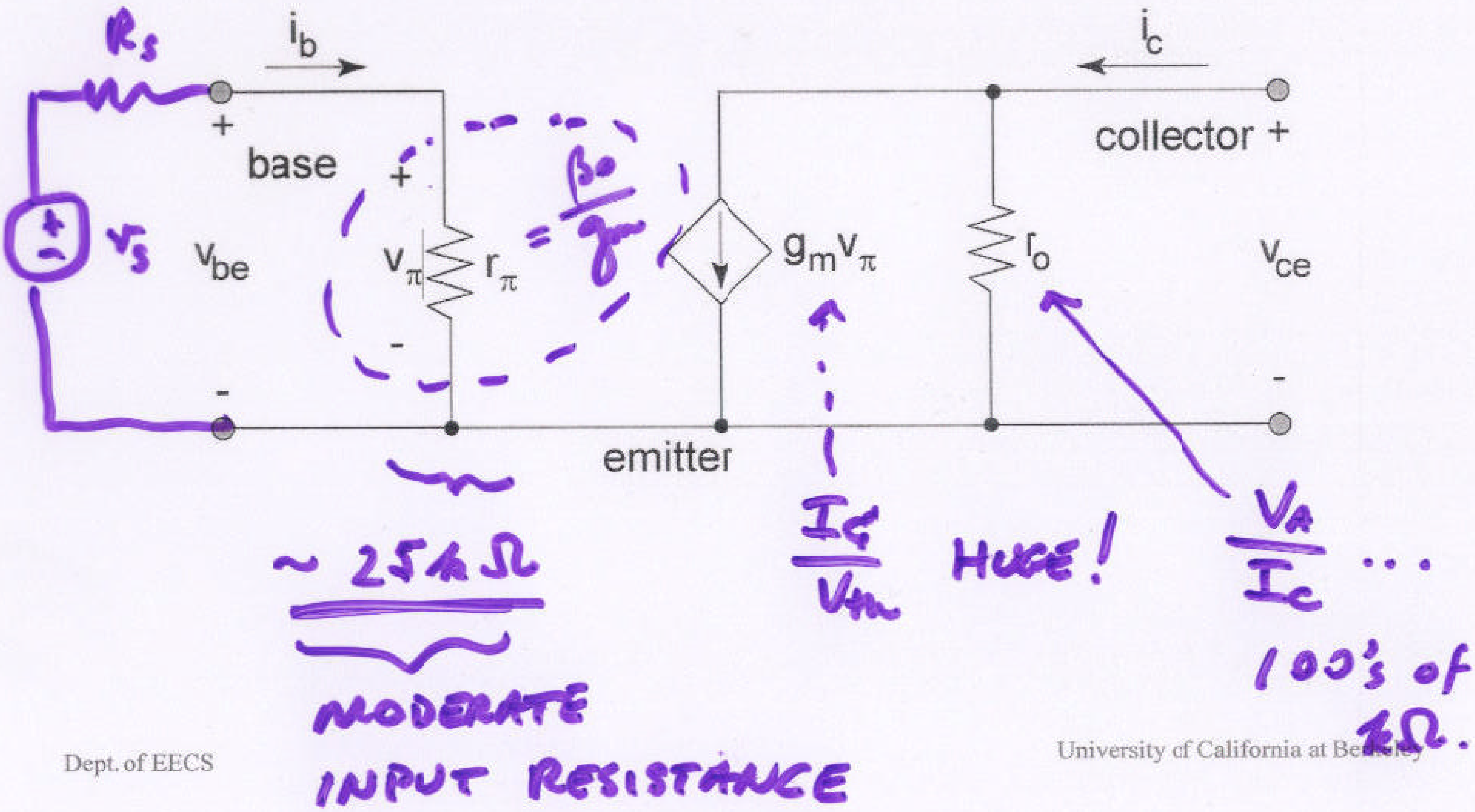
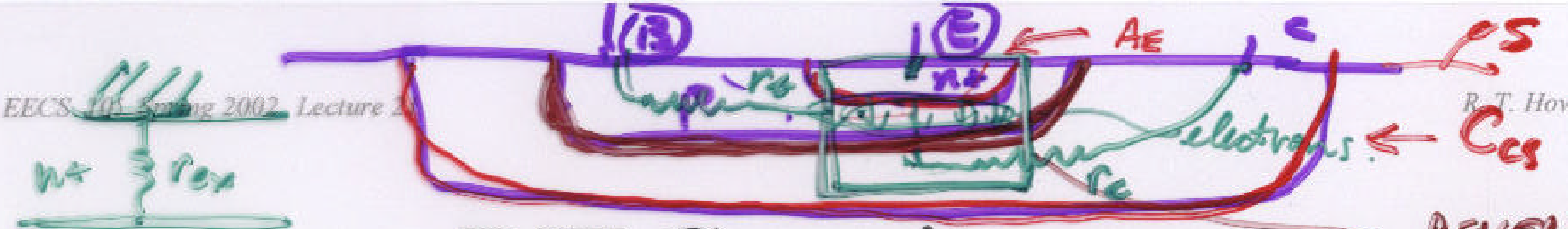
 R. T. Howe

Lecture 22

- Last time: FINISH HYBRID – π. (B.J.T.)
  - Small-signal model of the npn bipolar transistor
- Today: START CHAPTER 8!
  - Introduction to amplifiers: a common-source MOS single-stage amplifier

BJT Small-Signal Model

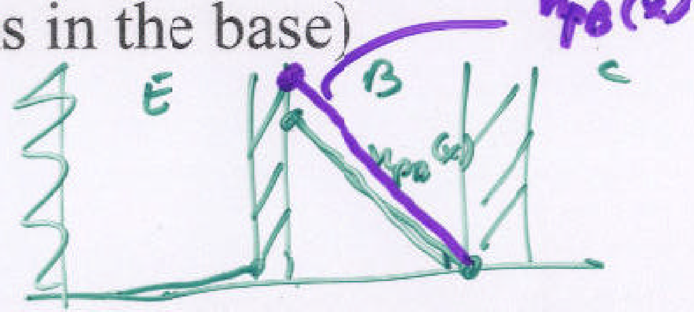




BJT Capacitances

- Base-charging capacitance C_b: due to minority carrier charge storage (mostly electrons in the base)

$$C_b = g_m \tau_F$$

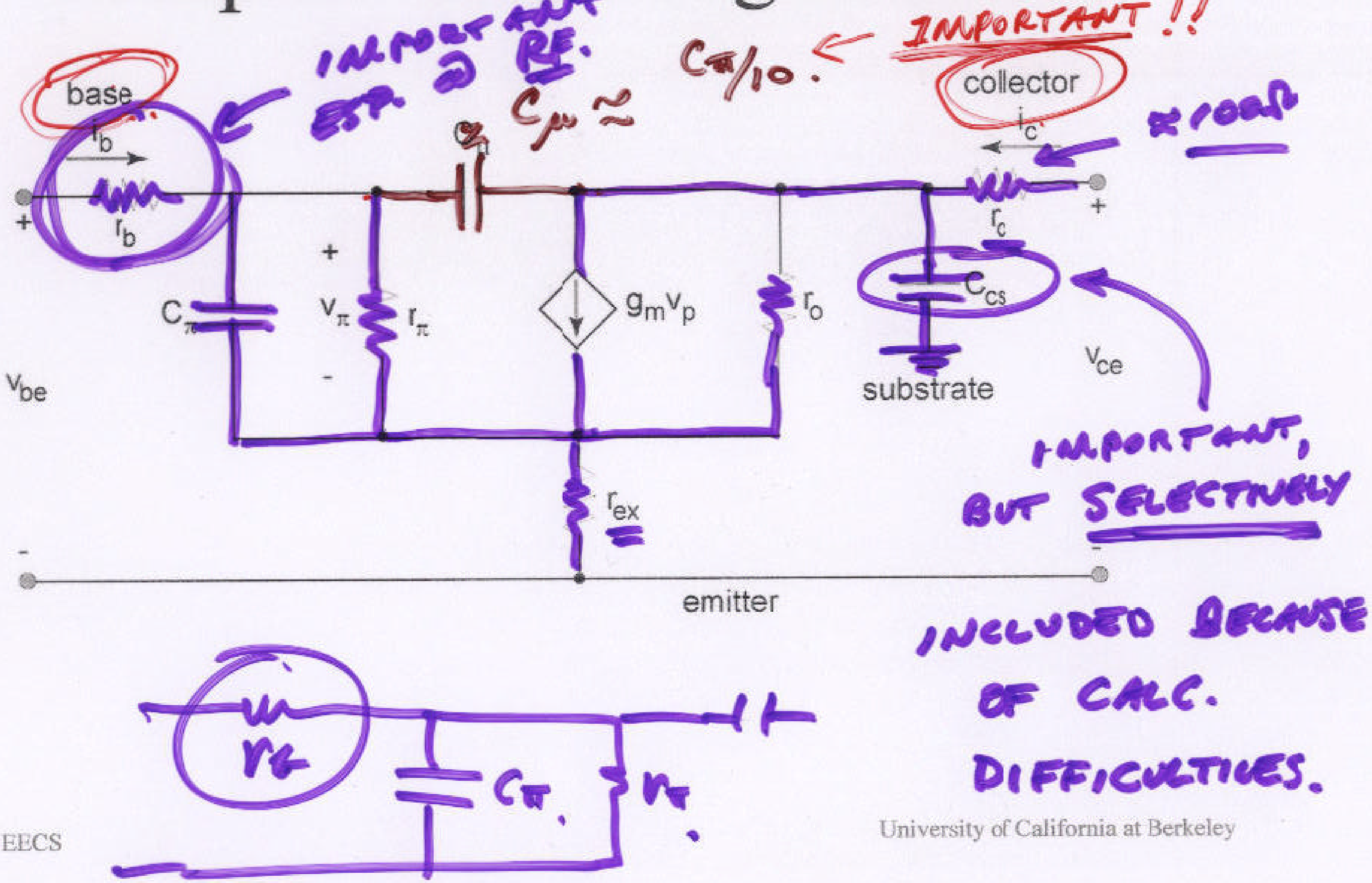


- Base-emitter depletion capacitance: $C_{jE} = 1.4\, C_{jEo}$

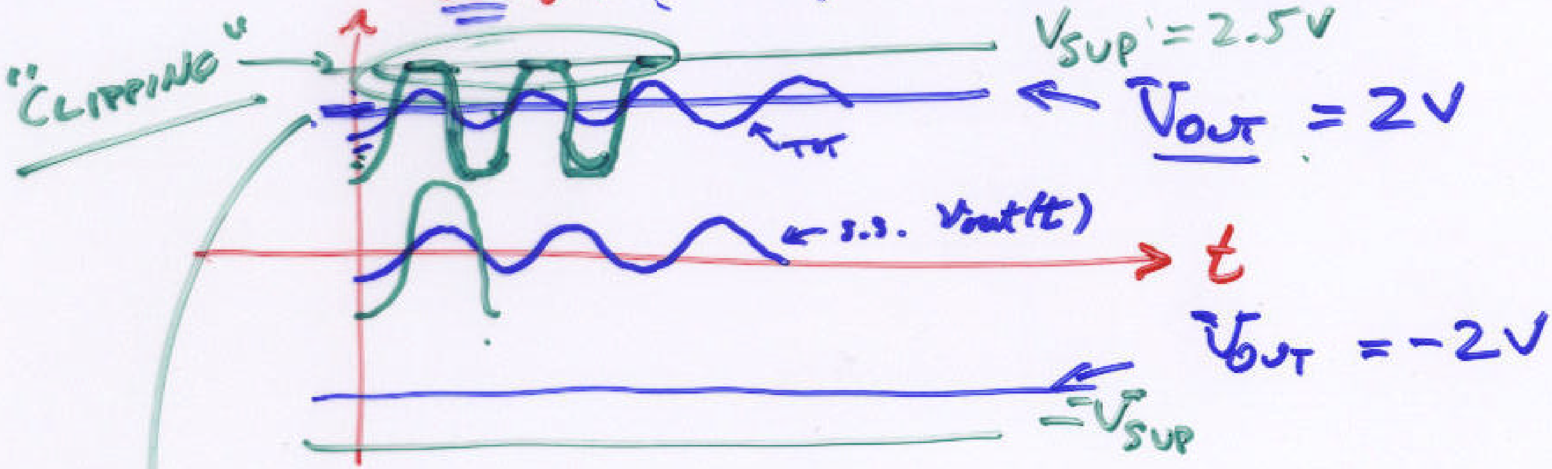
Total B-E capacitance: $C_\pi = C_{jE} + C_b$

$$C_{bc} = C_\mu = \frac{C_{j\mu o} \cdot A_{BC}}{\sqrt{1 - V_{BC}/\phi_{BC}}}$$

Complete Small-Signal Model

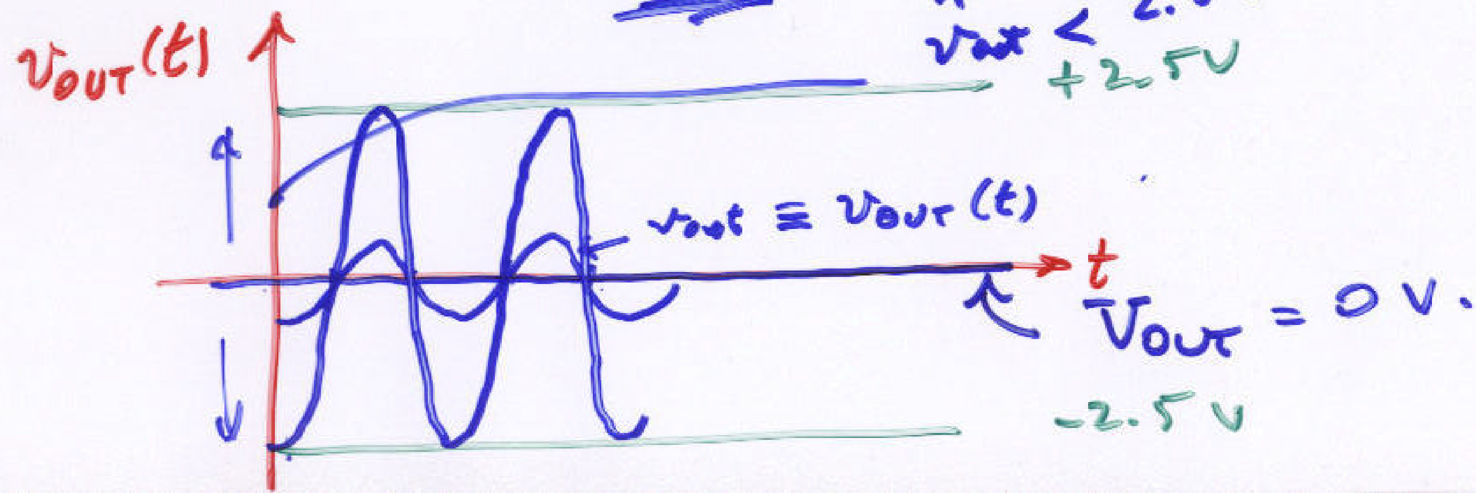


$v_{OUT}(t)$ (TOTAL) = $V_{OUT} + v_{out}(t)$



$v_{out}(t) = \hat{v}_{out} \cos \omega t.$

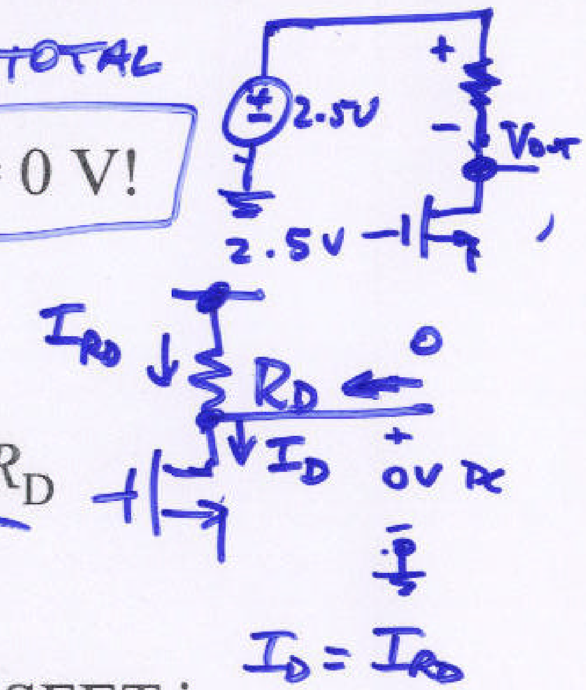
$< 0.5V.$



Selecting the Output Bias Point

V_{BIAS} is selected so that V_{OUT} is centered between $+V_{SUP}$ and $-V_{SUP}$ (why?)

$V_{OUT} = 0$ V ... **NOT** $v_{OUT} = 0$ V!



Constraint on the DC drain current:

$I_{RD} = (V_{SUP} - V_{OUT}) / R_D = V_{SUP} / R_D$

$I_{RD} = I_D = I_{D,SAT}$ ... verify that MOSFET is saturated after finding V_{BIAS}

Finding the Input Bias Voltage

- Hand calculation: neglect "fudge factor" in $I_{D,SAT}$.

$$I_{D,SAT} = (W/2L)\mu_n C_{ox}(V_{GS} - V_{Tn})^2$$

Typical numbers: $W = 40\ \mu m$, $L = 2\ \mu m$, $R_D = 25\ k\Omega$, $\mu_n C_{ox} = 100\ \mu A/V^2$, $V_{Tn} = 1\ V$, $V_{SUP} = 2.5\ V$

$$I_{RD} = \frac{V_{SUP}}{R_D} = I_{D,SAT} = 10 \cdot 100 \cdot (V_{GS} - 1)^2$$

CHAPTER 8.

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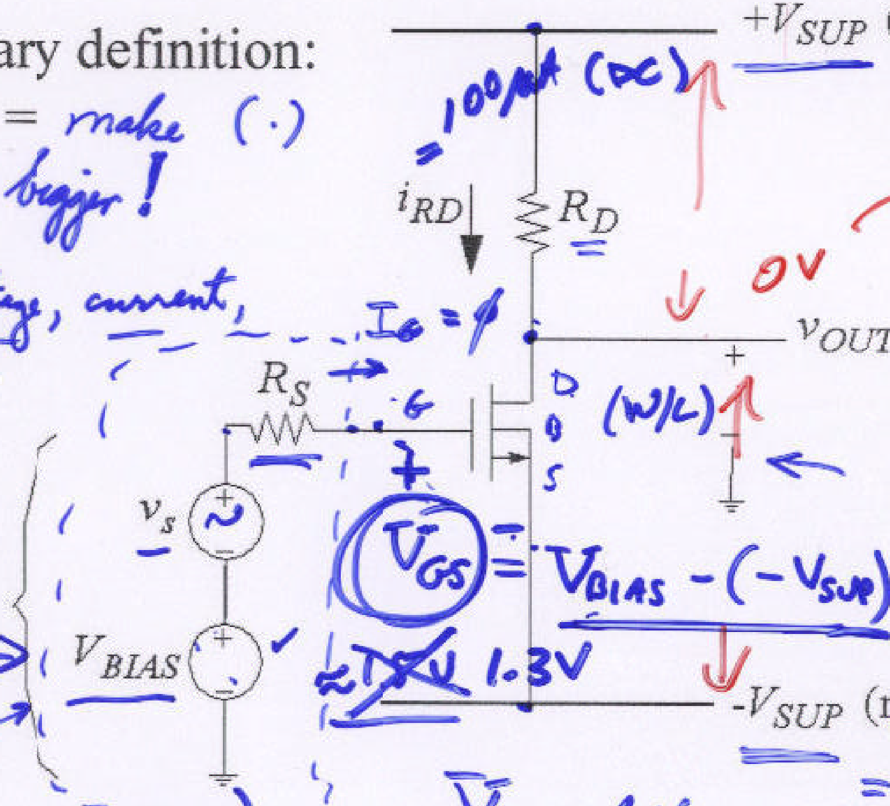
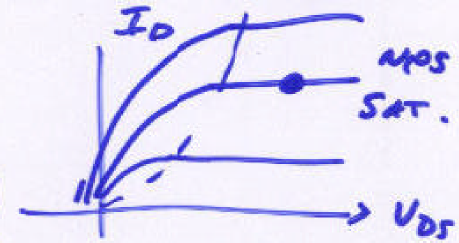
An MOS Amplifier

Dictionary definition:

amplify = make (·) bigger!

(·) = voltage, current, power.





VOLTS

$V_{TH} = 1V$.

CONSIDER v_s DISCONNECTED FOR SETTING (V_{OUT}, V_{BIAS})

$V_{GS} = V_{BIAS} - (-V_{SUP})$

$V_{BIAS} = 1.3 - 2.5$

Applying the Small-Signal Voltage

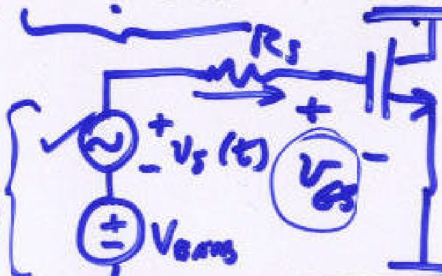
→ HARD WAY.

Approach 1. Just use v_{IN} in the equation for the total drain current i_D and find v_{OUT}

$v_{IN}(t) = V_{BIAS} + v_s(t)$

$v_{IN} = V_{BIAS} + v_s$ $v_{GS} = v_{IN} - (-V_{SUP}) = [V_{BIAS} + v_s + V_{SUP}]$

$v_s(t) = \hat{v}_s \cos(\omega t)$

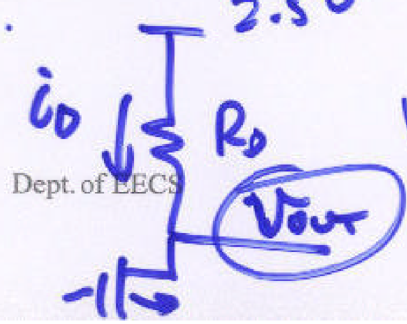


crude... neglect $i_g \cdot R_S$ drops... low ω.

Result:

TOTAL

$v_{OUT} = V_{SUP} - R_D i_D \cong V_{SUP} - R_D(\mu_n C_{ox})\left(\frac{W}{2L}\right)(V_{GS} + v_s - V_{Tn})^2$



$V_{GS} = V_{BIAS} + V_{SUP}$

$-(-V_{SUP})$

$(V_{GS} + v_s - V_{Tn})^2 = (V_{GS} - V_{Tn})^2 \left(1 + \frac{v_s}{V_{GS} - V_{Tn}}\right)^2$

Solving for the Output Voltage v_{OUT}

(PULL OUT TERM WITH BIAS V_{GS}.)

$$v_{OUT} = V_{SUP} - R_D(\mu_n C_{ox})\left(\frac{W}{2L}\right)(V_{GS} - V_{Tn})^2\left(1 + \frac{v_s}{(V_{GS} - V_{Tn})}\right)^2$$

I_D

$$v_{OUT} = V_{SUP} - R_D I_D\left(1 + \frac{v_s}{(V_{GS} - V_{Tn})}\right)^2$$

V_{SUP} = 2.5V; $R_D I_D$ = V_{SUP} = 2.5V.

$(V_{GS} - V_{Tn}) = (1.3 - 1) = 0.3V$

$v_s = 0$ ... DC

$v_{OUT} = 0V = V_{OUT}$

$v_{OUT}(t) = 2.5 - 2.5\left(1 + \frac{v_s}{0.3}\right)^2$

Small-Signal Case

Linearize the output voltage for the s.s. case

$v_s / (V_{GS} - V_{Tn})$

Expand $(1 + x)^2 = 1 + 2x + x^2$ … last term can be dropped when $x << 1$

$v_s << V_{GS} - V_{Tn} = 0.3V$ ASSUME

$$\left(1 + \frac{v_s}{V_{GS} - V_{Tn}}\right)^2 = 1 + \frac{2v_s}{V_{GS} - V_{Tn}} + \left(\frac{v_s}{V_{GS} - V_{Tn}}\right)^2$$