

DEVICES ✓

## Lecture 23

## • Last time:

- Introduction to amplifiers: a common-source MOS stage HARD WAY!

$$v_{in} = v_{sig} + v_f(t)$$

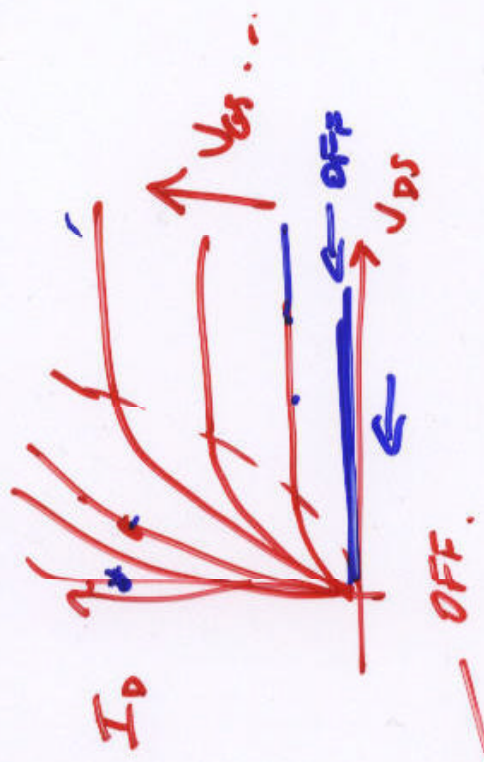
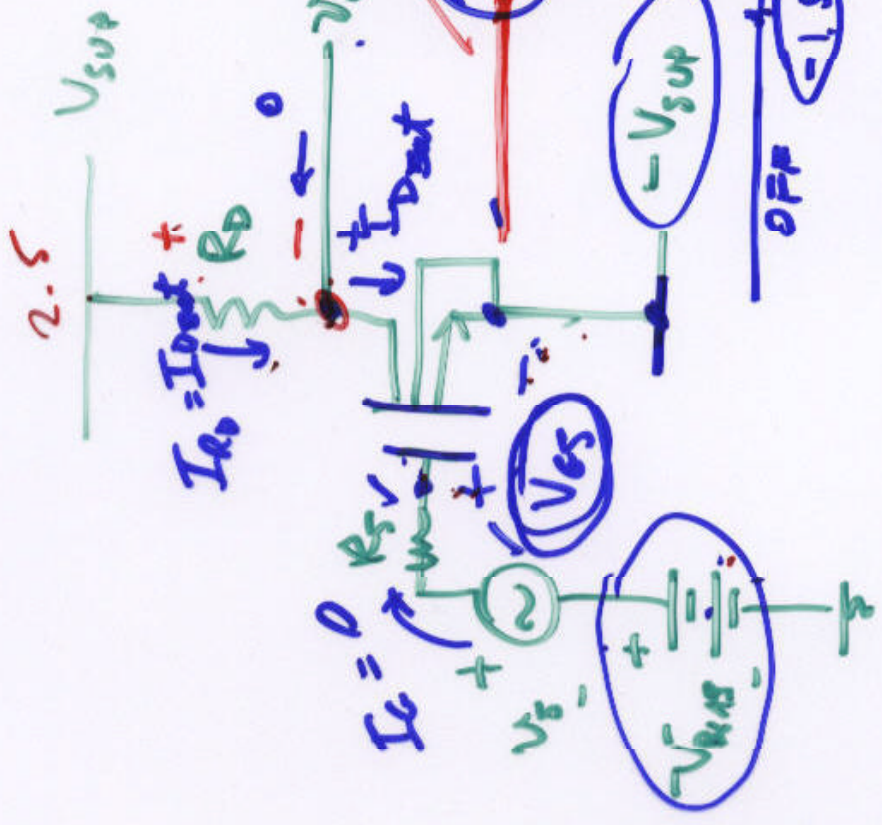
$$v_{out} = v_{out} + v_{sig}(t)$$

↙

## • Today :

- Small-signal model for the entire common-source amplifier
- Limits to model:

EASY WAY.



$V_{DS} \downarrow \dots$   
 FAIC TEST

$V_{DS} > V_{GS} - V_{TH}$   
 $\uparrow$

$V_{BIAS} = V_{GS} - 2.5V$

$V_{B,43} (ON) =$

$V_{TH} - 2.5V =$

$1 - 2.5V = -1.5V$

-2.5V

$V_{GS} = V_{B,43} - (-V_{SUP})$

$= V_{B,43} + 2.5V$

$1.3V$

$V_{OUT}$   
 $V_{SUP}$

NOIS SAT.

NOIS TRIODE

$f = -V_{OUT}$

-1.2V

-1.5V

OFF

# Linearized Output Voltage

For this case, the total output voltage is

$$v_{OUT} \approx \underbrace{V_{SUP}}_{V_{SUP}} - \underbrace{R_D I_D}_{V_{SUP}} \left( 1 + \frac{2v_s}{(V_{GS} - V_{Tn})} \right) = \cancel{V_{SUP}} - \cancel{V_{SUP}} - \frac{2R_D I_D v_s}{(V_{GS} - V_{Tn})}$$

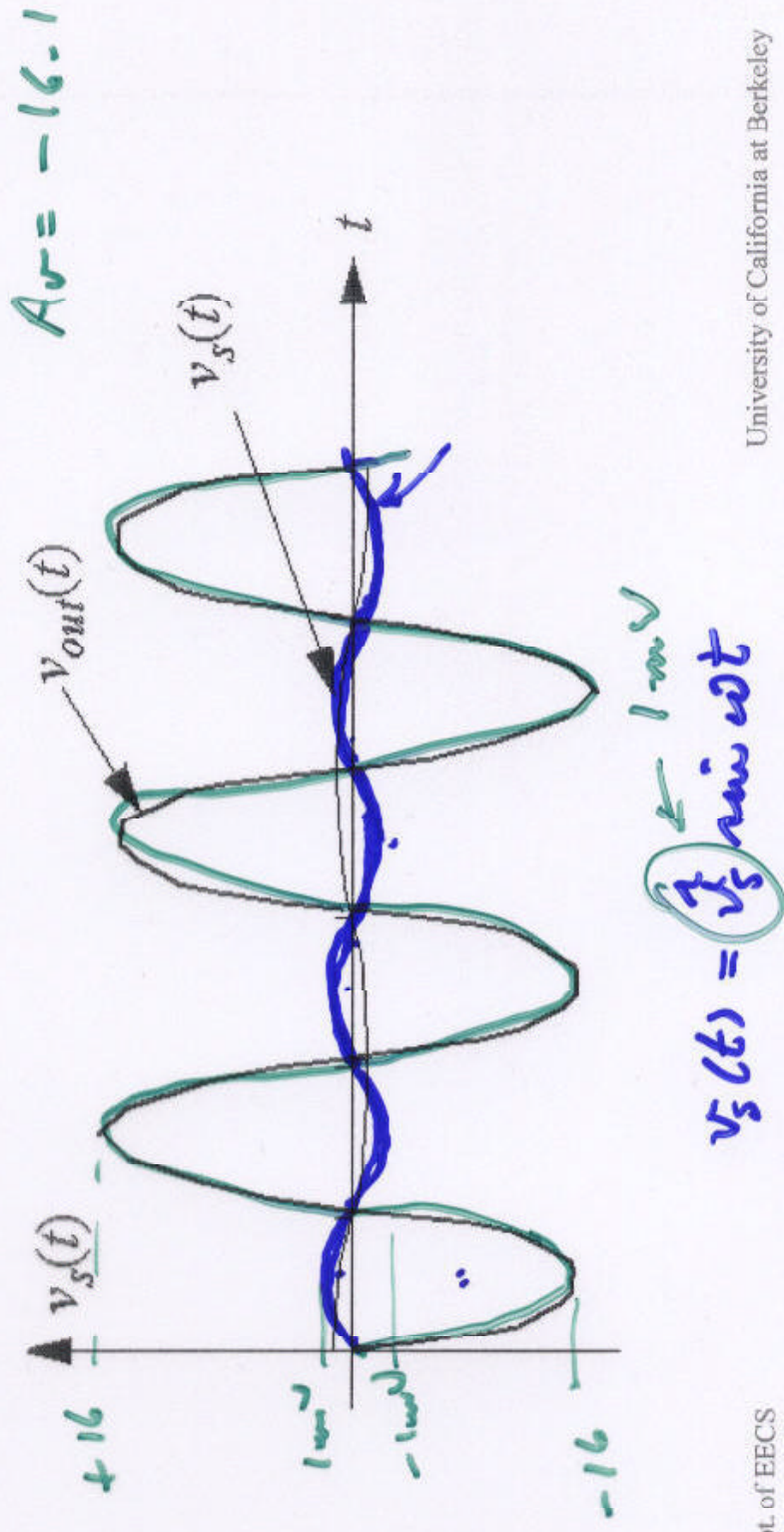
The average output voltage  $V_{OUT} = 0$  V so the total output voltage is the small-signal voltage in this special case:

$$v_{OUT} = \underbrace{v_{out}}_{+V_{out}} = - \left[ \frac{2R_D I_D}{(V_{GS} - V_{Tn})} \right] v_s = \boxed{- \left[ \frac{2V_{SUP}}{(V_{GS} - V_{Tn})} \right]} v_s = A_v v_s$$

$A_v = \text{voltage gain}$   
 $\approx - \frac{2(2.5V)}{(0.3V)} \approx -15$

# Plot of Output Waveform

$$\text{Numbers: } 2 I_D R_D / (V_{GS} - V_{Th}) = (2 \times 2.5) / 0.31 = 16.1$$



# Is there a Better Way?

→ What's missing: ✓ no inclusion of fudge factor term or of charge storage effects

**EASY WAY** → **TOO MESSY!!**

Approach 2. Do problem in two steps.  $i_{DSAT} = \dots \cdot (1 + \lambda v_{DS})$

1. DC voltages and currents (ignore small signals sources):

BIAS set bias point of the MOSFET ... we had to do this to BIAS V<sub>GS</sub>

DO NOT pick V<sub>BIAS</sub> already CAPITAL CAPM

2. Substitute the small-signal model of the MOSFET and the small-signal models of the other circuit elements ...

NEW.

c) FIND  $V_{OUT}$   
d) FIND  $v_{out}$

(c) Plot  $v_{out}(t) \leftarrow$  TOTAL

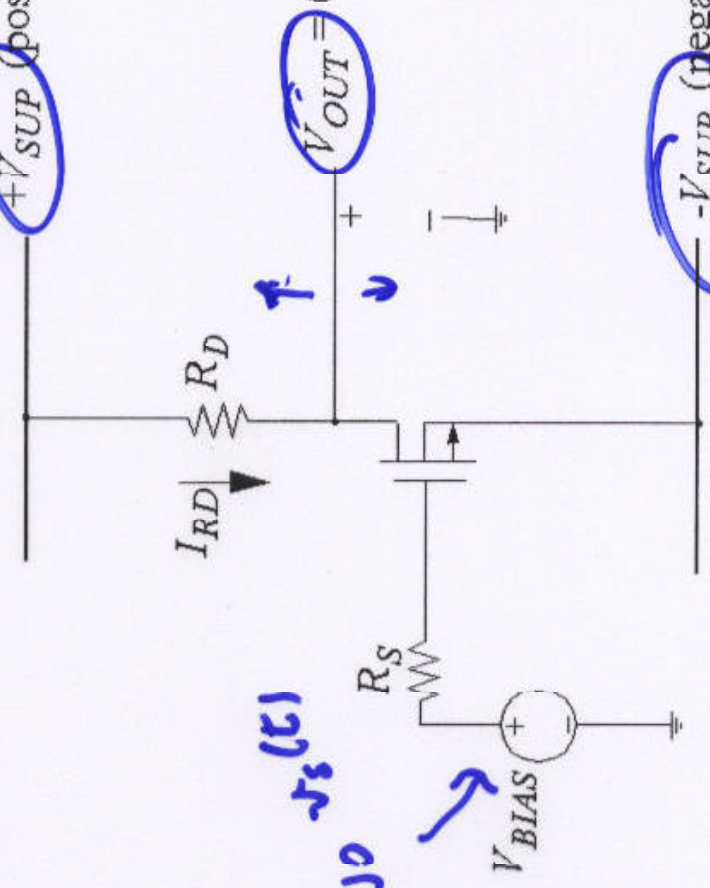
# Small-Signal Analysis

COMBINATION =  
SUM !!

Problem 1. Find DC Bias – ignore small-signal source

$V_{out} =$   
 $V_{out} + v_{out}$

$+V_{SUP}$  (positive DC supply)



could plot/sketch  
 $V_{OUT} = 0V \leftarrow V_{out}$  vs.  $V_{bias}$ .  
 $V_{BIAS}$  was found in

Lecture 22

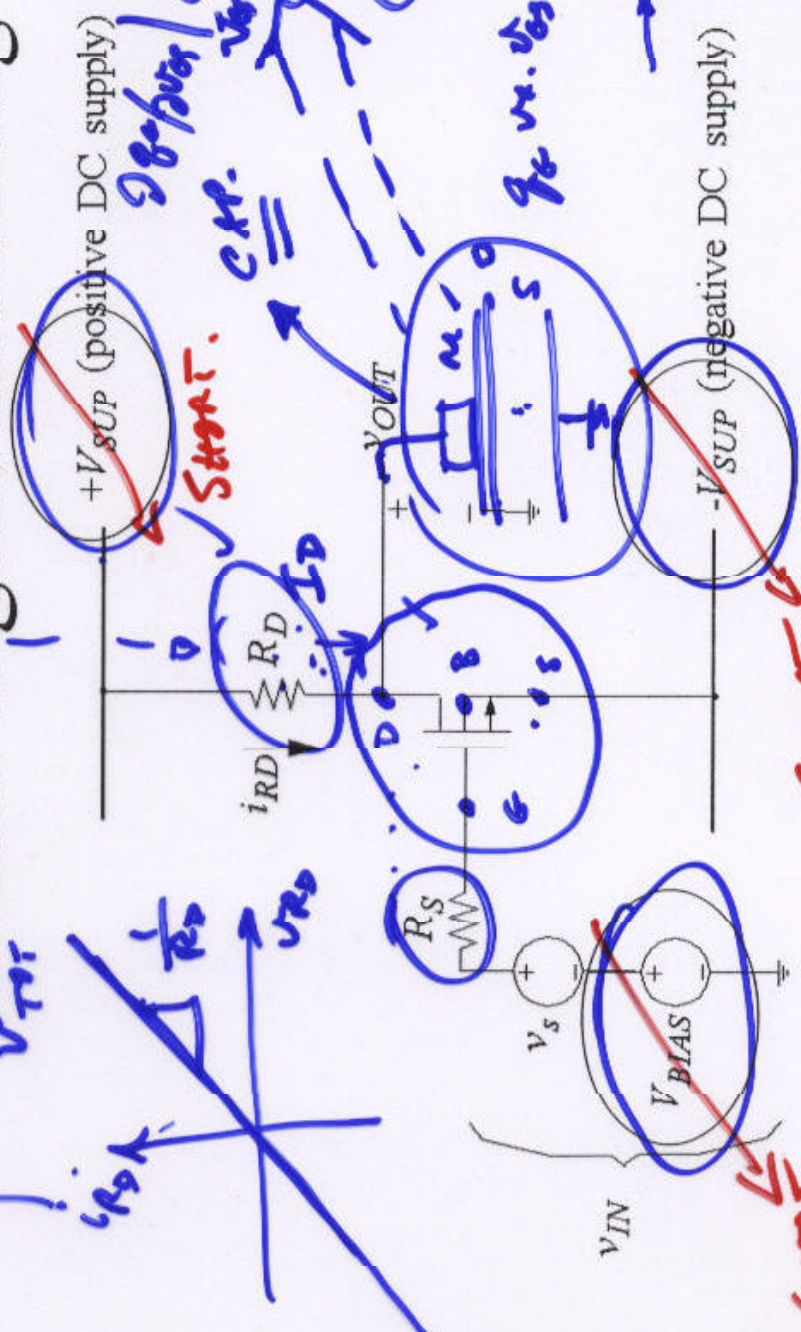
OVERKILL.

[WANT MOS SAT  
-V<sub>SUP</sub> (negative DC supply) WANT 1/2 WAY

BETWEEN LIMITS

$I_{D,SAT}$  ✓ Know  $V_{out}$ .

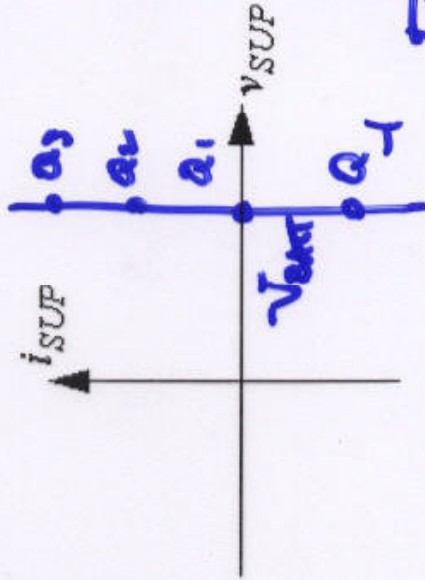
# Small-Signal Modeling



What are the small-signal models of the DC supplies?

# Small-Signal Models of Ideal Supplies

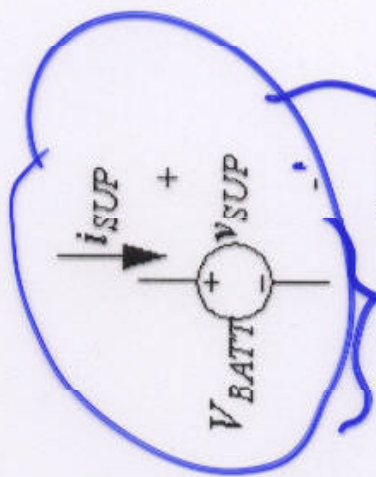
Small-signal model:



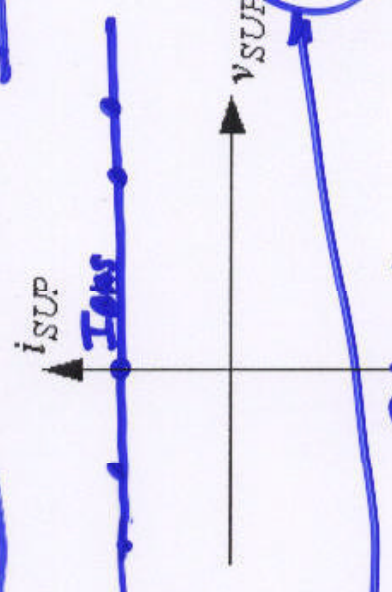
$$g_{batt} = \frac{\partial i_{SUP}}{\partial v_{SUP}} \bigg|_Q = \infty$$

$$r_{batt} = \frac{1}{g_{batt}} = 0 \Omega \quad \frac{1}{\infty}$$

Smart Circuit.

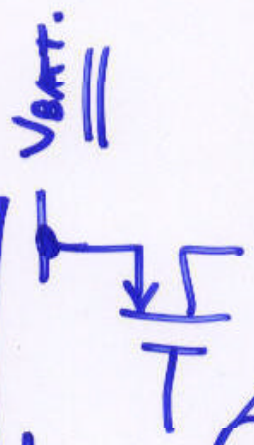
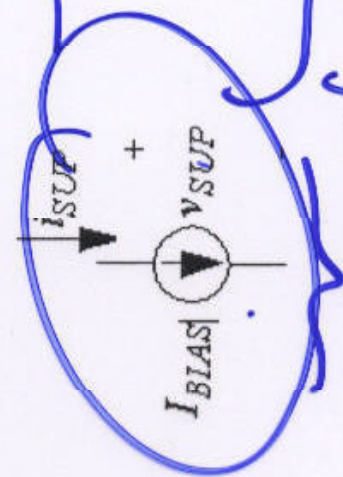


3 of these



$$g_{iSUP} = \frac{\partial i_{SUP}}{\partial v_{SUP}} \bigg|_Q = 0$$

more of these.



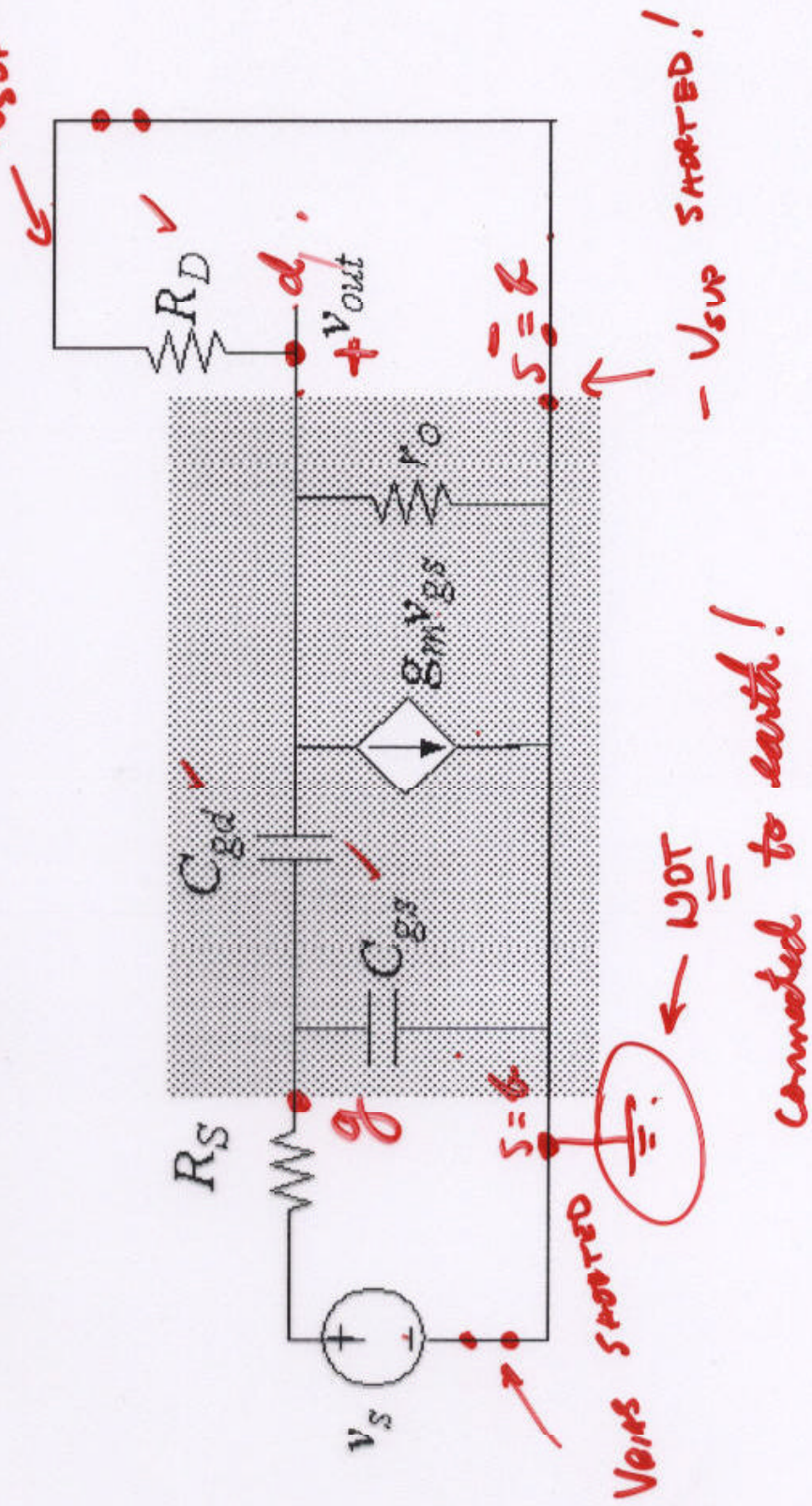
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$r_{amp} = \infty$  OPEN CRT.





# Small-Signal Circuit for Amplifier

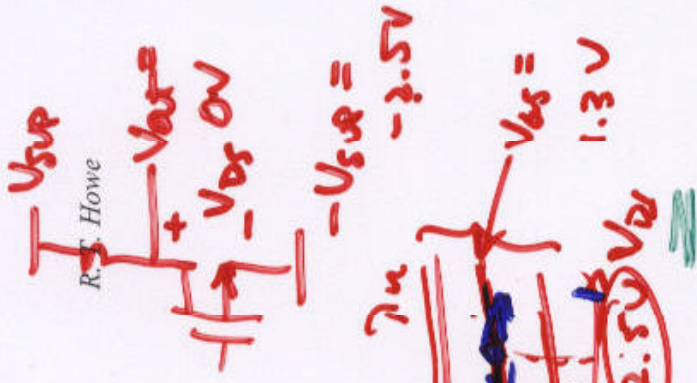


$$v_{out} = f(v_i)$$

# Voltage Gain (Cont.)

Substitute transconductance:

$$A_v = \left( -\frac{2I_{D,SAT}}{V_{GS} - V_{Tn}} \right) (R_D \parallel r_o)$$



Output resistance: typical value  $\lambda_n = 0.05 \text{ V}^{-1}$

$$r_o = \left( \frac{1}{\lambda_n I_{D,SAT}} \right) = \left( \frac{1}{0.05 \cdot 0.1} \right) (k\Omega) = 200k\Omega$$

Voltage gain:  $A_v = - \left( \frac{2 \cdot 0.1}{0.31} \right) (25 \parallel 200) = -14.3$

EECS

$$A_v = -g_m R_D$$

kΩ

mS

kΩ

EECS

## What Limits the Output Amplitude?

✓ 1.  $v_{OUT}(t)$  reaches  $V_{SUP}$  or  $-V_{SUP} \dots$  OR

2. MOSFET leaves constant-current region and enters triode region

$$V_{DS} \leq V_{DS,SAT} = V_{GS} - V_{Tn} = 0.31V$$

$$v_{OUT,MIN} = -V_{SUP} + V_{DS,SAT} = -2.5V + 0.31V$$



# Low-Frequency Voltage Gain

Consider first  $\omega \rightarrow 0$  case ... capacitors are open-circuits

$$v_{out} = -g_m v_s (R_D || r_o)$$

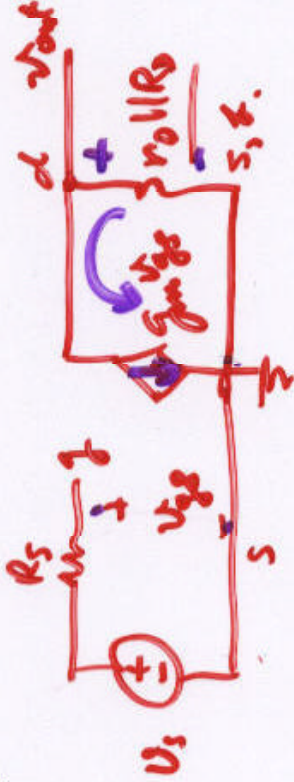
$$A_v = -g_m (R_D || r_o)$$

Transconductance

$$v_{gs} = v_s$$

$$g_m = \frac{2I_{D,SAT}}{V_{GS} - V_{Th}}$$

$$g_m = \frac{\mu_n C_{ox} (W/L)(V_{GS} - V_{Th})}{1} = \frac{\partial i_{D,SAT}}{\partial v_{gs}}$$



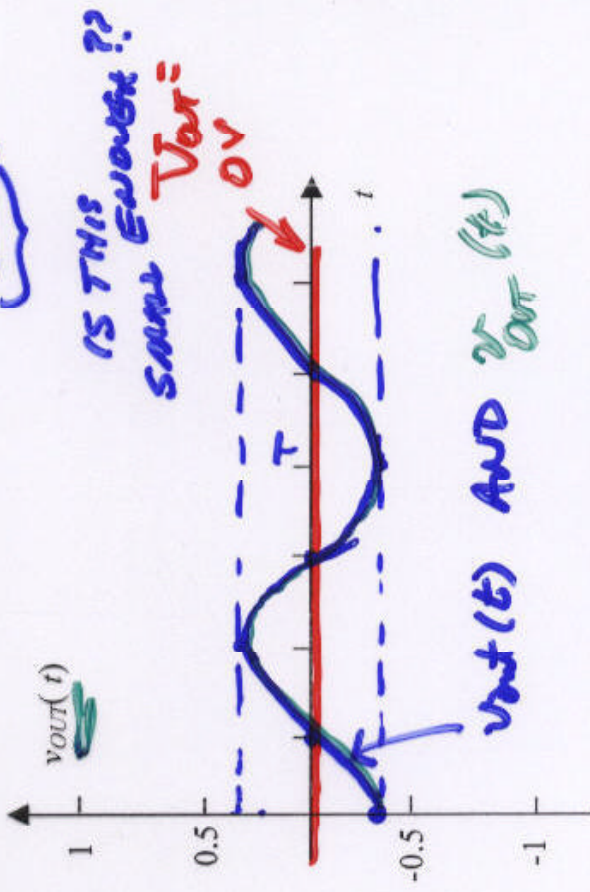
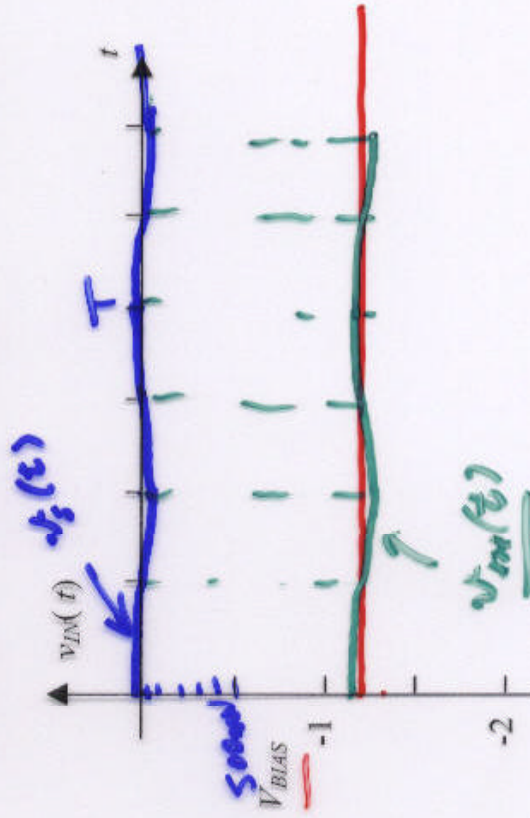
# Input and Output Waveforms

$$v_s(t) = 25 \text{ mV} \cos \omega t$$

$\uparrow 2\pi/T$

Input small-signal voltage amplitude: 25 mV

Output small-signal voltage amplitude:  $14 \times 25 \text{ mV} = 350$



$$V_{os} = 1.3 = \underbrace{V_{bias}}_{-1.2V} + \underbrace{2.5V}_{-(-V_{sup})}$$

$$v_{out} \approx (14) v_i = (-350 \text{ mV}) \cos \omega t = -0.35$$

# Maximum Output Amplitude

$$v_{out}(t) = \underbrace{-2.19 \text{ V}}_{v_{rms} = \frac{A_{v}}{\sqrt{2}}} \cos(\omega t) \rightarrow v_s(t) = \underline{153 \text{ mV}} \cos(\omega t)$$

How accurate is the small-signal (linear) model?

$$\underbrace{\text{LAST TIME}} \left\{ \frac{v_s}{V_{GS} - V_{Th}} = \frac{0.15}{0.31} \approx \underline{0.5} \right.$$

Significant error in neglecting third term in expansion of  $i_D = i_D(v_{GS})$

