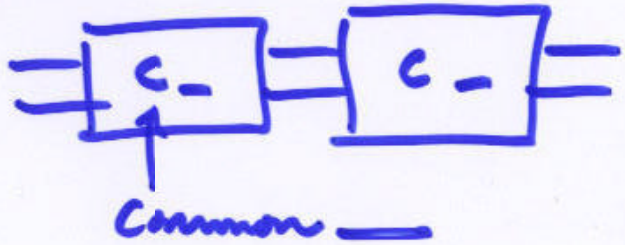
LECTURE 34 (B)

LAST TIME:

CASCODE I SOURCE $\begin{cases} r_{oc} \rightarrow \text{HUGE} \\ v_{SUP,\,MIN} \text{ LARGER.} \end{cases}$

MULTI-STAGE (CHAP. 3)

(3) 6 MOS STAGES
3 BJT STAGES



2-PORT MODELS.

NOT BASIC CHAP.

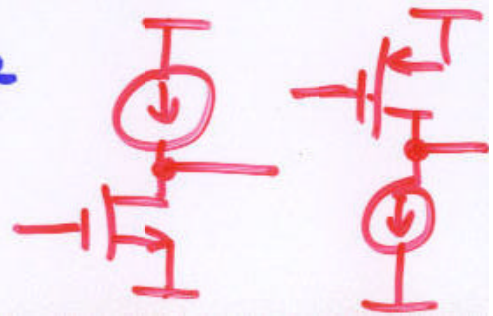
427 MODELS.

TODAY:

MORE EXAMPLES... CURRENT BUFFER

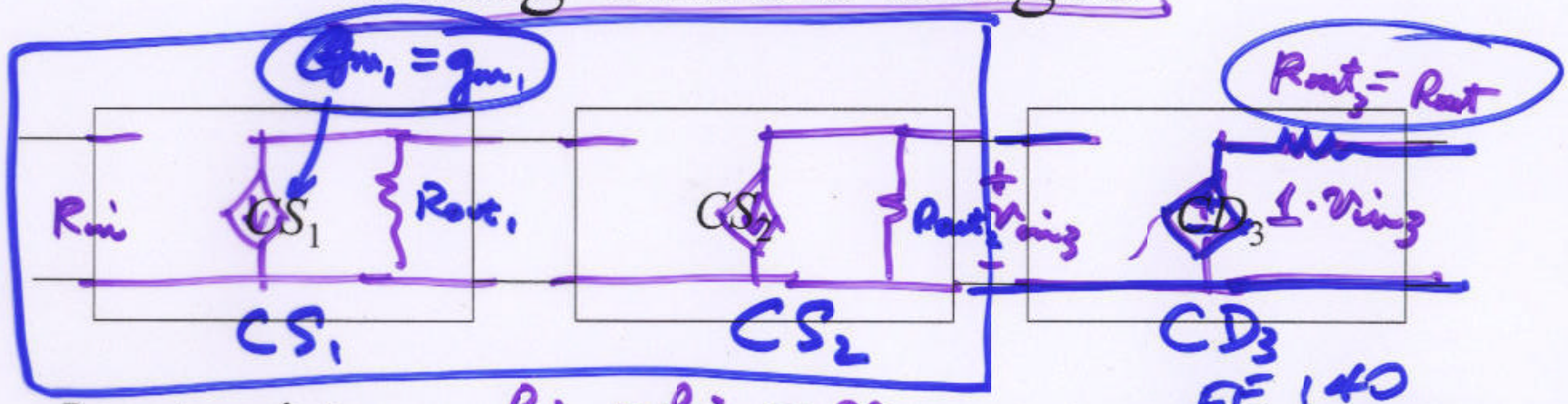
DC COUPLING.

$\Rightarrow$



VOLTAGE AMPS

Using CMOS Stages



Input resistance: $R_{in} = R_{in1} = \infty$

∞

Voltage gain (2-port parameter):

BIG

$(-g_{m1} R_{out1})(-g_{m2} R_{out2})(\cdot 1)$

$g_{m1} g_{m2} R_{out1} R_{out2}$

$A_{V1} \cdot A_{V2} \rightarrow$

Output resistance:

SMALL

$R_{out} = \left(\frac{1}{g_m}\right)$ ← use gmb ... $v_{SB} = 0$

SMALL

Dept. of EECS

University of California at Berkeley

EE 140

WHY HUGE GAIN?

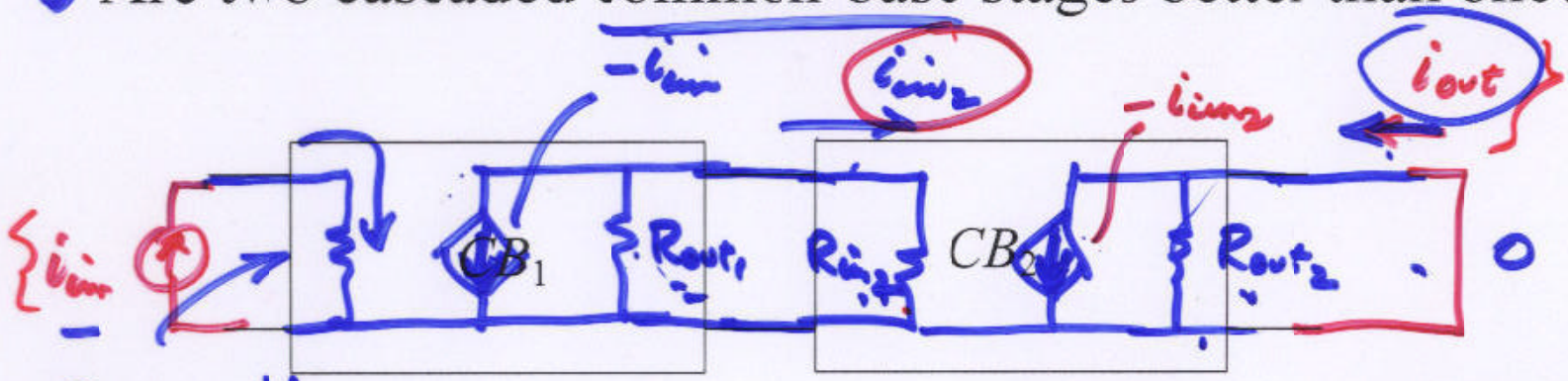
WE WILL USE FEEDBACK TO DESIGN BETTER AMPS.

WASN'T TRUE FOR CE, -CE ✓

R. T. Howe

Multistage Current Buffers

- Are two cascaded common-base stages better than one?



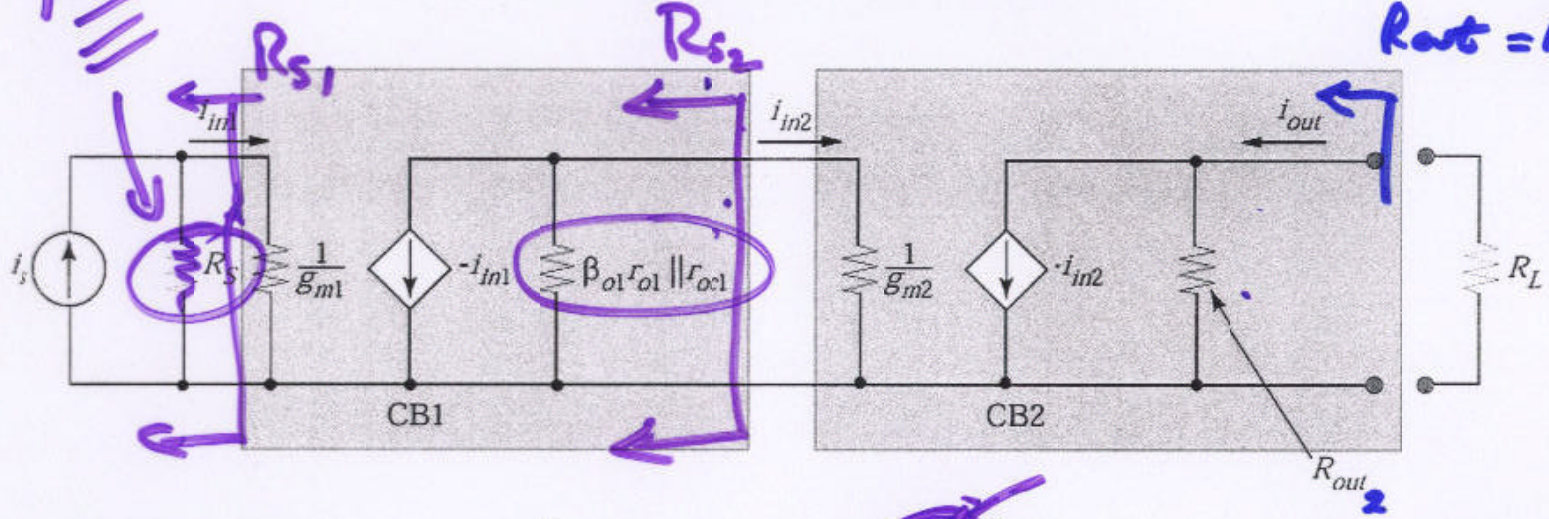
Input resistance: $R_{in} = R_{in1}$

$$A_i = \left.\frac{i_{out}}{i_{in}}\right|_{\substack{R_S=\infty \\ R_L=0}} = (-1)\left(\frac{R_{out1}}{R_{in2}+R_{out1}}\right)$$

$$i_{in2} = [-(-i_{in})]\left[\frac{R_{out1}}{R_{in2}+R_{out1}}\right]$$

$$i_{out} = -i_{in2}$$

Two-Port Models



$$R_{out} = R_{out2} \cong r_{02}\left(1 + g_{m2} r_{\pi 2} \| R_{S2}\right) \| r_{oc2}$$

$$R_{out} = r_{o2}\left(1 + g_{m2} r_{\pi 2} \,\|\, \{ r_{oc1} \,\|\, \{ (1 + g_{m1} r_{\pi 1} \,\|\, R_S) r_{o1} \} \}\right) \| r_{oc2}$$

$r_{\pi 1}$

$R_S = R_{out1}$

$$R_{out1} = r_{oc1} \,\|\, \{(1+\beta_o) r_{o1}\} \approx r_{oc1} \,\|\, \beta_o r_{o1} \leftarrow \text{TABLE.}$$

$R_S \gg r_{\pi 1}$ (TYPICAL ASSUMPTION)

$r_{\pi 2}$

$$R_{out} = r_{o2}\left(1 + g_{m2}(r_{\pi 2} \,\|\, \{ r_{oc1} \,\|\, \beta_o r_{o1} \})\right) \| r_{oc2}$$

BIG!!

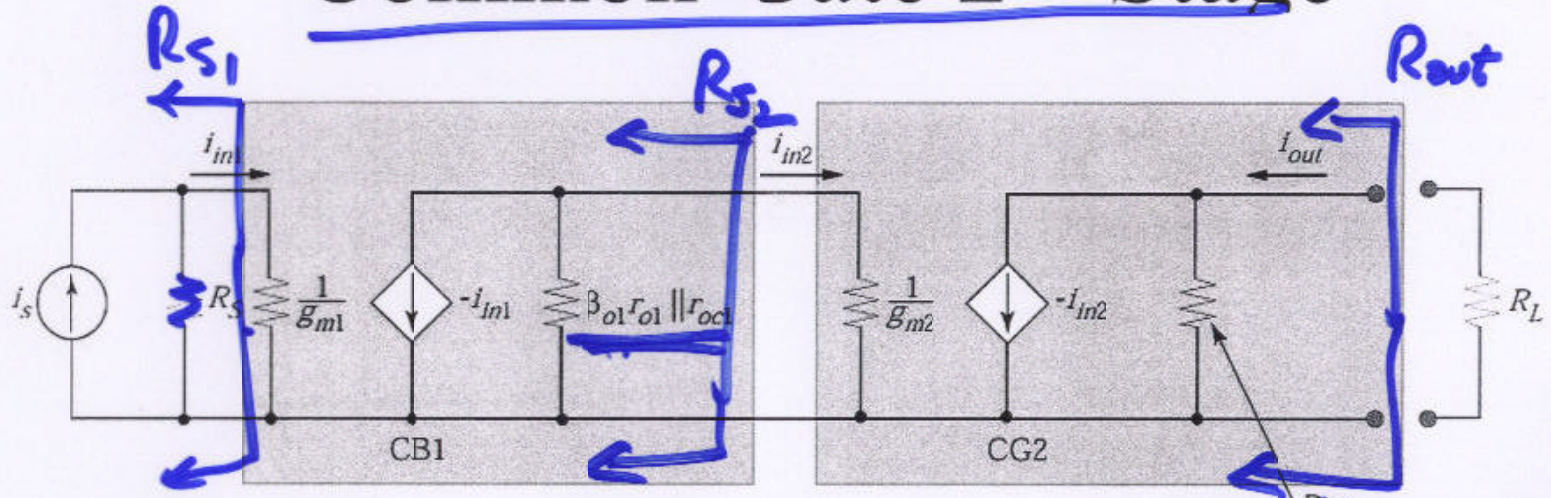
$$= r_{o2}(1 + g_{m2} r_{\pi 2}) \,\|\, r_{oc2}$$

$1 + \beta_o \approx \beta_o$

$$\boxed{R_{out} = \beta_o r_{o2} \,\|\, r_{oc2}}$$

CB1 - CG2

Common-Gate 2nd Stage



R_{S1} R_{S2} R_{out}

$$R_{out} = R_{out2} \cong r_{02}\left(1 + g_{m2} R_{S2}\right) \| r_{oc2} = r_{02}\left(1 + g_{m2} \cdot \left(R_S \| r_{o1} \| r_{oc1}\right)\right) \| r_{oc2}$$

$> 1\,M\Omega$

$$R_{S2} = R_{out1} = \left[\left(1 + g_{m1} r_{\pi 1} \| R_S\right) r_{o1}\right] \| r_{oc1} \approx 100\, r_{o2}$$

$100\,M\Omega$

$R_S >> r_{\pi 1}$

$$\cong (1+\beta_0)\, r_{o1} \| r_{oc1}$$

WORKS.

Summary of Cascaded Amplifiers

General goals:

1. Boost the gain parameter (except for buffers)
2. Optimize the input and output resistances

CHAPTER 8, SEC. 1

		R_{in}	R_{out}
I	Voltage:	∞	0
II	Current:	0	∞
III	Transconductance:	∞	∞
IV	Transresistance:	0	0

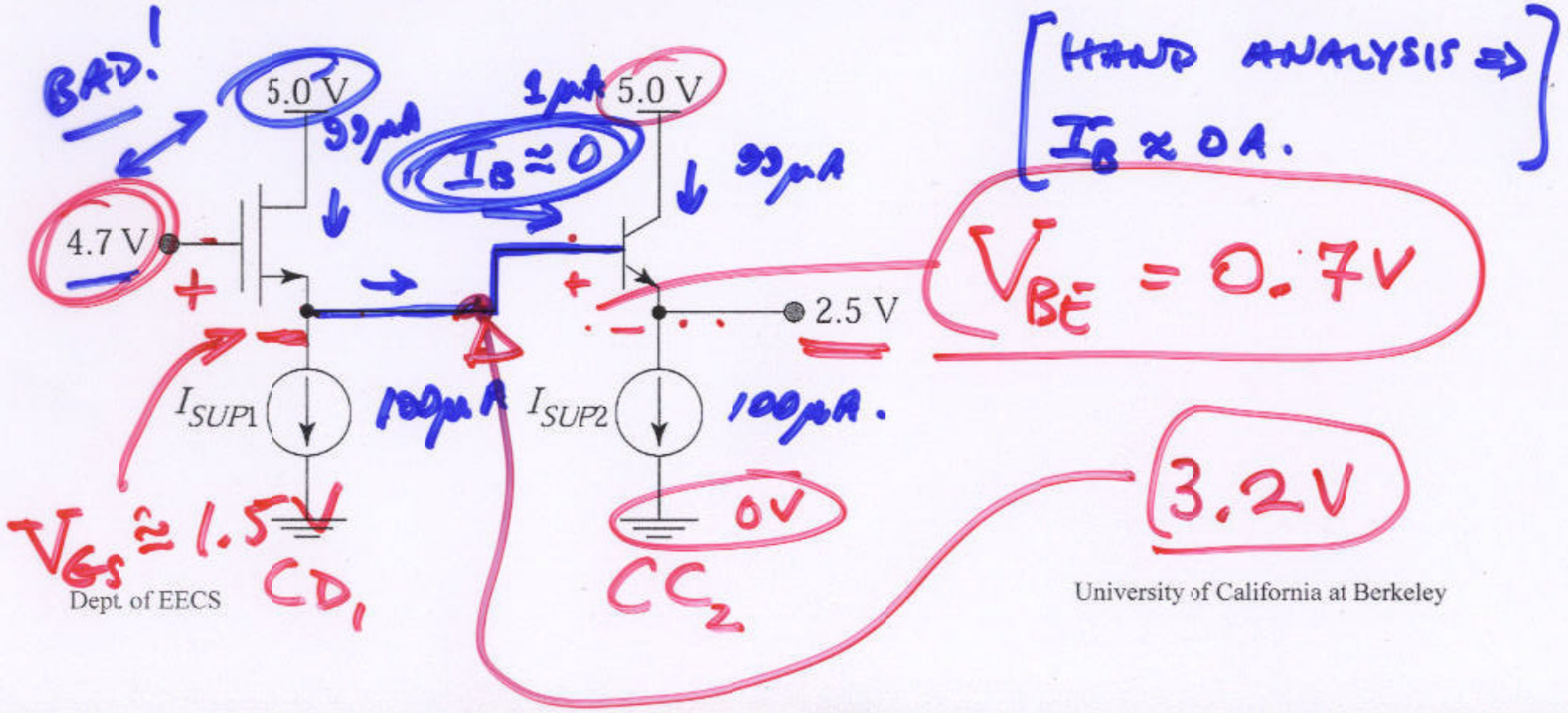
THIS MAKES DESIGN INTERESTING

Second Design Issue: DC Coupling

~~800~~ μH ≠ C ≠ 1μF

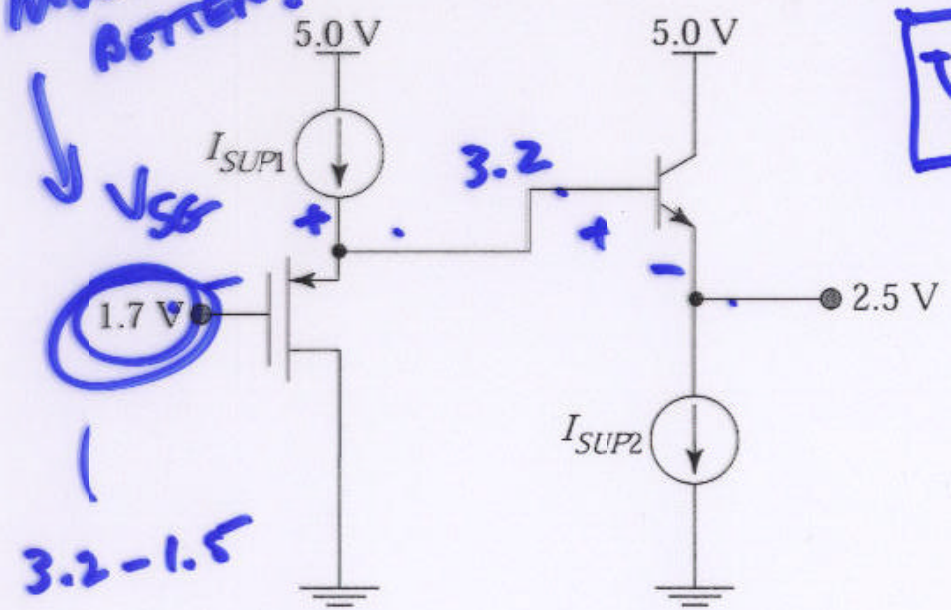
Constraint: large inductors and capacitors are not available

- Output of one stage is directly connected to the input of the next stage → must consider DC levels … why?



Alternative CG-CC Cascade

Use a PMOS CD Stage: DC level shifts upward



MUCH BETTER!

V_{SG}

3.2 - 1.5

$V_{SG} \approx 1.5$ V.

$V_{SG} = -V_{Tp} + \sqrt{\frac{2(-I_D)}{\mu_p C_{ox}(W/L)}}$

$-(-1)$

0.5

CD_1 CC_2

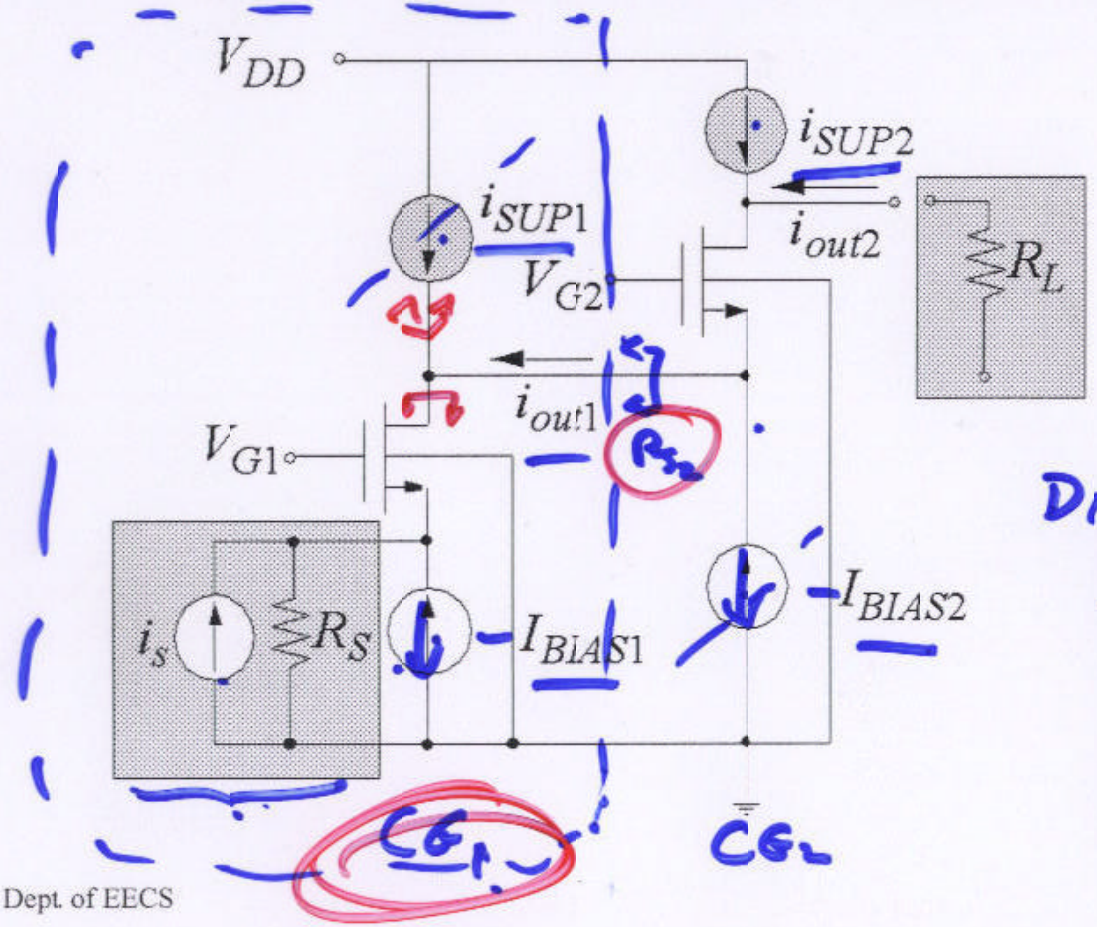
↑

PMOS VARIANT.

WEIRD STAGE.

CG Cascade: DC Biasing

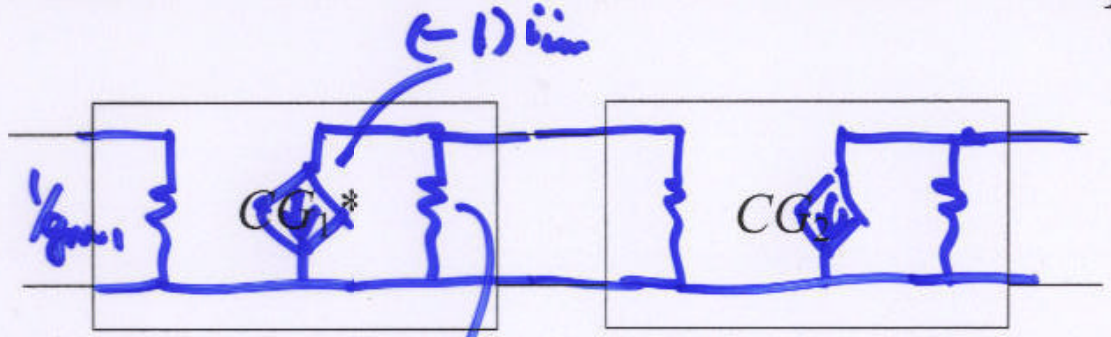
- Two stages can have different supply currents

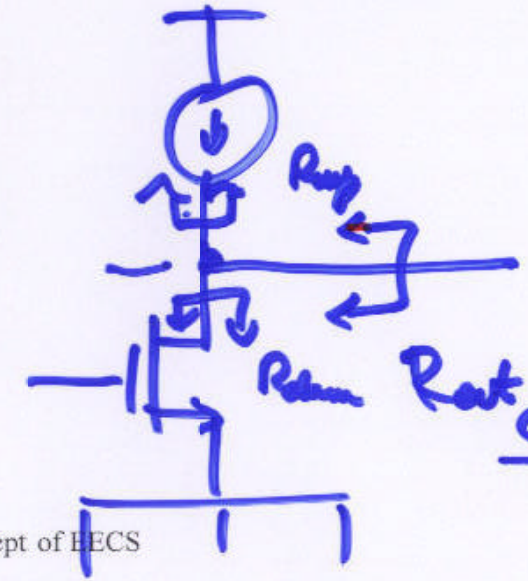


Extreme case:
$I_{BIAS2} = 0$ A

DIFFERENT I_D's ...
SOME ADVANTAGE
$1/g_m$.

• Two-Port Model of Common-Gate Cascade with Shared Current Supply





$R_{out_1} = R_{down} = (1 + g_{m1} R_{S1}) r_{o1}$

$R_{out_{CG}} = R_{up} \parallel R_{down}$

$= r_{oc} \parallel (1 + g_{m1} R_{S1}) r_{o1}$

NO r_{oc}.