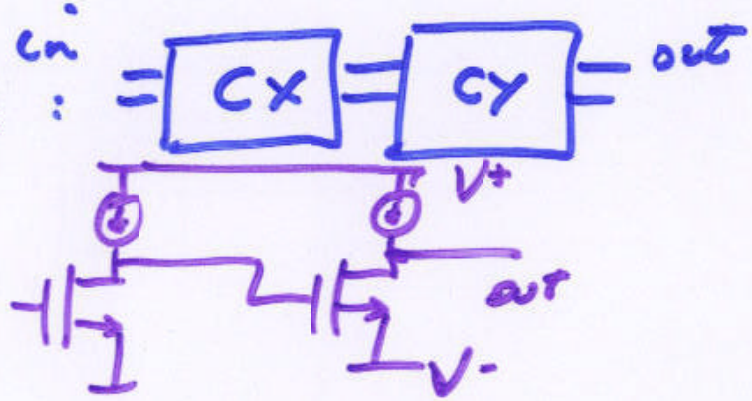
Lecture 35

- Last time:
  - More examples of cascades (§9.1)
  - DC coupling issues
- Today :
  - Cascode amplifiers
  - Totem pole voltage supplies
  - Start: multistage amplifier design examples...



EE 140.

→ CHAPTER 10 NEXT WEEK

WHAT IS ω_{-3dB}? (MULTISTAGE)

DC LEVEL SHIFTS

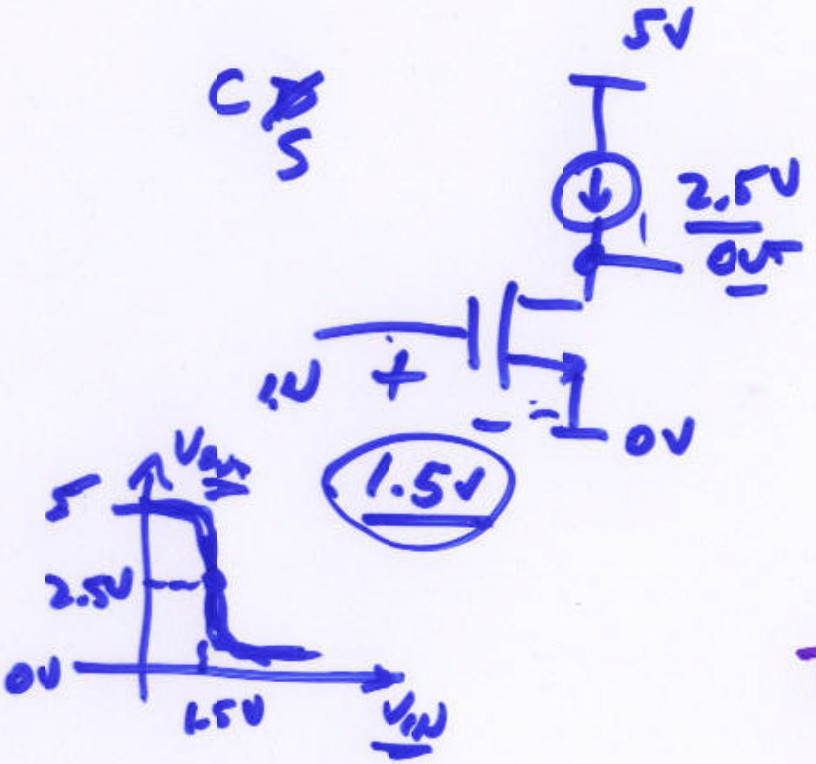
MOS STAGES

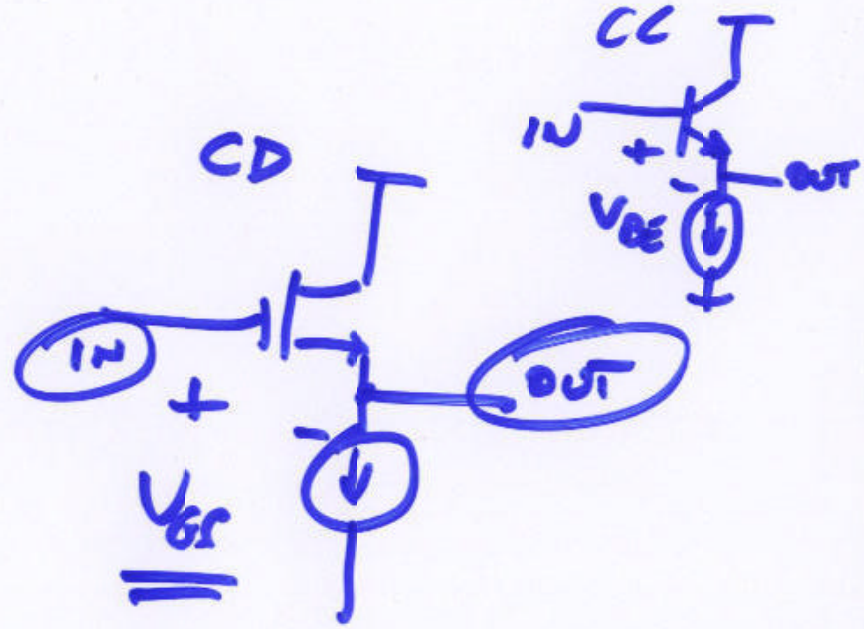
	NMOS	PMOS
CS	↑ TYPICAL	↓ TYPICAL
CG	↑	↓
CD	↓ *	↑ *

BJT STAGES

	npn
CE	↑
CB	↑
CC	↓ * ≃ 0.7V

* PRECISE/KNOWN SHIFT



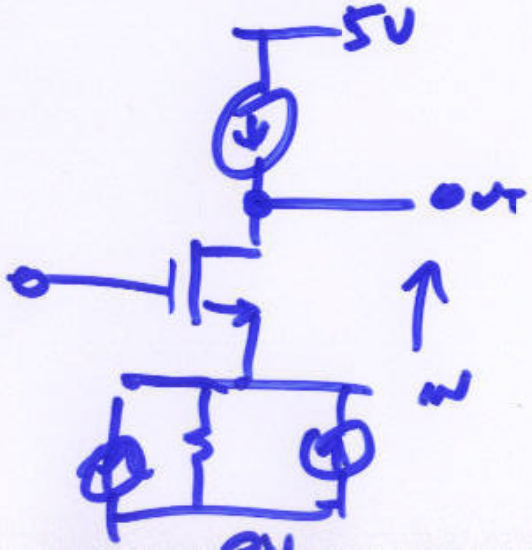


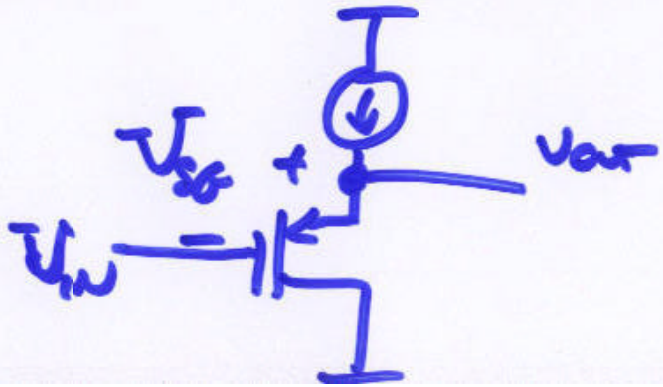
$V_{OUT} = V_{IN} - V_{GS}$.

KNOWN ...

DESIGN IT!

$V_{out}/V_{in} \simeq 1$





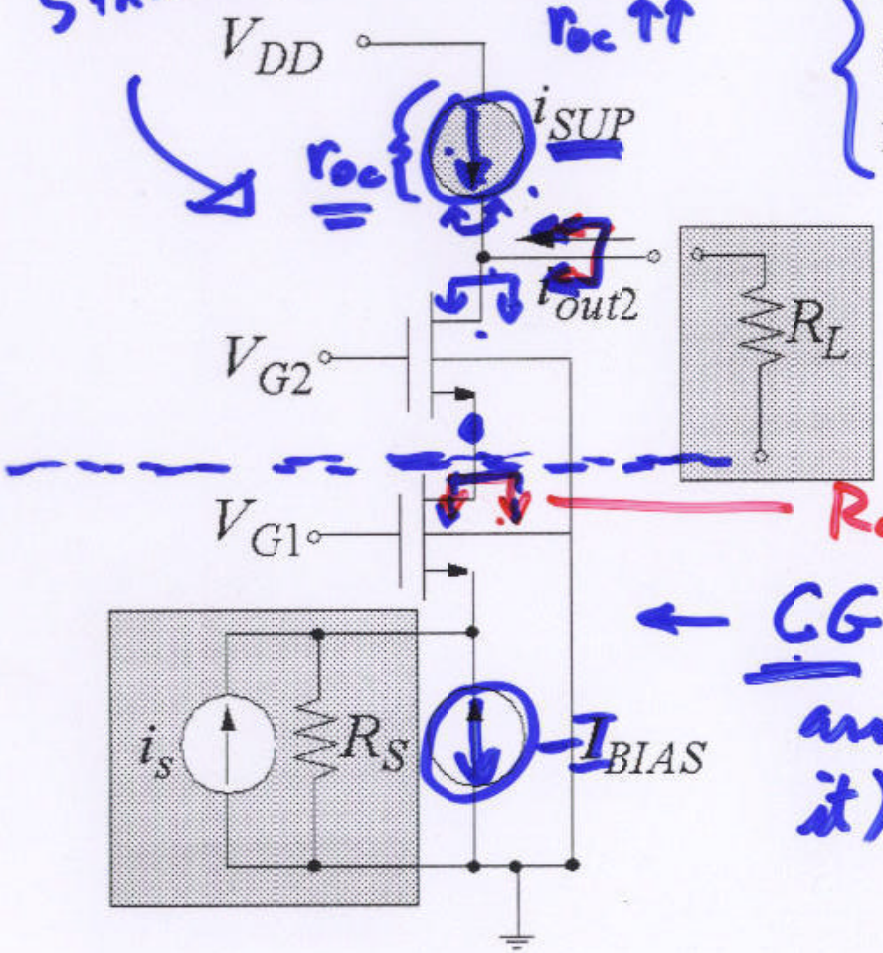
CG1/CG2 (TYPICALLY)

R. T. Howe

CG Cascade: Sharing a Supply

STACKED/CASCODE i_{SUP}. r_{oc} ↑↑

First stage has no current supply of its own → its output resistance is modified



$R_{out} = r_{oc} \| \{ r_{o2}(1 + g_{m2} R_{S2}) \}$

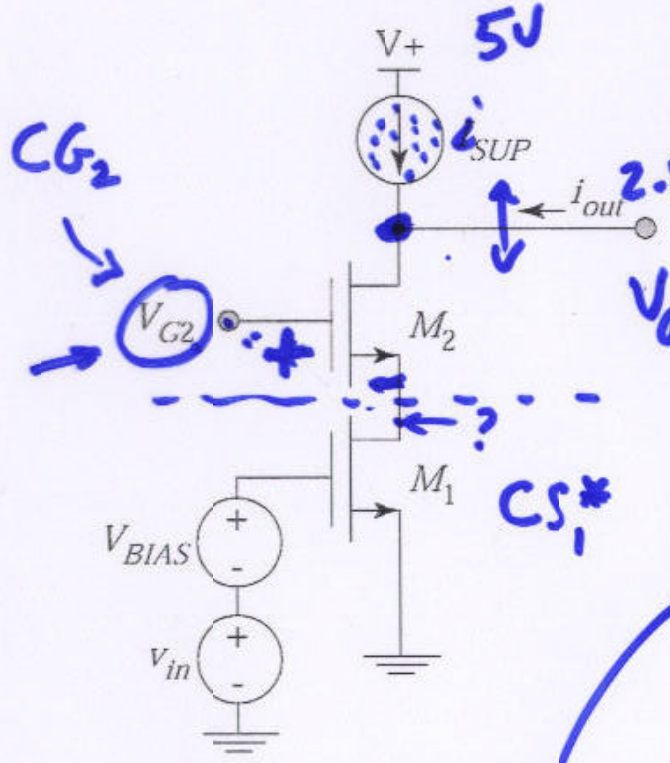
↑ $R_{out_{CG*}}$

$R_{out_{CG*}} = R_{down}$.

← CG* (no i_{SUP} associated with it) → no r_{oc} ↓

$R_{out} = r_{o1}[1 + g_{m1} R_S]$

The Cascode Configuration



Common source / common gate cascade is one version of a *cascode* (all have shared supplies)

$V_{GS_2} = V_{GS_1}$ (CONVENIENCE)

DC bias: SELECT V_{BIAS} SUCH THAT

$$I_{D_1} = I_{SUP} = \mu_n C_{ox} \left(\frac{W}{2L}\right)_1 (V_{BIAS} - V_{tn})^2$$

Two-port model: first stage has no current supply of its own

TYPICAL

$$V_{BIAS} = V_{tn} + \sqrt{\frac{2 I_{SUP}}{\mu_n C_{ox} (W/L)_1}}$$

100 μA

$\frac{W}{L} = 200$

$L = 1$

$\mu_n C_{ox} = 100\ \mu A/V^2$

$= V_{tn} + \sqrt{\frac{1}{100}}$

- WHAT SETS V_{G2}?

$$V_{S2} = V_{D1} = V_{G2} - V_{GS2}$$

1.1V

$$V_{OUT,min} = V_{S2} + V_{DS2,min}$$

?

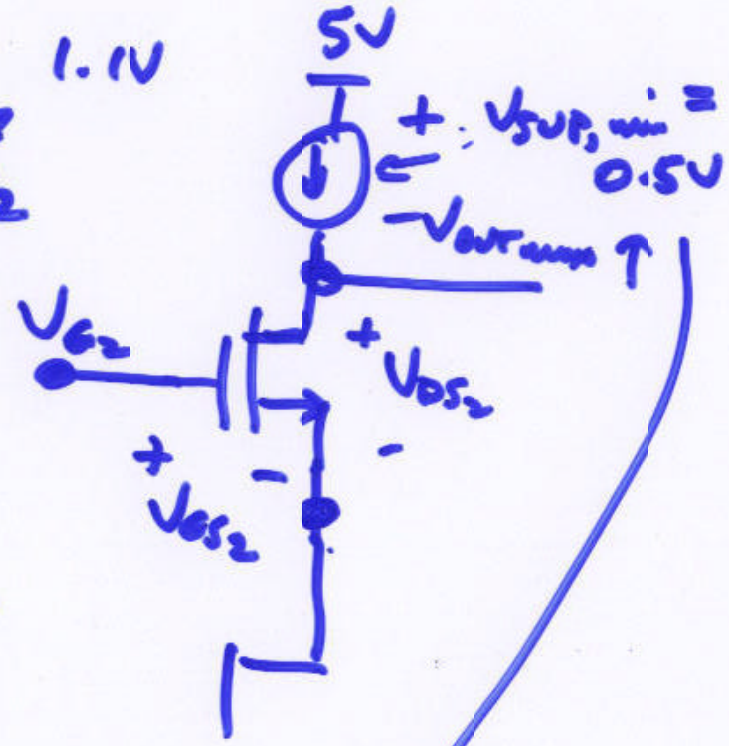
$$V_{DS2,SAT} = V_{GS2} - V_{TH} = 1.1 - 1 = 0.1$$

$$V_{OUT,min} = V_{S2} + 0.1$$

$$V_{G2} - 1.1$$

$$V_{OUT,min} = V_{G2} - 1.1^{V} + 0.1^{V}$$

$$\boxed{V_{OUT,min} = V_{G2} - 1V.}$$



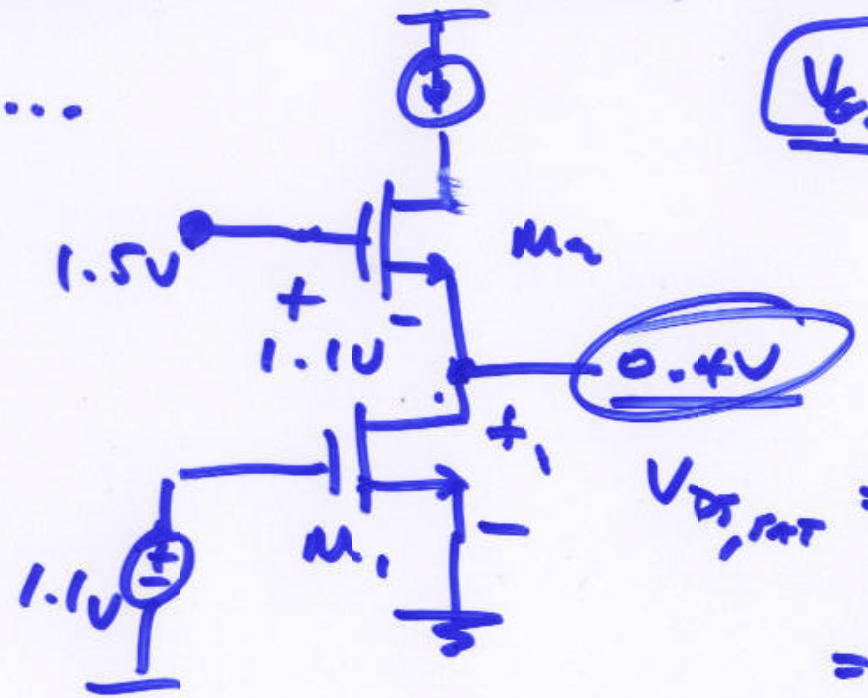
$$V_{OUT,max} = 5V - V_{SUP,min} = 4.5V$$

Symmetry ⇒ $V_{OUT,max} = 1.5V$.

$V_{OUT,min} = 0.5V$. ⇒

$V_{GS_2} = 1.5V$

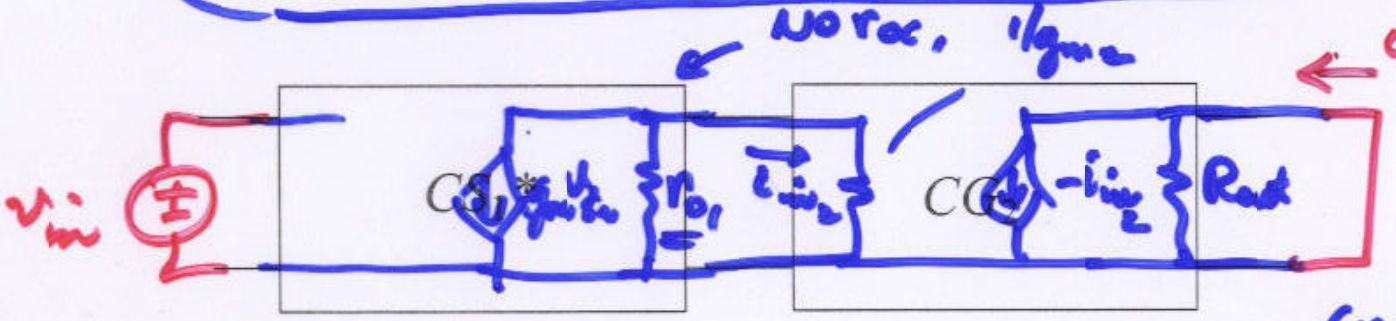
Check ...



$V_{DS,sat} = 1.1 - V_{th}$

$= 0.1$

Cascode Two-Port Model



Output resistance of first stage = $R_{out,CS^*} = R_{down,CS} = r_{o1}$

→ Why is the cascode such an important configuration?

$G_m \equiv \left.\frac{i_{out}}{v_{in}}\right|_{R_L \to 0\,\Omega,\ R_S \to 0\,\Omega}$

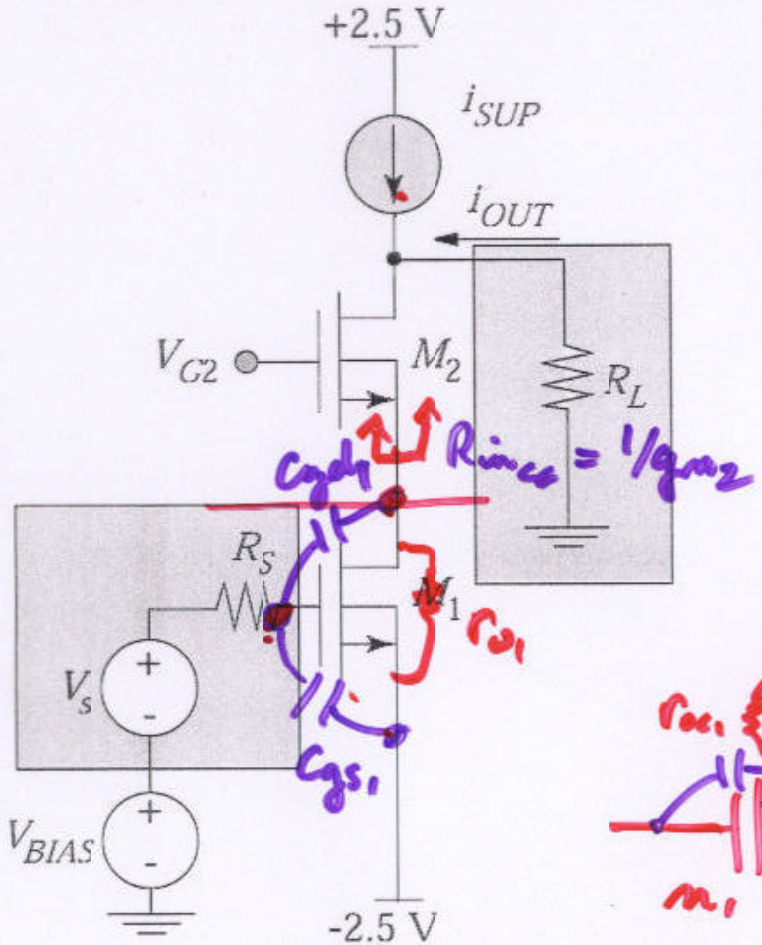
$i_{out} = -i_{in_2}$

$i_{in_2} = \left[-g_{m_1} v_{in}\right] \cdot \left[\frac{r_{o1}}{r_{o1} + 1/g_{m2}}\right] \to 1$

$G_m = +g_{m_1}$

Miller Capacitance of Input Stage

Find the Miller capacitance for C_{gd1}



Input resistance to common-gate second stage is low → gain across C_{gd1} is small.

→ KILLS THE MILLER EFFECT

$\frac{1}{g_{m2}}$

$-g_{m1}\cdot[r_{o1} \| R_{in\,CG}]$

$C_{M1} = C_{gd1}\left(1 - A_{V\,C_{gd1}}\right)$

$\approx C_{gd1}\left(1 - \left(-\frac{g_{m1}}{g_{m2}}\right)\right) = 2C_{gd1}$

$A_{VC_{gd1}} = \frac{v_{d1}}{v_{g1}} = \frac{v_{ds1}}{v_{gs1}}$

$R_{in2} = 1/g_{m2}$

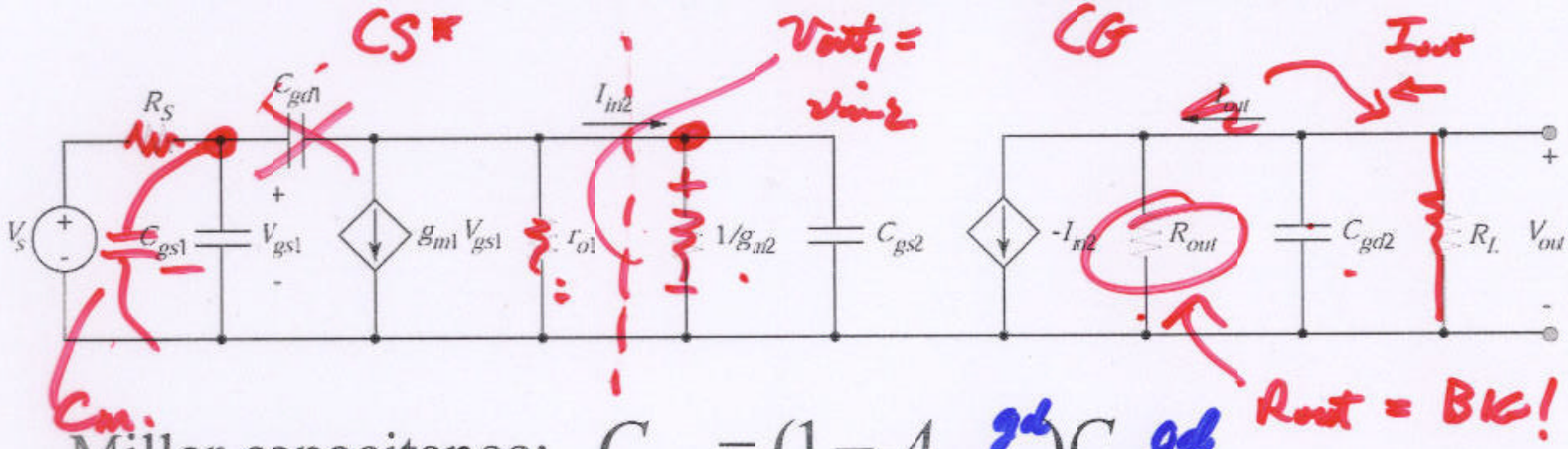
C_{gd1} r_{o1} C_{gs1}

r_{oc1} R_{up} m_1

$A_{VC_{gd1}} = -g_{m1}\, r_{o1} \| R_{oc1}$ ↓ R_{up}

normal ≈ -100.

Two-Port Model with Capacitors



Miller capacitance: $C_M = (1 - A_{vC})C_{gd1}$

$A_{vgd} = \frac{V_{out1}}{V_{in1}} = -g_{m1}[r_{o1} \| (1/g_{m2})] \approx -\frac{g_{m1}}{g_{m2}}$

← NOT v_s!

SMALL

$C_M = \left(1 + \frac{g_{m1}}{g_{m2}}\right) C_{gd1}$

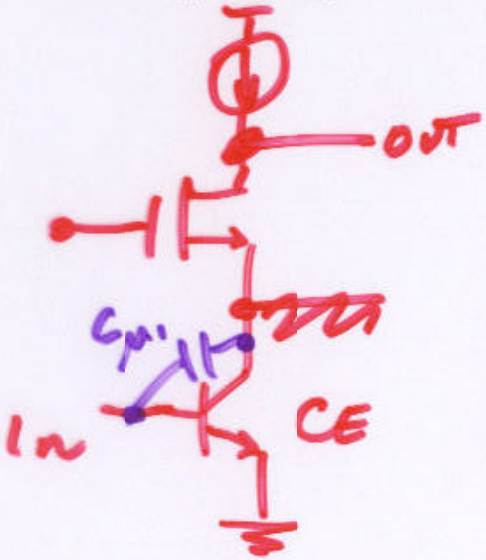
LARGE.

$v_{out}/v_{in} = A_v = -g_{m1}(R_{out} \| R_L)$

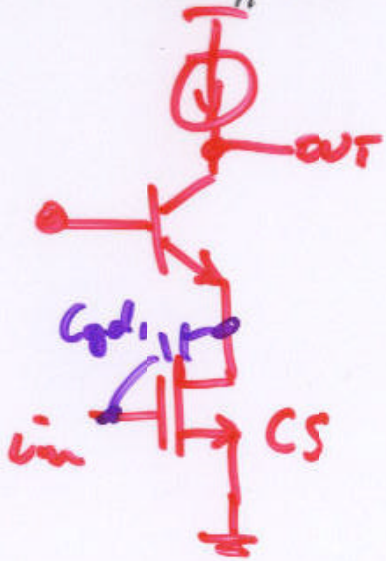
Other Cascode Configurations

Basic configuration: transconductance stage followed by current buffer

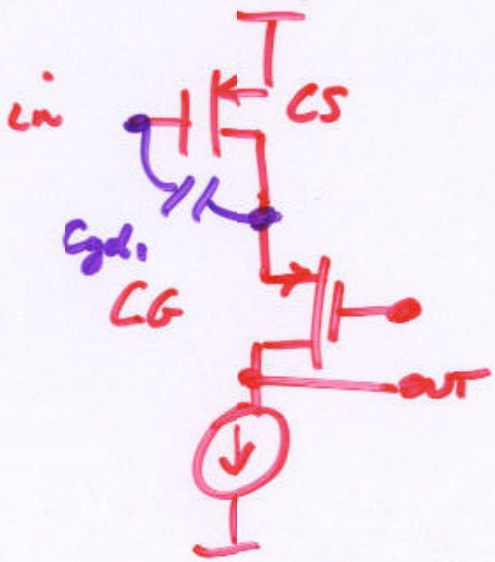
CE_n-CG_n



CS_n-CB

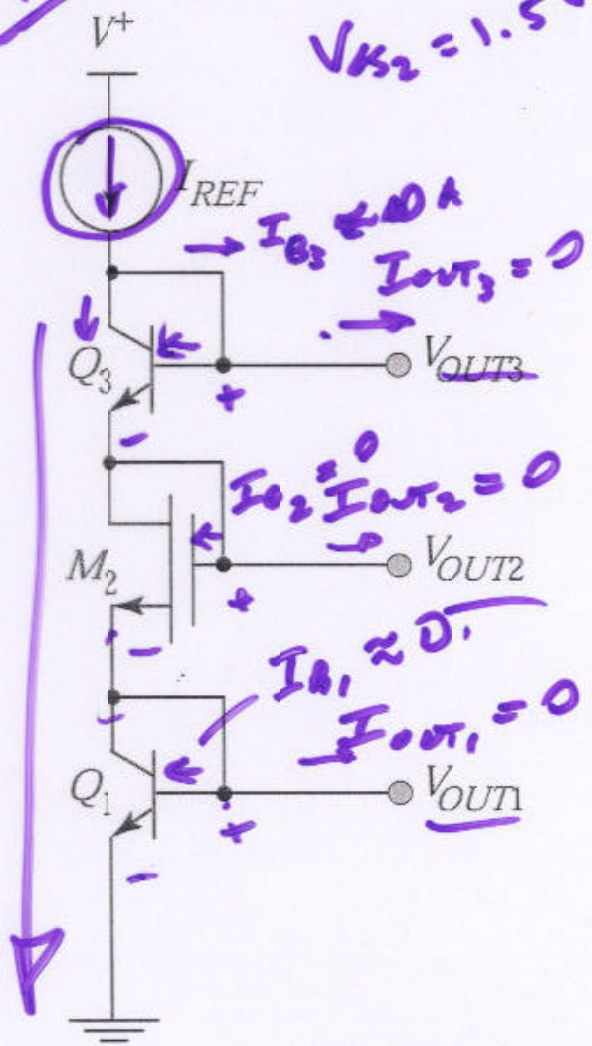


CS_p-CG_p



TOTEM POLE

Generating Multiple DC Voltages



$V_{GS_2} = 1.5V$

$I_{B_3} \approx 0$ A

$I_{OUT_3} = 0$

$I_{B_2} = 0$ $I_{OUT_2} = 0$

$I_{B_1} \approx 0$

$I_{OUT_1} = 0$

Stack-up diode-connected MOSFETs or BJTs and run a reference current through them → pick off voltages from gates or bases as references

$V_{OUT_1} = 0.7V$

$V_{OUT_2} = 0.7V + 1.5 = 2.2V$ (V_{GS_2})

$V_{OUT_3} = 2.2V$.