Lecture 37

- Last time:
  - Complete "lecture design" of two-stage CMOS transconductance amplifier
- Today :
  - CMOS cascode transconductance amplifier design example

OH TUESDAY 9:30 – 11

STRATEGY.

V_{OUT} OR i_{OUT}

✓ (1) FIND THE LIMITS USING MOS.

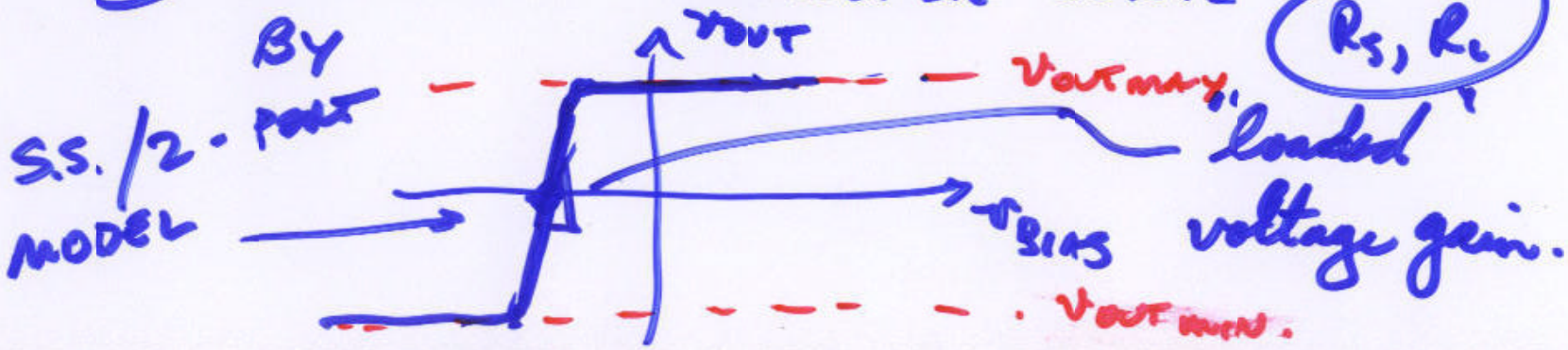
→ TRIODE / SAT BOUNDARY

→ CURRENT LIMITS.

.* THERMAL LIMITS. [FUTURE COURSES...]

PICKING THE LOWEST ONE.

(2) COMPLETE TRANSFER CURVE BY SS./2-PORT MODEL



Limits to Output Voltage

- M_6 will leave saturation when v_{OUT} drops to:

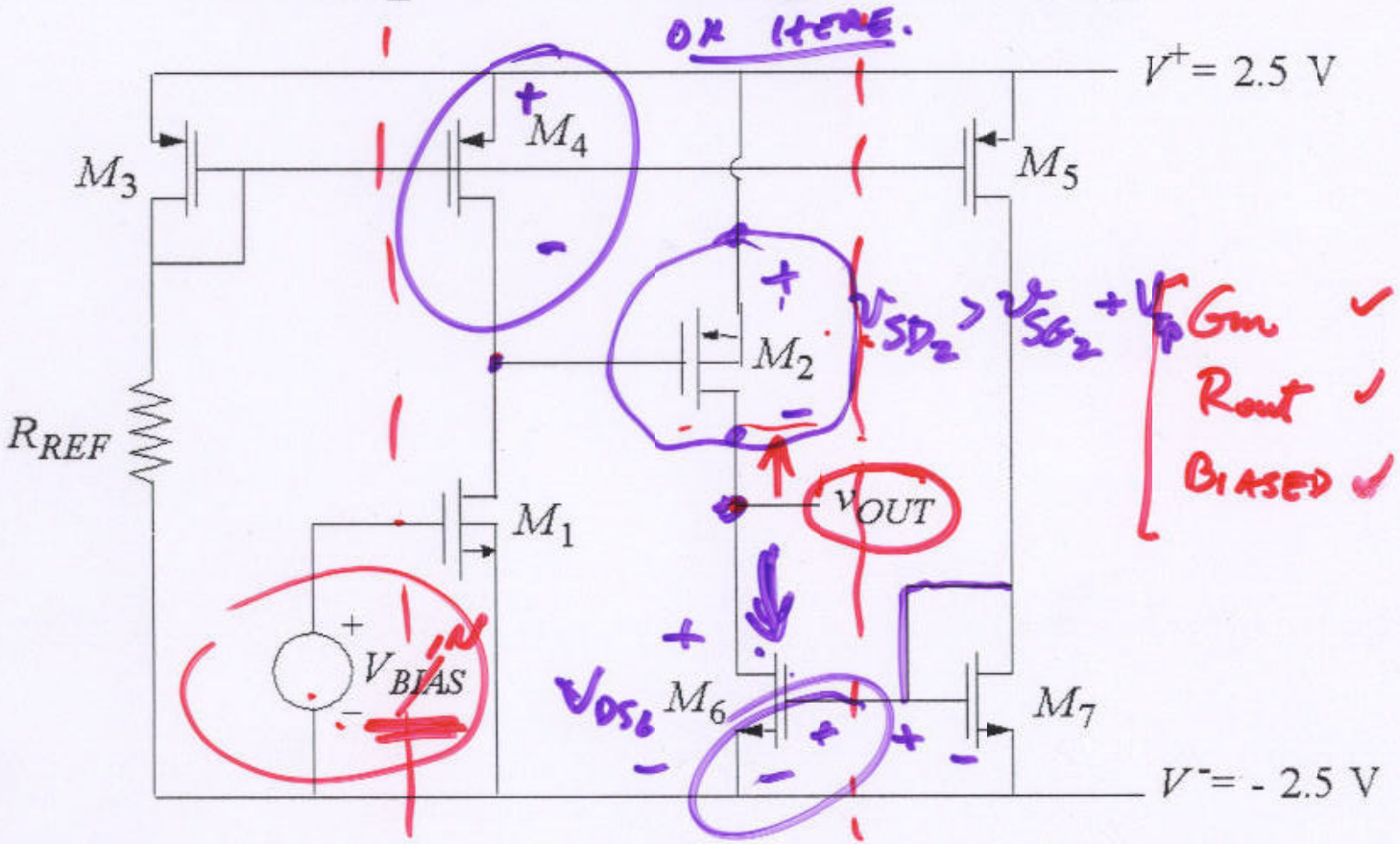
$$v_{OUT,MIN} = V^- + V_{DS6,sat} = -2.5 + \sqrt{\frac{2I_{D6}}{\mu_n C_{ox}(W/L)_6}}$$

- M_2 will leave saturation when v_{OUT} rises to:

$$v_{OUT,MAX} = V^+ - V_{SD2,sat} = +2.5 - \sqrt{\frac{2(-I_{D2})}{\mu_p C_{ox}(W/L)_2}}$$

What about M_4?

Output Voltage Swing



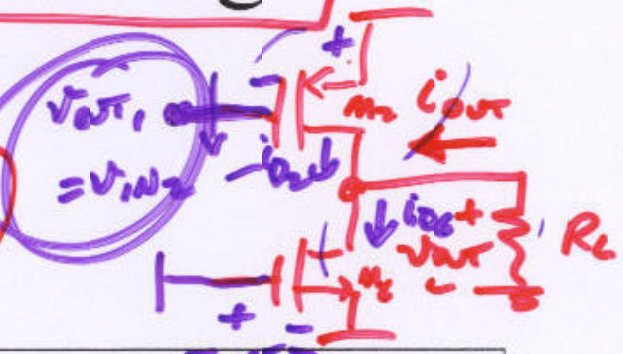
- Transistors M_2 and M_6 will limit the output swing

→ TRANSFER FN. $V_{OUT} = f(V_{BIAS})$

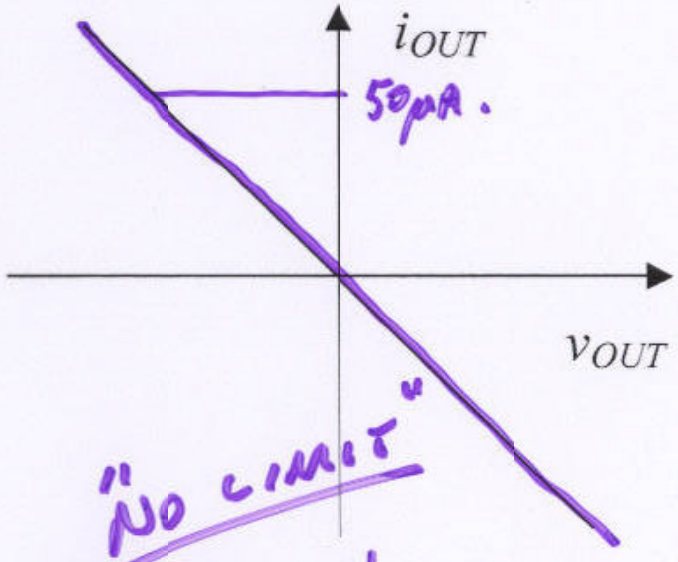
Output *Current* Swing

Load resistor: pick $R_L = 25\ \text{k}\Omega$

Output current: $i_{OUT} = -v_{OUT} / R_L$



$$i_{OUT} = i_{D6} - \left(-i_{D2}\right)$$



Limits: asymmetrical

M_2: can increase - i_{D2} . .

= BY INPUT

M_6: can't increase i_{D6}

$i_{D6} \approx 50\mu A.$

Output Current Limits

- Positive output current (negative v_{OUT})

$$i_{OUT,MAX} = i_{D6} - (0) = 50\mu A = -v_{OUT,MAX} / R_L$$

$$v_{OUT,MAX} = -(50\mu A)(25k\Omega) = -1.25V$$

(greater than limit set by saturation of M_6)

- Negative output current (positive v_{OUT})
  - No limit on current from M_2), so voltage swing sets current limit

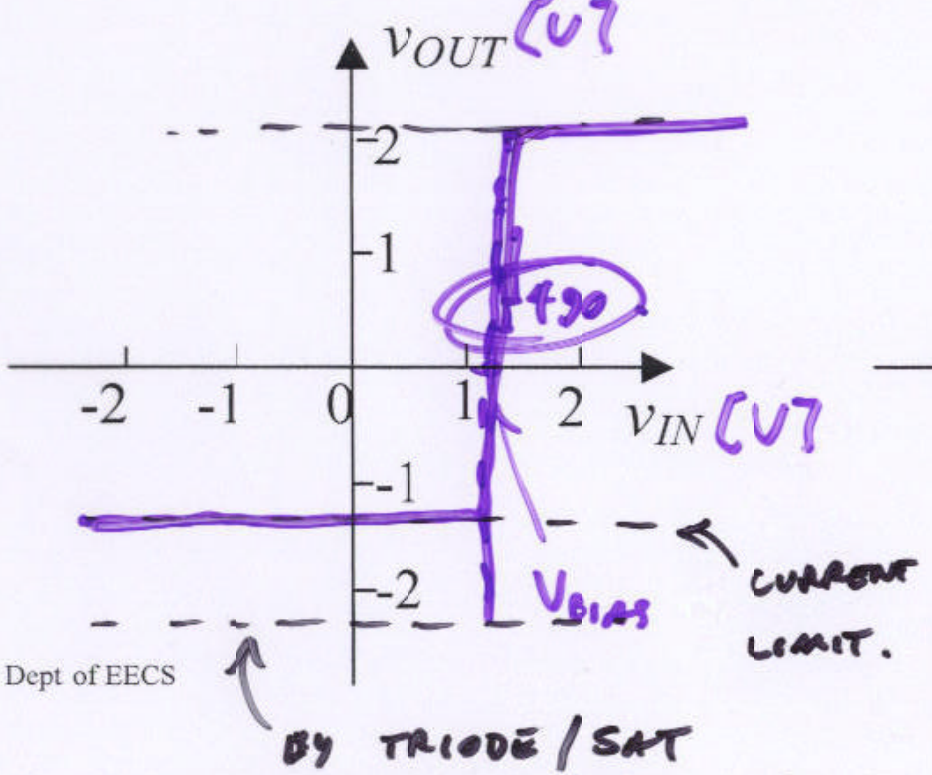
$$i_{OUT,MIN} = -v_{OUT,MAX} / R_L = -(2.18V / 25k\Omega) = -87.2\mu A$$

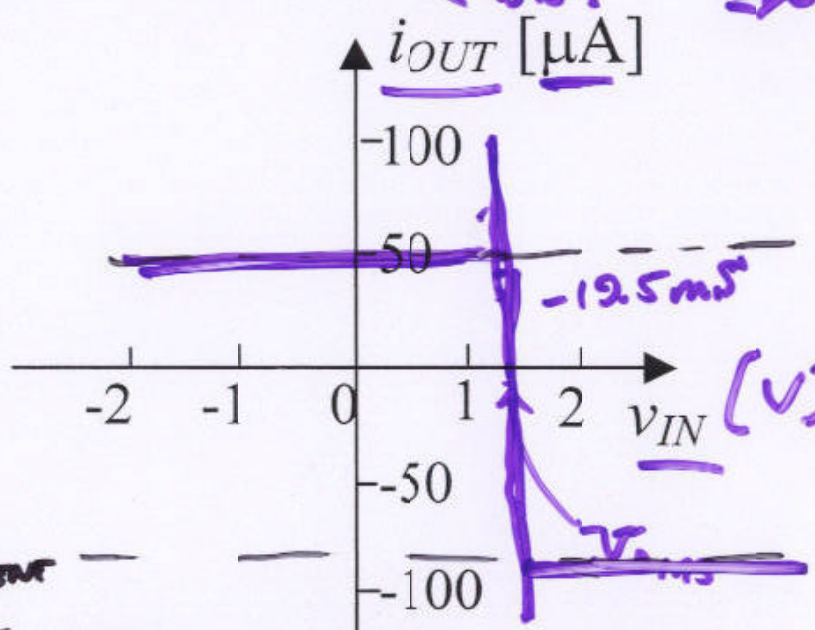
Transfer Curves (for $R_L = 25\ \text{k}\Omega$)

Loaded voltage gain = $v_{out}/v_{in} = (g_{m1}R_{out1})(g_{m2}R_{out}||R_L) = 490$

Loaded transconductance = i_{out}/v_{in}

$= (-g_{m1}R_{out1})(g_{m2})(R_{out}/(R_{out} + R_L) = -19.5\ \text{mS}$



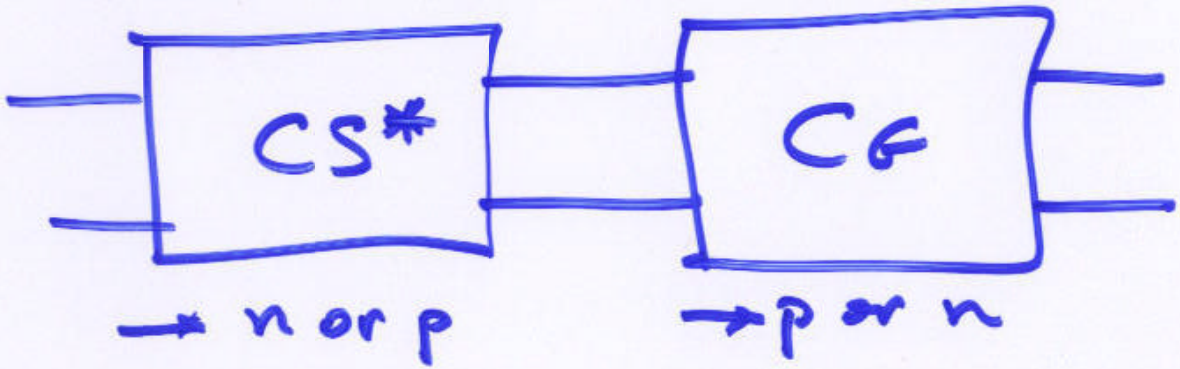


Amplifier Topology

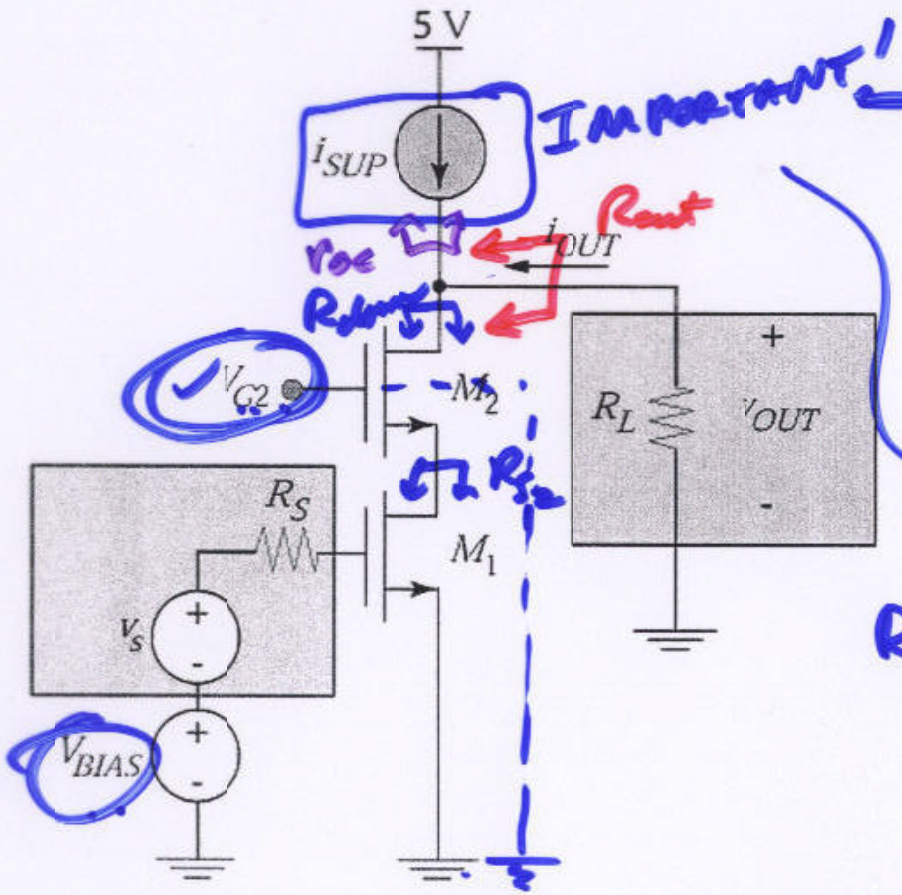
Goals: R_{in} and R_{out} should be maximized

Common source – common gate cascode makes sense

✓Share the current supply . . . STACK THEM UP.



* Amplifier Schematic



IMPORTANT!

Note that the backgate connection for M_2 is not specified: ignore g_{mb}

WHY?

r_{o1}

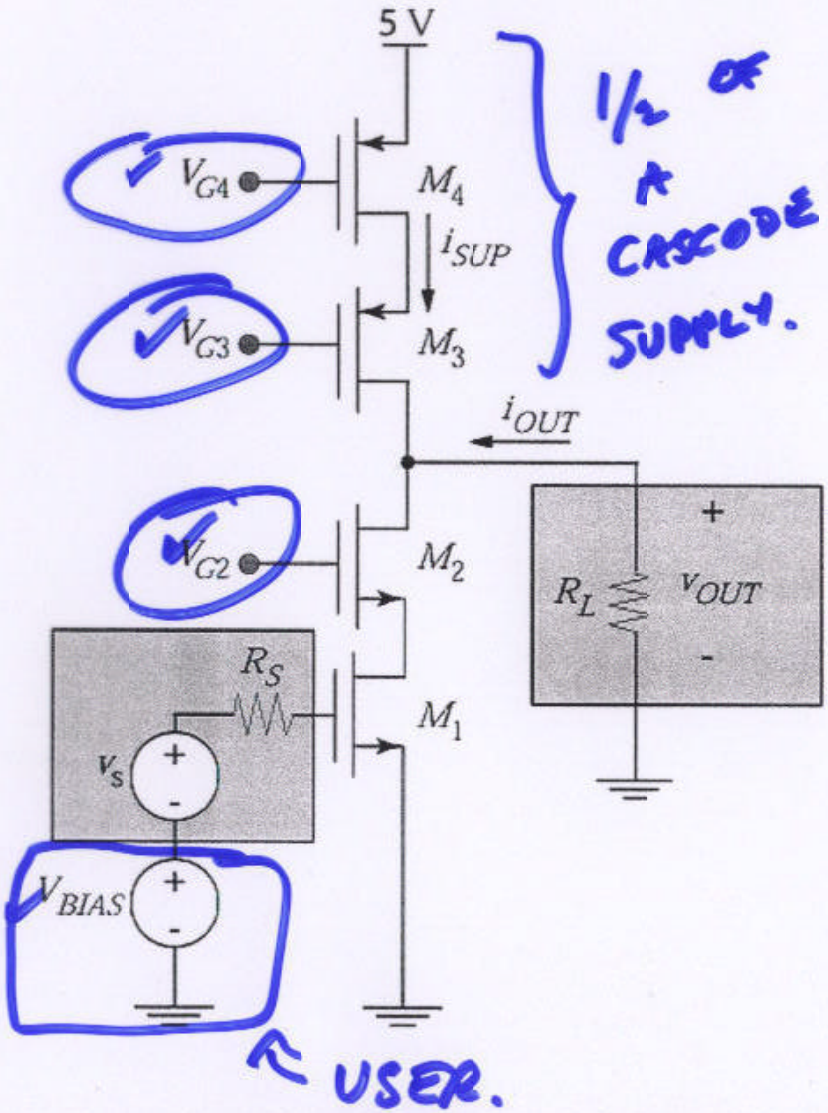
$r_{o2}(1+g_{m2}R_S)$

$R_{out} = r_{oc} \| R_{down}$

R_{up} MUST BE LARGE!

SIMPLE SOURCE ISN'T GOOD ENOUGH

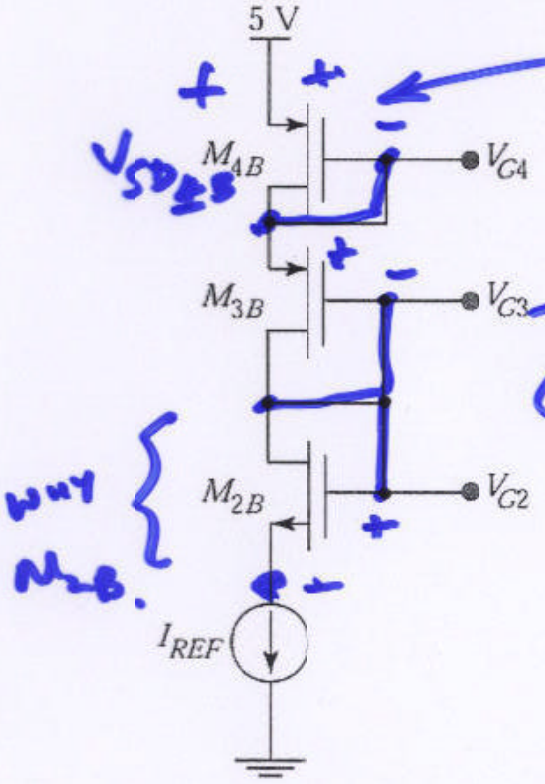
Current Supply Design



Output resistance goal requires large r_{oc} → use cascode current source.

Totem Pole Voltage Supply

DC voltages must be set for the cascode current supply transistors M_3 and M_4, as well as the gate of M_2.



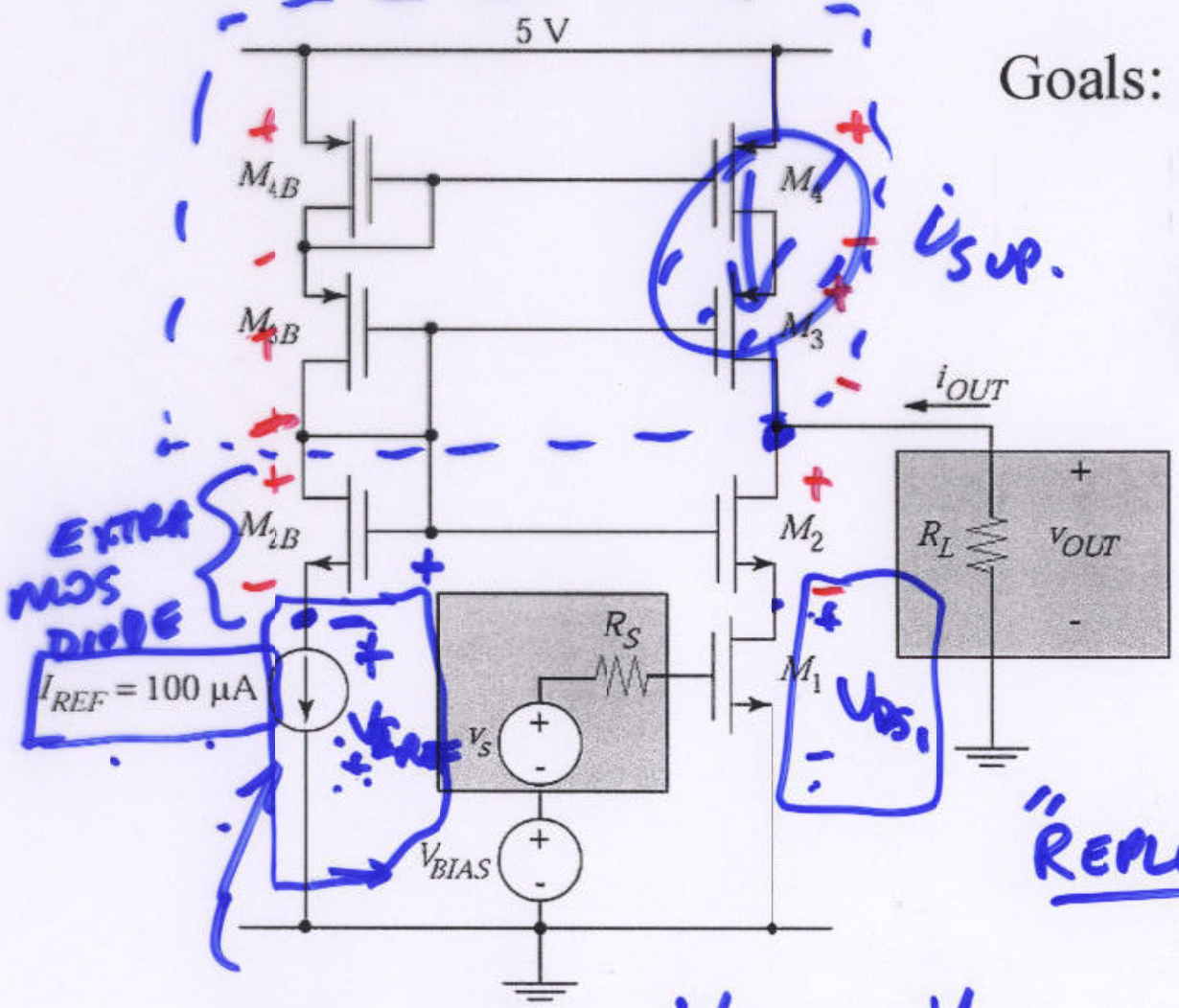
$V_{G4} = 5V - V_{SG4}$

$V_{SG4B} = -V_{tp} + \sqrt{\frac{2(-I_{REF})}{\mu_p C_{ox} (W/L)_{4B}}}$

$V_{G4} - V_{SG3B}$

Why include M_{2B}?

Complete Amplifier Schematic



Goals: $g_{m1} = 1$ mS,
$R_{out} = 10$ MΩ

i_{SUP}.

$\left(\frac{W}{L}\right)_{4B} = \left(\frac{W}{L}\right)_4$

EXTRA NMOS DIODE

"REPLICA BIASING".

M_{2B} MAKE $V_{I_{REF}} = V_{DS}$

Device Sizes

M_1: select $(W/L)_1 = 200/2$ to meet specified $g_{m1} = 1$ mS

→ find $V_{BIAS} = 1.2$ V

Cascode current supply devices: select $V_{SG} = 1.5$ V

$(W/L)_4 = (W/L)_{4B} = (W/L)_3 = (W/L)_{3B} = 64/2$

M_2: select $(W/L)_2 = 50/2$ to meet specified $R_{out} = 10$ MΩ

→ find $V_{GS2} = 1.4$ V

Match M_2 with diode-connected device M_{2B}.

Assuming perfect matching and zero input voltage, what is V_{OUT}?