 R. T. Howe

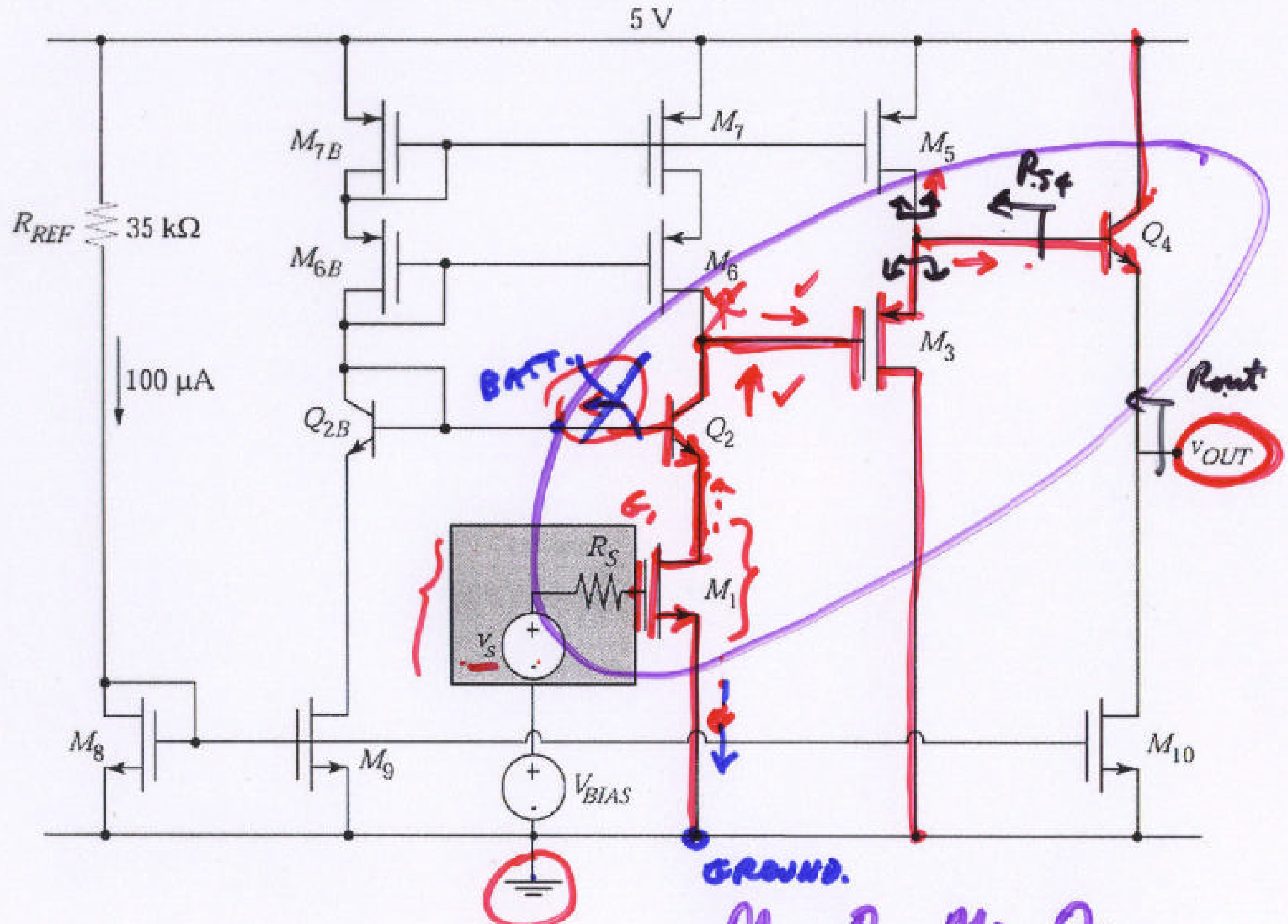
Lecture 39

- Last time:
  - BiCMOS voltage amplifier: example of "dissection" technique for a complicated circuit
- Today :
  - Bias and output swing for BiCMOS voltage amp
  - Start open-circuit time constant analysis (back to Chapter 10)

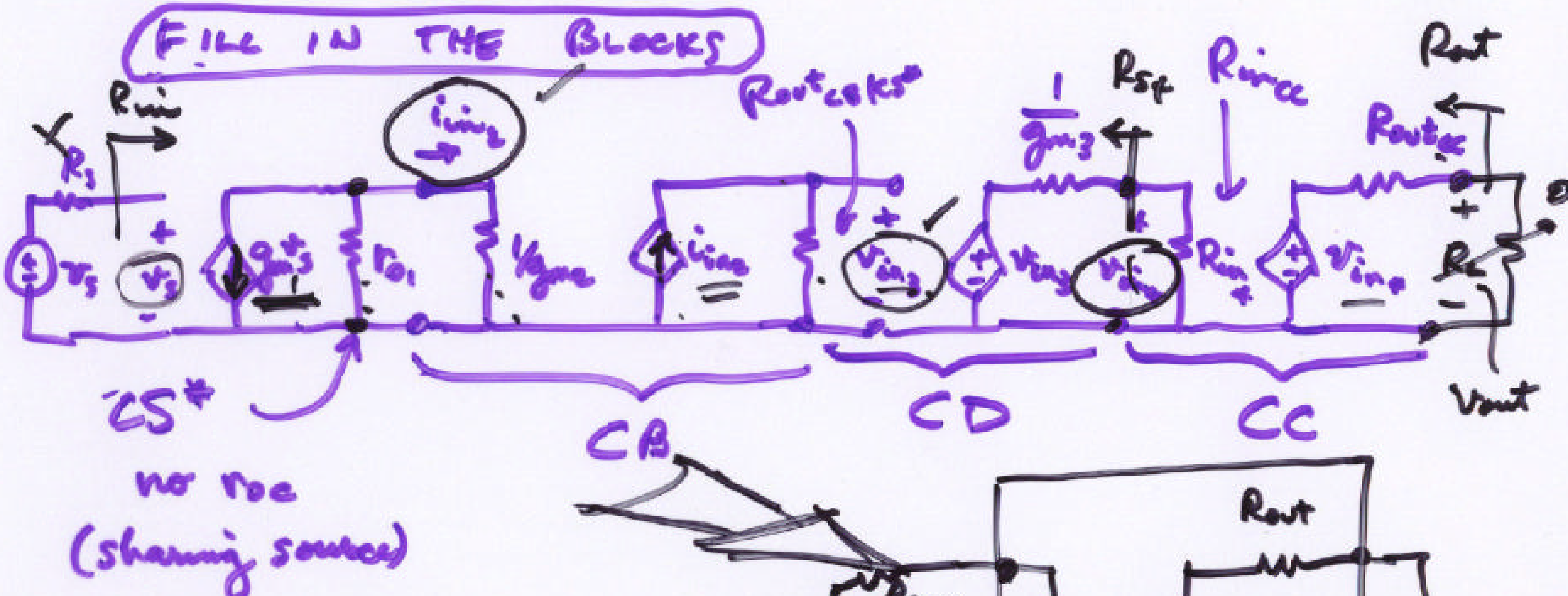
LAST TOPIC.

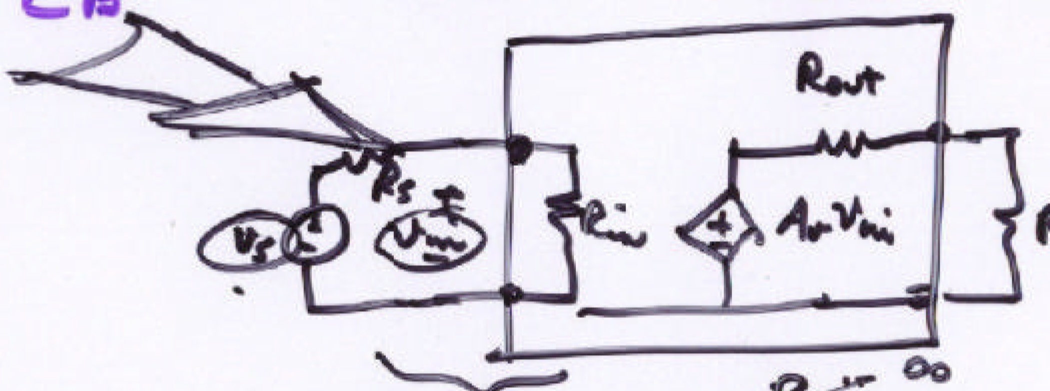
TO DISSECTION / SIMPLIFICATION ...

Second Approach: Find "Signal Path"



M_1, Q_2, M_3, Q_4 ...





VOLTAGE AMP

$A_v \uparrow$

$R_{in} = \infty$ GREAT ✓

$R_{out} = 0\Omega \cdots$ WANT

DIVIDER → $\frac{R_{in}}{R_S + R_{in}}$ ($R_{in} \to \infty$)

OUTPUT DIVIDER → $\frac{R_L}{R_L + R_{out}}$ ($R_{out} \to 0$)

$R_{out} = R_{out_{CC}} = \frac{1}{g_{m4}} + \frac{R_S \to 1/g_{m3}}{\beta_o}$ SMALL ✓

STEP 1

$$i_{in_2} = -g_{m1} v_s \left[\frac{r_{o1}}{r_{o1} + 1/g_{m2}} \right] \approx 1$$

STEP 2

$$v_{in_3} = i_{in_2} \cdot R_{out_{CS^*\text{-}CB}} \leftarrow \text{HUGE!}$$

STEP 3

$$v_{in_4} = v_{in_3} \left[\frac{R_{in_4}}{(1/g_{m3}) + R_{in_4}} \right] \approx 1$$

$R_{in_4} = R_{in_{CC}}$ BIG

$1/g_{m3}$ SMALL

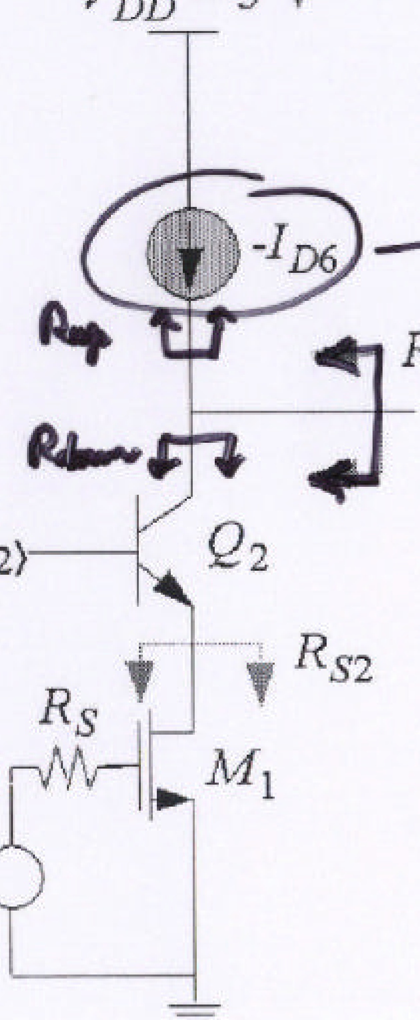
STEP 4 $v_{out} \leftarrow v_{in_4}$

FINDING

$$\left.\frac{v_{out}}{v_{in}}\right|_{R_S = 0,\ R_L = \infty} \cong -g_{m1} R_{out_{CS^*\text{-}CB}}$$

HUGE

Find Key Two-Port Parameters



NOT A C.G.!

Output resistance of cascode:

$$R_{out,CS^*/CB} = r_{oc} \,\|\, \left\{ r_{o2}\left(1 + g_{m2}\left(r_{\pi 2} \,\|\, R_{S2}\right)\right) \right\}$$ TABLE

$$r_{oc} = R_{up} = r_{o6}\left(1 + g_{m6} R_{S6}\right)$$

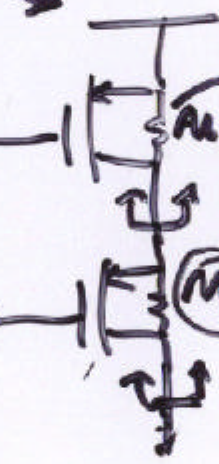
$$\approx r_{oc}\left(1 + g_{m6} r_{o7}\right)$$

$$R_{out,CS^*/CB} = r_{oc} \,\|\, \left(r_{o2}\beta_2\right)$$

$$= r_{oc}\left(1 + g_{m6} r_{o7}\right) \,\|\, \beta_o r_{o2}$$

$> 10\,M\Omega$, $> 10\,M\Omega$

$$\approx 5\,M\Omega.$$

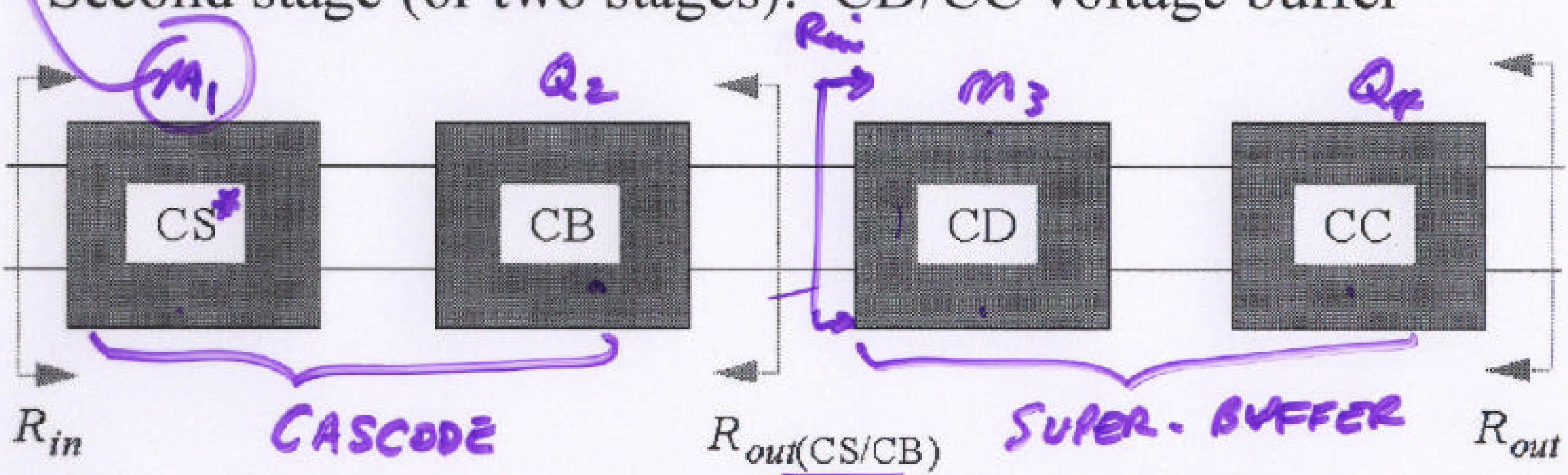


LOOK FOR THE LOW NUMBERS!!

Identifying the Stages

First stage (or two stages): CS/CB cascode

Second stage (or two stages): CD/CC voltage buffer

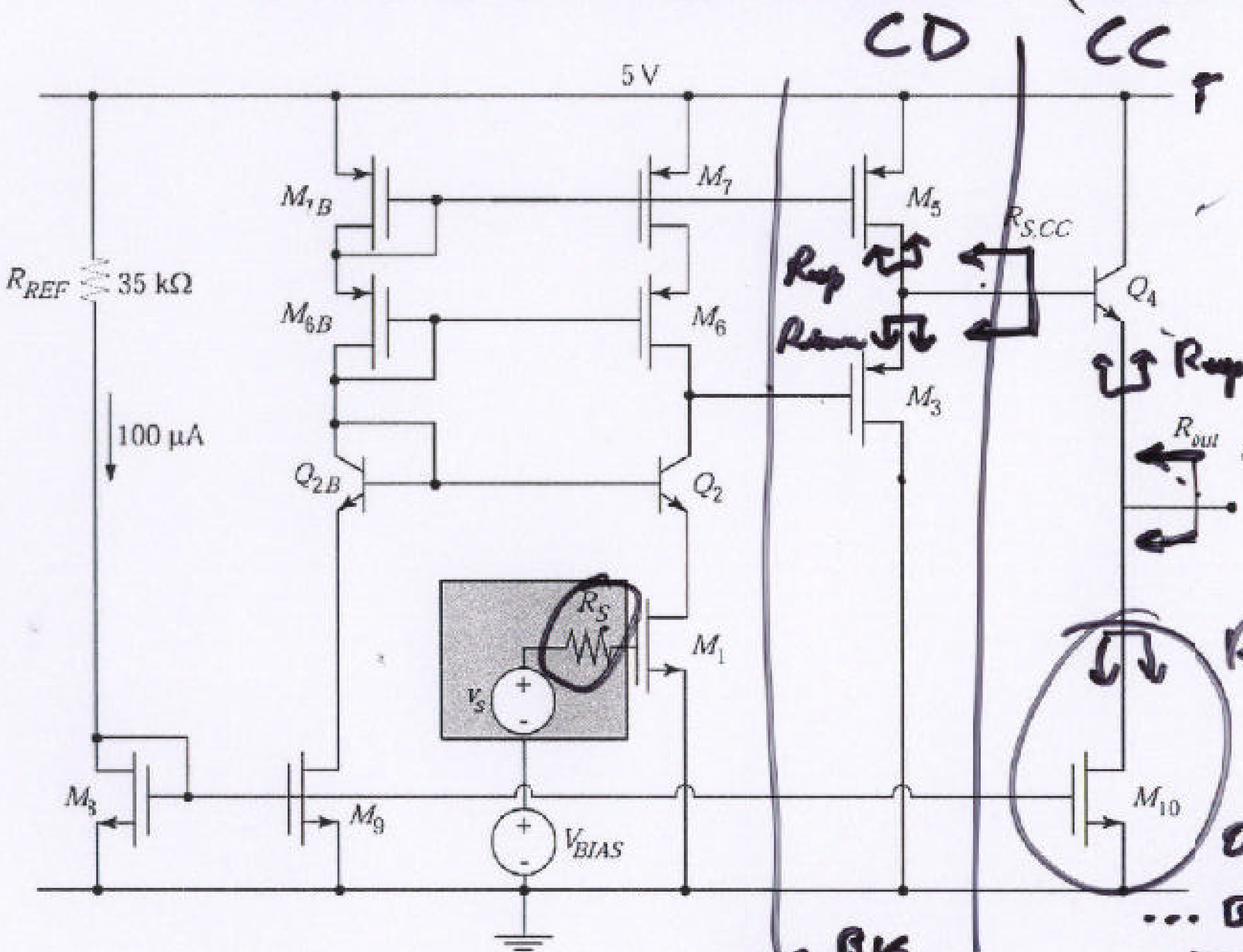


- Why does this make sense for a voltage amplifier?

$R_{out}|_{CS/CB}$ = HUGE

$R_{in}|_{CD} = \infty$

Two-Port Parameters (Cont.)



$R_{up} = \frac{1}{g_{m4}} + \frac{R_{S,CC}}{\beta_o}$ ← no R_L!

$R_{out} = \frac{v_t}{i_t}\Big|_{R_L \text{ removed}, R_S \text{ left}}$

OMITTED in the ckt. ... BIG

$R_{S,CC} = R_{out,CD} = r_{o5} \,||\, \frac{1}{g_{m3}} = \frac{1}{g_{m3}}$ (r_{oc} BIG)

Output Resistance and Voltage Gain

Source resistance of the CC stage is the output resistance of the CD stage (small)

$$R_{out} = R_{out,CC} = \frac{1}{g_{m4}} + \frac{R_{S,CC}}{\beta_o} = \frac{1}{g_{m4}} + \frac{1}{g_{m3}\beta_o} \approx \frac{1}{g_{m4}}$$

$R_{out,CD}$: $\frac{1/g_{m3}}{100} \sim \frac{1\,k\Omega}{100} = 10\,\Omega$; $\frac{1}{g_{m4}} \approx 100\,\Omega$.

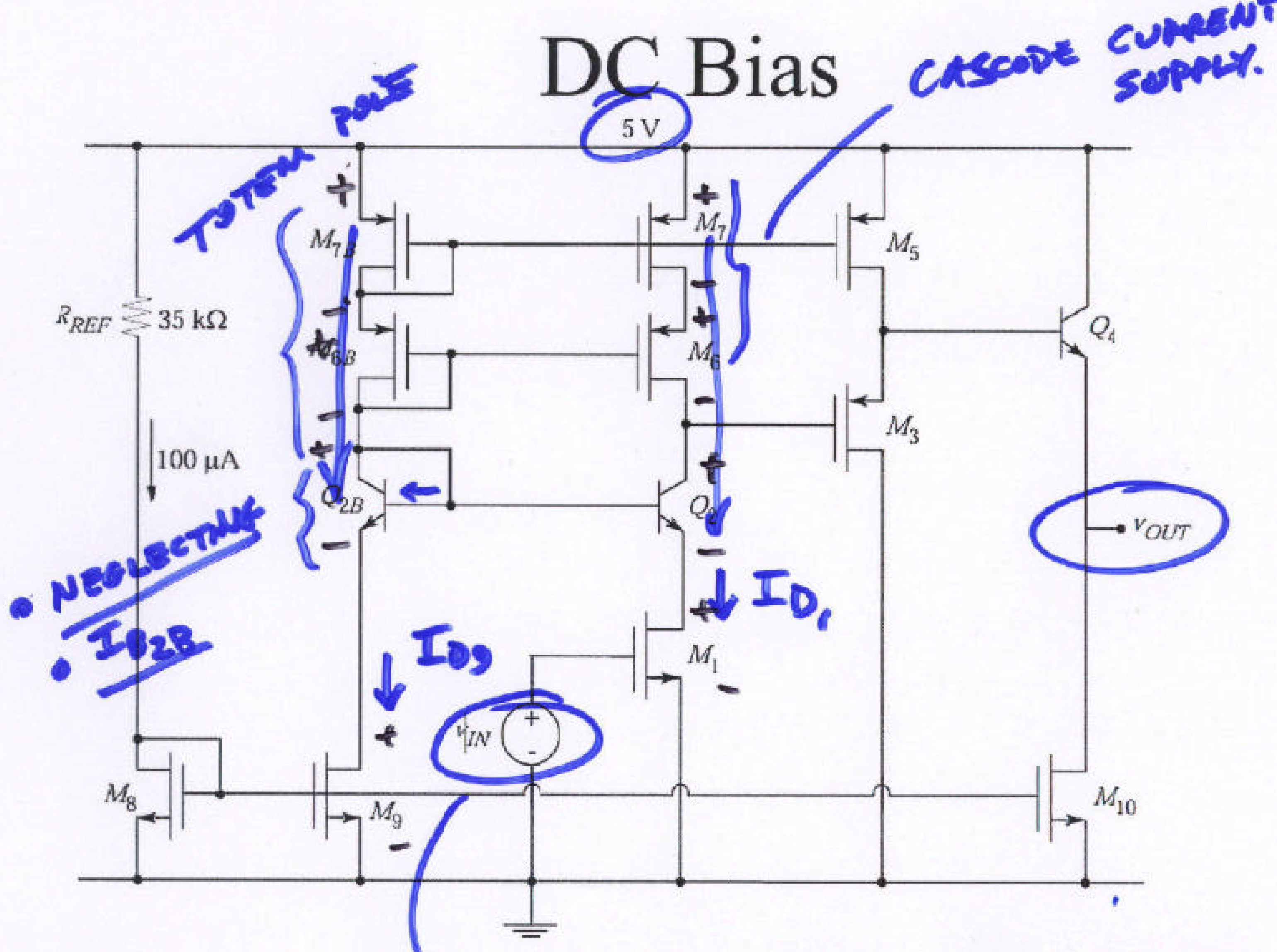
Open-circuit voltage gain A_v (last two stages have nearly unity gain):

$$A_v = -g_{m1}\left(\beta_o r_{o2} \,\|\, r_{o6}\left(1 + g_{m6} r_{o7}\right)\right)$$

R_{out,CS^*-CB}

$R_{out} \cong \frac{1}{g_{m4}} = \frac{1}{I_{C4}/V_{th}} = \frac{V_{th}}{I_{C4}}$

DC Bias



VIN SUCH THAT VOUT = 2.5V.

DC Bias (Cont.)

- Simplifying assumption: $V_{GSn} = 1.5V = V_{SGp}$

  LOOKING AHEAD

- Cascode current supply and totem pole: TO EE 140 .

  diode connected devices set both source-gate and source-drain voltages

  1ST ORDER

  2nd ORDER .

  select input bias voltage such that $I_{D1} = I_{D9}$

  devices M_1, Q_2, M_6, and M_7 must have same $|V_{DS}|$ or V_{CE} as M_9, Q_{2B}, M_{6B}, and M_{7B} (2nd order effect) → sometimes called "replica biasing"

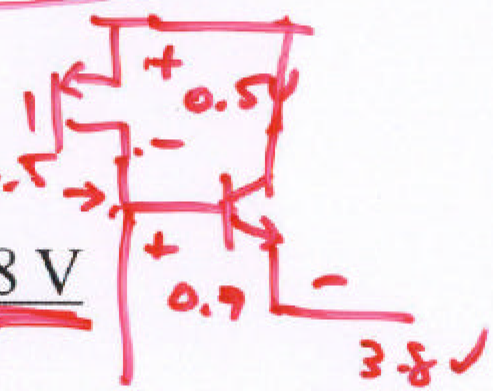
$$I_D = \mu_n C_{ox} \left(\frac{W}{2L}\right)(V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS})$$

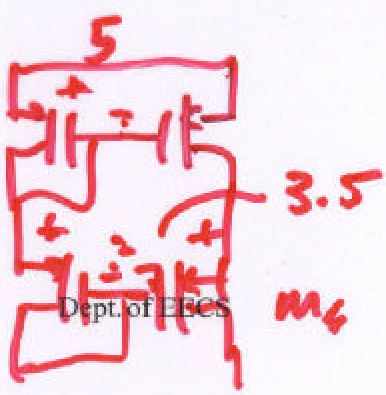
Output Swing: $V_{OUT,MAX}$

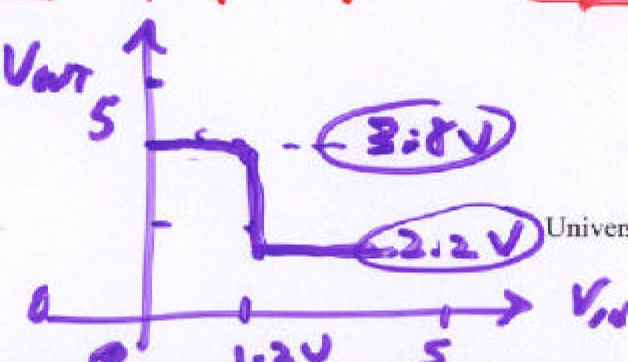
Maximum output voltage: Q_4, M_5, and M_6 are "suspects"

- Q_4 goes into saturation when $V_{CE4} = 0.1\text{ V} \rightarrow V_{OUT} = \underline{4.9\text{ V}}$
- M_5 goes triode when $V_{SD5} = 0.5\text{ V} \rightarrow V_{OUT} = \underline{3.8\text{ V}}$
- M_6 goes triode when $V_{SD6} = 0.5\text{ V} \rightarrow$

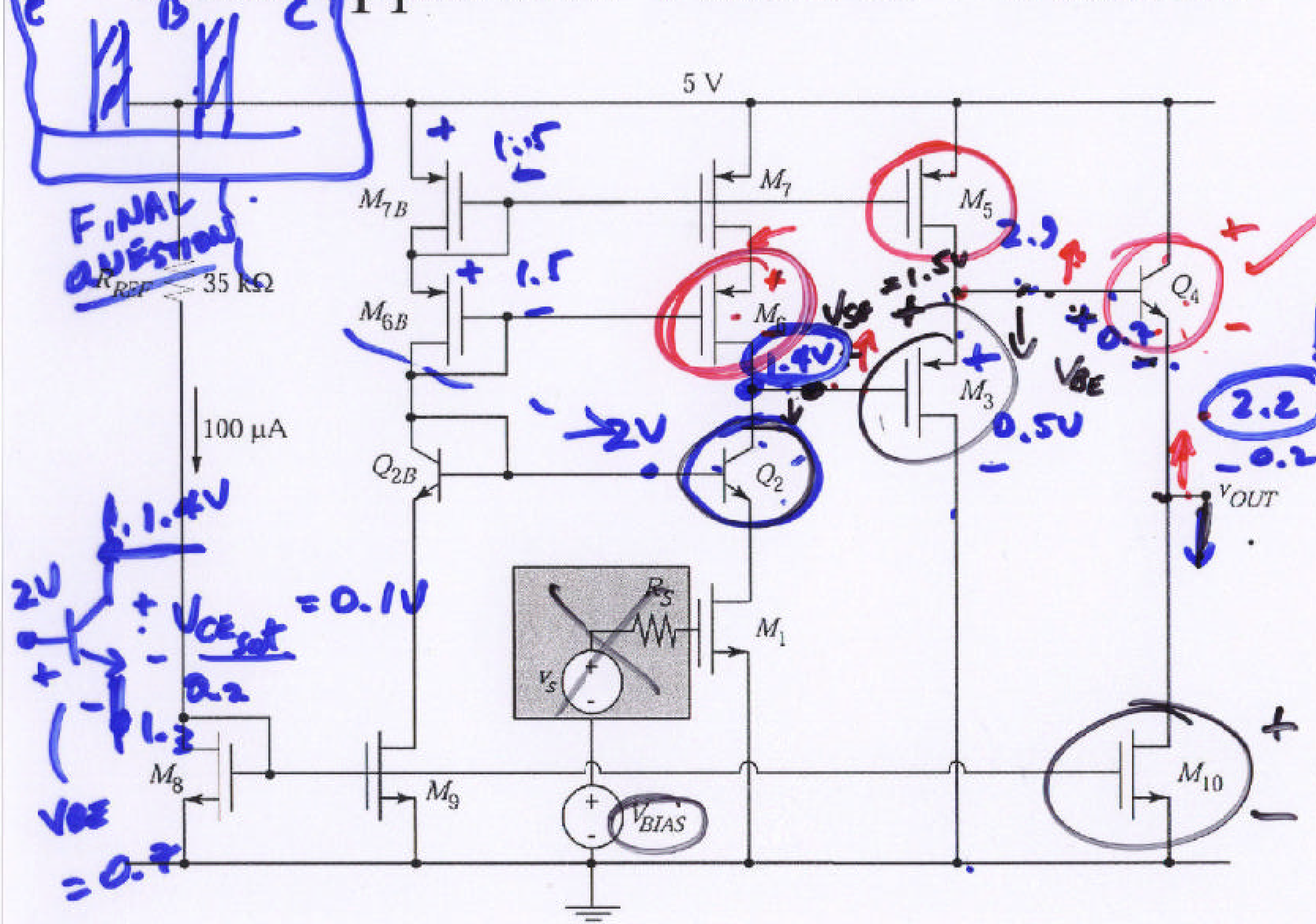
$$V_{OUT} = V_{S6} - 0.5\text{ V} + V_{SG3} - V_{BE4}$$
$$= 3.5 - 0.5 + 1.5 - 0.7\text{ V} = \underline{3.8\text{ V}}$$







First Approach: Find I & V Sources



IMPORTANT FOR EE 105

Output Swing: $V_{OUT,MIN}$

Minimum output voltage: M_{10}, M_3, and Q_2 are "suspects"

HUNTING ...

- ✓ M_{10} goes into triode when $V_{OUT} = \underline{0.5\text{ V}}$

  $V_{DS,10} = V_{DS10,SAT} = V_{GS10} - V_{Tn} = 0.5\text{V}$

- ✓ M_3 goes into triode when $V_{SD3} = 0.5\text{ V} \rightarrow$

  $V_{OUT} = 0.5\text{ V} - 0.7\text{ V} = \underline{-0.2\text{ V}}$

- ✓ Q_2 goes into saturation when $V_{CE2} = 0.1\text{ V}$

  or $V_{BC2} = 0.6\text{ V}$

  $$V_{OUT} = V_{B2} - V_{BC2} + V_{SG3} - V_{BE4}$$

  $$= 2\text{ V} - 0.6\text{ V} + 1.5\text{ V} - 0.7\text{ V}$$

  $$V_{OUT} = \underline{2.2\text{ V}}$$ WOW!