Microelectronic Devices and Circuits- EECS105
Final Exam

Tuesday, December 17, 2002
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College of Engineering
Department of Electrical Engineering and Computer Sciences

Your Name: ____________________________________________
(last)  (first)
Your Signature: __________________________________________

1. Print and sign your name on this page before you start.
2. You are allowed three, 8.5"x11" handwritten sheets. No books or notes!
3. Do every thing on this exam, and make your methods as clear as possible.
4. Always show the expression before you do the final calculation. A correct expression is
   worth 70% of the credit. A correct calculation gets you the remaining 30%.

Problem 1 ________  / 40
Problem 2 ________  / 25
Problem 3 ________  / 35
TOTAL ________  / 100

MOS Device Data
1 (you may not have to use all of these...)
µnCox = 50µA/V², µpCox = 25µA/V², Vtn = 1V, Lmin = 2µm, Vbs = 0.
λn = λp = 0.1V⁻¹ when L = 1µm, and it is otherwise proportional to 1/L.
Cox = 2.3F/µm², Cjn = 0.1F/µm², Cjp = 0.3F/µm², Cjsw = 0.5F/µm².
Covn = 0.5F/µm², Covp = 0.5F/µm², Cjswn = 0.5F/µm², Cjswp = 0.35F/µm².

BJT Device Data (you may not have to use all of these...)
βf = 100, Is = 10⁻¹⁷A, Vbeq = 0.7V, Vceq = 25V, τv = 50ps, Cov = 15F/µV, Vao = 0.7V,
Cov = 10F/µV, Vg = 2.0V

1 Except as indicated on the particular problem.

Problem 1 of 3: Answer each question briefly and clearly. (40 points)

1.1 Why circuit nodes with very high impedance matter in terms of frequency response?
   (4pts)

1.2 When we say that an amplifier stage is "broadband", what do we mean? (4pts)

1.3 Place check marks where appropriate (4pts)

<table>
<thead>
<tr>
<th>Amp Type</th>
<th>Check if Broadband</th>
<th>Check if high Rin</th>
<th>Check if high Rout</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS</td>
<td></td>
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<tr>
<td>CD</td>
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<td>CB</td>
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</table>
1.4 Choose the most appropriate answer (3pts)
The Open-Circuit Time Constant method can only work properly if:
- there is one dominant pole and no zeros
- there is an Open-Circuit connection
- there is no Miller Capacitance
- the Time is Constant.

1.5 In this class we talked about the Miller Approximation. Why is it “approximate”? (4pts)

1.6 Match the SPICE control cards (for the types of analysis) to the plots. (3pts)

(a) .DC  Figure 1
(b) .AC  Figure 2
(c) .TRAN Figure 3


1.7 For the n-channel MOS transistor shown below, please mark the two ends of the channel (near the source and near the drain) and indicate whether or not each must be inverted so that this device is in saturation. (4pts)

1.8 What is the “law of the junction” and when does it apply? (4pts)

1.9 What are the two (small signal) capacitive components of a forward biased junction? (4pts)

Symbol of first capacitance:
Verbal Definition:

Symbol of second capacitance:
Verbal Definition:
1.10 For each of these circuits, calculate the “no-signal” DC bias point at the nodes A and B, assuming that every MOS device is biased so that $V_{GS} = 1.5V$ and every BJT is biased so that $V_{BE} = 0.7V$. After you have done that, circle the circuit that is the “best” in terms of voltage swing at the input A and low frequency response, and explain where the other two fall short. (6pts)

2. Note that the input voltage should not be allowed to go over 5V during the operation of these amps. Assume that all the current sources in this question have a minimum voltage drop of 0.5V.

Problem 2 of 3: Answer each question briefly and clearly. (25 points)

2.1 Design a Common Base “current buffer” amplifier stage so that it meets the following constraints: Total $R_{out} > 20\Omega$ if $R_s = 50k\Omega$, and an absolute current gain $I_{out}/I_{in}$ greater than 0.99, when the stage output is shorted. (Use the simplified formulae that assume that $g_{m}r_{o} >> 1$, $r_{t} >> 1/g_{m}$, $r_{o} >> R_{L}$ and that the intrinsic current gain, $A_i = -1$.) (13pts)
2.2 Write the 2-port model of this amplifier, add the $C_\pi$ and $C_\mu$ parasitic capacitances at the proper locations and calculate $G$ (assume that $V_{BE} = -2V$). Then, assuming that $R_L = 0$ (shorted) find the pole of this amplifier and draw the magnitude and phase Bode plot of the current gain $\frac{i_{out}}{i_s}$ (12 pts).

2-port circuit with capacitors

<table>
<thead>
<tr>
<th>Expression</th>
<th>Value</th>
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<tbody>
<tr>
<td>$C_\pi$</td>
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Transfer function $\frac{i_{out}}{i_s}$ as a function of $\omega$.

Bode Plots

3. Please do a complete analysis of this transconductance amplifier as follows. Make sure that you use the transistor parameters shown below.

Problem 3 of 3: Answer each question briefly and clearly. (35 points)

3.1 Calculate $(W/L)_1$ of $M_1$ such that the small-signal transconductance $\frac{i_{out}}{v_s} = 1\text{mS}$. Assume $R_L = 0 \Omega$ for this part. (7pts)

2-port circuit with capacitors

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>$(W/L)_1$</td>
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3. Please make sure that you draw the 2-port, and not the small signal model.
3.2 Calculate the value of $V_{\text{BIAS}}$ using the $(W/L)_1$ calculated in part a so that $I_{\text{OUT}} = 0\,\text{A}$. (7pts)

3.3 Calculate the output resistance of this amplifier. (7pts)

3.4 Find the maximum and the minimum value of the output voltage, and state which transistor limits it in each case, when unloaded ($R_L = \infty$). (7pts)

<table>
<thead>
<tr>
<th>Expression</th>
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<tbody>
<tr>
<td>$V_{\text{BIAS}}$</td>
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<table>
<thead>
<tr>
<th>Expression</th>
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<tbody>
<tr>
<td>$V_{\text{OUT max}}$</td>
<td></td>
</tr>
<tr>
<td>Limited by:</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OUT min}}$</td>
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3.5 What is the maximum value of the load resistor $R_L$ at which the overall transconductance is degraded by 20% from the original value of 1mS? (7pts)

<table>
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<tbody>
<tr>
<td>$R_{L\text{ max}}$</td>
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