Context

In the last lecture, we discussed

- Structure of MOS transistors
  - Modes of operation

In this lecture, we will build models of MOS Transistors

- Voltage controlled resistor model
- I-V curve (Square-Law Model)
- Saturation model
- Small Signal Model (Linearized Model)
Reading

- We will be covering all of chapter 4 in the text
- Wednesday: Section 4.5→4.6
- Then we look at the analog characteristics of simple digital devices, 5.2→5.4
- Following that, we will cover PN diodes again, and develop small signal models: Chapter 6
- And following the midterm, we will start transistor amplifiers: Chapter 8

MOS operation

- An inversion mode MOS transistor operates by producing a sheet carriers just under the oxide
- The names source and drain are picked so that the inversion charge is larger at the source end
- Approximate inversion charge $Q_N(y)$: drain is higher than the source $\Rightarrow$ less charge at drain end of channel
Voltage controlled resistor mode

In the voltage controlled resistor mode, the gate→drain voltage is approximately the same as the gate→source voltage, so the charge is the same across the length of the gate. The current just depends on the velocity of that charge which is given by

\[ v = \mu E \]

Square law mode

As the drain voltage gets higher, the gate→drain voltage is not as large as the gate→source voltage, so the charge varying across the length of the gate, but it is still inverted at the drain end. The current can be approximately found by taking the average charge and field under the gate.
**Saturation**

As the drain voltage gets still higher, the gate→drain voltage is high enough so that the channel is pinched off somewhere before the drain connection, so the charge varying across the length of the gate, but it is still inverted at the drain end.

**Current stays constant during Saturation**

If the drain voltage is increased even further the pinch off region grows, but the current remains approximately constant.
Water hose analogy

Try this good physical analogy for pinch off—
Think of a rubber hose that you are trying to suction water through. As you increase the suction (increase the voltage to pull the electrons), the flow of water increases. However, if you increase the suction more, the hose begins to collapse (pinch off).

If it were to collapse entirely closed, the flow of water would stop, but then the pressure from the other end would build up and open up the pinched section again. So the steady state ends up with a region near the suction end which is pinched down and constraining the flow, and across this region most of the pressure drop occurs.

Increasing suction doesn’t increase the flow of water, but increasing the pressure at the other end does!

Inversion Charge at Source/Drain

The charge under the gate varies along the gate, but we are going to make a simple approximation, that the average charge is the average of the charge near the source and drain

\[ Q_N(y) \approx \frac{Q_N(y = 0) + Q_N(y = L)}{2} \]

\[ Q_N(y = 0) = -C_{ox}(V_{GS} - V_{Tn}) \]

\[ Q_N(y = L) = -C_{ox}(V_{GD} - V_{Tn}) \]

\[ V_{GD} = V_{GS} - V_{DS} \]
Average Inversion Charge

**Source End**  
\[ Q_N(y) \approx -\frac{C_{ox}(V_{GS} - V_T) + C_{ox}(V_{GD} - V_T)}{2} \]

**Drain End**  
\[ Q_N(y) \approx -\frac{C_{ox}(V_{GS} - V_T) + C_{ox}(V_{GS} - V_{SD} - V_T)}{2} \]

\[ Q_N(y) \approx -\frac{C_{ox}(2V_{GS} - 2V_T)}{2} - C_{ox}V_{SD} = -C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2}) \]

- Charge at drain end is lower since field is lower
- Notice that this only works if the gate is inverted along its entire length
- If there is an inversion along the entire gate, it works well because Q is proportional to V everywhere the gate is inverted

Drift Velocity and Drain Current

“Long-channel” assumption: use mobility to find \( v \)

\[ v(y) = -\mu_n E(y) \approx -\mu_n (-\Delta V / \Delta y) = -\frac{\mu_n V_{DS}}{L} \]

And now the current is just charge per area, times velocity, times the width:

\[ I_D = -WvQ_N \approx W\mu \frac{V_{DS}}{L} C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2}) \]

\[ I_D \approx W \frac{L}{\mu} C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2}) \]

Inverted Parabolas, I is proportional to the square of the drain-source voltage
Square-Law Characteristics

Boundary: what is $I_{D,SAT}$?

The Saturation Region

When $V_{DS} > V_{GS} - V_{Tn}$, there isn’t any inversion charge at the drain … according to our simplistic model

Why do curves flatten out?
**Square-Law Current in Saturation**

Current stays at maximum (where \( V_{DS} = V_{GS} - V_{Th} = V_{DS,SAT} \))

\[
I_D = \frac{W}{L} \mu C_{ox} (V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}
\]

\[
I_{DS,sat} = \frac{W}{L} \mu C_{ox} (V_{GS} - V_T - \frac{V_{GS} - V_T}{2})(V_{GS} - V_T)
\]

\[
I_{DS,sat} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_T)^2
\]

Measurement: \( I_D \) increases slightly with increasing \( V_{DS} \)
model with linear “fudge factor”

\[
I_{DS,sat} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})
\]

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**Pinching the MOS Transistors**

- When \( V_{DS} > V_{DS,sat} \) the channel is “pinched” off at drain end (hence the name “pinch-off region”)  
- Drain mobile charge goes to zero (region is depleted), the remaining electric field is dropped across this high-field depletion region  
- As the drain voltage is increases further, the pinch off point moves back towards source  
- Channel Length Modulation: The effective channel length is thus reduced \( \rightarrow \) higher \( I_{DS} \)
linear MOSFET Model

Channel (inversion) charge: neglect reduction at drain

Velocity saturation defines $V_{DS,SAT} = E_{sat} L = \text{constant}$

$V_{DS,SAT} = \frac{v_{sat}}{\mu_n}$

Drain current:

$I_{D,SAT} = -WvQ_N = -W(v_{sat})[-C_{ox}(V_{GS} - V_{Th})]$

$|E_{sat}| = 10^4 \text{ V/cm}, L = 0.12 \mu m \Rightarrow V_{DS,SAT} = 0.12 \text{ V}$

$\lambda_n V_{DS} = 1 + \frac{\lambda_n V_{DS}}{W}$

Gradual channel approximation

- We have played pretty fast and loose, using the average charge and average velocity, etc.
- A more accurate model of the physics includes the fact that the charge density under the gate and the velocity vary along the channel length
- The current at each point along the length of the device must be independent of position in steady state (no buildup of charge)

$I_D = -Wv_y(y)Q_N(y)$

- Where $I_D$ is the drain current, $y$ is the distance in the direction from the source to the drain, $v_y$ is the component of velocity in the source→drain direction, and $Q_N(y)$ is the charge density of the electrons under the gate
Gradual channel approximation -2

- For most FET’s the distances in y, the Source→Drain direction, are significantly larger than the distances in the x direction, (perpendicular to the oxide).
- If this assumption is not true, it’s called a short channel device.
- This means that the fields in the x direction are much stronger than the fields in the y direction.
- This is in the text, section 4.3, with the main difference from the simple approximation being the back gate effect, due to the variation in the depletion width to the body (substrate).

Effect of substrate voltage

- What is the effect of different substrate voltages?
  - Depletion width W changes
  - Need to account for different depletion region charge

\[
(V_{SB} = 0): \quad Q_B = \sqrt{2qN_Ae_S} - 2\phi_P
\]

\[
(V_{SB} \neq 0): \quad Q_B = \sqrt{2qN_Ae_S} - 2\phi_P + V_{SB}
\]
**Threshold voltage: general**

- General form (with substrate bias):

\[ V_T = V_{FB} - 2\phi_P - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \]

- Substituting the capacitance as a function of voltage:

\[ V_T = V_{T0} + \gamma\left(\sqrt{-2\phi_P + V_{SB}} - \sqrt{2\phi_P}\right) \]

Where:

\[ \gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}} \]

+ for NMOS
- for PMOS

**Threshold voltage, summary**

- If \( V_{SB} = 0 \) (no substrate bias):

\[ V_{T0} = V_{FB} - 2\phi_P - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \]

- If \( V_{SB} \neq 0 \) (non-zero substrate bias)

\[ V_T = V_{T0} + \gamma\left(\sqrt{-2\phi_P + V_{SB}} - \sqrt{2\phi_P}\right) \]

- Body effect (substrate-bias) coefficient:

\[ \gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}} \quad \text{(NMOS)} \]

- Threshold voltage increases as \( V_{SB} \) increases. The threshold voltage will also vary along the gate. This is called the body effect, or back gate effect.
**Threshold Voltage (NMOS vs. PMOS)**

<table>
<thead>
<tr>
<th></th>
<th>NMOS (p-substrate)</th>
<th>PMOS (n-substrate)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Fermi potential</td>
<td>$\phi_p &lt; 0$</td>
<td>$\phi_n &gt; 0$</td>
</tr>
<tr>
<td>Depletion charge density</td>
<td>$Q_B &lt; 0$</td>
<td>$Q_B &gt; 0$</td>
</tr>
<tr>
<td>Substrate bias coefficient</td>
<td>$\gamma &gt; 0$</td>
<td>$\gamma &lt; 0$</td>
</tr>
<tr>
<td>Substrate bias voltage</td>
<td>$V_{SB} &gt; 0$</td>
<td>$V_{SB} &lt; 0$</td>
</tr>
<tr>
<td>Threshold voltage (enhancement devices)</td>
<td>$V_T &gt; 0$</td>
<td>$V_T &lt; 0$</td>
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</tbody>
</table>

**Body effect**

- Voltage $V_{SB}$ changes the threshold voltage of transistor
  - For NMOS, Body normally connected to ground
  - For PMOS, body normally connected to $V_{cc}$
  - Raising source voltage increases $V_T$ of transistor
Threshold voltage adjustment

- Threshold voltage can be changed by doping the channel region with donor or acceptor ions
- For NMOS:
  - The threshold voltage is increased by adding acceptor ions
  - The threshold voltage is decreased by adding donor ions
- For PMOS:
  - The threshold voltage is increased by adding donor ions
  - The threshold voltage is decreased by adding acceptor ions
- Approximate change in threshold voltage:
  - Density of implanted ions = $N_i$ [cm$^{-2}$]

\[ \Delta V_{T0} = \frac{qN_i}{C_{ox}} \]

Channel Length Modulation

- As $V_{DS}$ is increased, the pinch-off point moves closer to source, shortening the channel length
- The drain current increases due to shorter channel

\[ L' = L - \Delta L \]

\[ I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 \left( 1 + \lambda V_{DS} \right) \]

\[ \lambda = \text{channel length modulation coefficient} \]
Review

Cutoff

\[ V_{GS} < V_{TN} \Rightarrow I_D = 0 \]
\[ V_{GS} < V_{TP} \Rightarrow I_D = 0 \]

Linear

\[ V_{GS} \geq V_{TN}, \quad V_{DS} < V_{GS} - V_{TN} \Rightarrow I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \]
\[ V_{GS} \leq V_{TP}, \quad V_{DS} > V_{GS} - V_{TP} \Rightarrow I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

Saturation

\[ V_{GS} \geq V_{TN}, \quad V_{DS} \geq V_{GS} - V_{TN} \Rightarrow I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]
\[ V_{GS} \leq V_{TP}, \quad V_{DS} \leq V_{GS} - V_{TP} \Rightarrow I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

Note: if \( V_{SB} \neq 0 \), need to calculate \( V_T \)

NMOS

- Slope due to Channel length modulation
- \( V_{GS} \) Steps
We now have reasonable mathematical models for NMOS and PMOS field effect transistors. In the next lecture, we will develop small signal models, allowing us to make equivalent circuits. The whole idea will be to make models that you can manipulate easily, and analyze and design circuits with FETs. We will also look at how SPICE models FETs for both small signal models and large signal models.