Lecture 29: Diode connected devices, mirrors, cascode connections

Prof. J. S. Smith

Context
Today we will be looking at more single transistor active circuits and example problems, and then starting multi-stage amplifiers

Lecture Outline
- Summary of single-transistor amplifiers
- Diode connected MOSFETs
- Current Mirrors
- Biasing Schemes

Single Stage Amplifiers
- Common-source is the only stage that provides both current and voltage gain
  - Miller effect limits high frequency response
- Common-drain can buffer a poor voltage source into a very good voltage source one
- Common-gate can buffer a poor current source into a very good current source, or replicate a current source into many current sources (current mirror)
NMOS pullup

- Rather than using a big (and expensive) resistor, let’s look at a NMOS transistor as an active pullup device.

Note that when the transistor is connected this way, it is not an amplifier, it is a two terminal device. When the gate is connected to the drain of this NMOS device, it will be in saturation, so we get the equation for the drain current:

\[ I_D = \left( \frac{W}{2L} \right) \mu_n C_{ox} (V_{SD} - V_{th}) \left( 1 + \lambda V_{DS} \right) \]

IV for NMOS pull-up

- The I-V characteristic of this pull-up device:

\[ I = \left( \frac{W}{L} \right) \mu_n C_{ox} (V_{DD} - V_{th}) \]

Small signal model

- So we have:

\[ I_D = \left( \frac{W}{2L} \right) \mu_n C_{ox} (V_{SD} - V_{th}) \left( 1 + \lambda V_{DS} \right) \]

The N channel MOSFET’s transconductance is:

\[ g_n = \frac{\partial I_D}{\partial V_{DS}} = \left( \frac{W}{L} \right) \mu_n C_{ox} \left( V_{SD} - V_{th} \right) \]

And so the small signal model for this device will be a resistor with a resistance:

\[ R = \left( \frac{1}{g_n} \right) \]

Active Load

- We can use this as the pullup device for an NMOS common source amplifier:

\[ I_{D1} = \left( \frac{W}{2L} \right) \mu_n C_{ox} \left( V_{gs1} - V_{th} \right) \]

\[ I_{D2} = \left( \frac{W}{2L} \right) \mu_n C_{ox} \left( V_{gs2} - V_{th} \right) \]

\[ V_0 = V_{DD} - V_{gs2} \]

\[ V_s = V_{DD} - V_{gs1} - \left[ \frac{2I_2}{\mu_n C_{ox} (W_1 / L_1)} \right] \]
Active Load

Since $I_2 = I_1$ we have:

$$V_0 = V_{DD} - V_{S2} - \frac{2I_1}{\mu_c C_{ox} (W_2/L_2)}$$

And since: $$V_{gs1} = V_i$$

$$V_0 = V_{DD} - V_{S1} - \frac{W_1/L_1}{W_2/L_2} (V_i - V_{th})$$

Behavior

- If the output voltage goes higher than one threshold below $V_{DD}$, transistor 2 goes into cutoff and the amplifier will clip.
- If the output goes too low, then transistor 1 will fall out of the saturation mode.
- Within these limitations, this stage gives a good linear amplification.

CMOS Diode Connected Transistor

- Short gate/drain of a transistor and pass current through it
- Since $V_{GS} = V_{DS}$, the device is in saturation since $V_{DS} > V_{GS}-VT$
- Since FET is a square-law (or weaker) device, the I-V curve is very soft compared to PN junction diode

Diode Equivalent Circuit

$$R_D = \left( \frac{dI_{OUT}}{dV_{OUT}} \right)_{I_{OUT}=0}^{-1} = \frac{V_i}{I_i}$$

$$R_D \approx \frac{1}{g_m}$$
The Integrated “Current Mirror”

- M₁ and M₂ have the same \( V_{GS} \).
- If we neglect CLM (\( \lambda = 0 \)), then the drain currents are equal.
- Since \( \lambda \) is small, the currents will nearly mirror one another even if \( V_{out} \) is not equal to \( V_{GS} \).
- We say that the current \( I_{REF} \) is mirrored into \( i_{OUT} \).
- Notice that the mirror works for small and large signals!

Currently Mirror as Current Source

- The output current of M₂ is only weakly dependent on \( V_{OUT} \) due to high output resistance of FET.
- M₂ acts like a current source to the rest of the circuit.

Small-Signal Resistance of \( I \)-Source

- The output current of M₂ is only weakly dependent on \( V_{OUT} \) due to high output resistance of FET.
- M₂ acts like a current source to the rest of the circuit.

Goal: increase \( r_{oc} \).
Approach: look at amplifier output resistance results … to see topologies that boost resistance.

Looks like the output impedance of a common-source amplifier with source degeneration.
Effect of Source Degeneration

- Equivalent resistance loading gate is dominated by the diode resistance … assume this is a small impedance.
- Output impedance is boosted by factor \((1 + g_m R_s)\).

Cascode (or Stacked) Current Source

Insight: \(V_{DS2} = \text{constant} \text{ AND } V_{GS2} = \text{constant}\)

Small-Signal Resistance \(r_{ss}\):

\[
R_s = \frac{V_d}{I} = (1 + g_m R_s) r_s
\]

\[
R_s = \frac{V_d}{I} = (1 + g_m R_s) r_s
\]

\[
R_s = g_m R_s \gg r_s
\]

Drawback of Cascode \(I\)-Source

Minimum output voltage to keep both transistors in saturation:

\[
V_{OUT_{MIN}} = V_{DS2_{MIN}} + V_{GS2_{MIN}}
\]

\[
V_{DS2_{MIN}} > V_{GSS2_{MIN}} - V_{T0} - V_{DSAT2}
\]

\[
I_{OUT} = \frac{V_{OUT_{MIN}}}{V_{GS2} + V_{GS4} - V_{T0}}
\]

Current Sinks and Sources

**Sink:** output current goes to ground

**Source:** output current comes from voltage supply
Current Mirrors

Idea: we only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.

The Integrated “Current Mirror”

- M₁ and M₂ have the same V_{GS}
- If we neglect CLM (λ=0), then the drain currents are equal
- Since λ is small, the currents will nearly mirror one another even if V_{out} is not equal to V_{GS1}
- We say that the current I_{REF} is mirrored into i_{OUT}
- Notice that the mirror works for small and large signals!

Current Mirror as Current Source

- The output current of M₂ is only weakly dependent on V_{OUT} due to high output resistance of FET
- M₂ acts like a current source to the rest of the circuit

Small-Signal Resistance of i-Source
**Improved Current Sources**

Goal: increase $r_{oc}$

Approach: look at amplifier output resistance results … to see topologies that boost resistance

Looks like the output impedance of a common-source amplifier with source degeneration

**Cascode (or Stacked) Current Source**

Insight: $V_{GS2} = \text{constant AND}$ $V_{DS2} = \text{constant}$

Small-Signal Resistance $r_{oc}$:

- $R_n \approx (1 + g_m R_s) r_o$
- $R_n \approx (1 + g_m r_o) r_o$
- $R_n \approx g_m r_o^2 \gg r_o$

**Effect of Source Degeneration**

- Equivalent resistance loading gate is dominated by the diode resistance … assume this is a small impedance
- Output impedance is boosted by factor $(1 + g_m R_s)$

**Drawback of Cascode I-Source**

Minimum output voltage to keep both transistors in saturation:

- $V_{OUT,MIN} = V_{DS4,MIN} + V_{DS2,MIN}$
- $V_{DS2,MIN} > V_{GS2} - V_T = V_{DSAT2}$
- $V_{GS2} > V_{DSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_T$
- $V_{OUT,MIN} = V_{GS2} + V_{GS4} - V_T$
Current Sinks and Sources

**Sink:** output current goes to ground

**Source:** output current comes from voltage supply

Current Mirrors

**Idea:** we only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.