Lecture 30:

Prof J. S. Smith

Context

In today’s lecture, by request, we will look at more single transistor active circuits and example problems, and start multi-stage amplifiers.
Reading

- We are starting on chapter 9, multi-stage amplifiers

Lecture Outline

- LED driver
- Peak detector
- CS amplifier with active pullup
  - small signal model
  - Frequency response
- Transimpedance Amplifier
- Source Follower
- Current Mirror
- Push-Pull Amplifier
- Multistage Amplifiers
Example: turn on an LED

- In this example, we have a low power CMOS output, 0-3 volts, and we want to turn on an LED when the output goes high.
- Use a NPN bipolar discrete transistor.
- First cut:

![Diagram](image1)

Problem: The transistor will go into saturation, drawing too much current from the CMOS output.
Problem: The current through the LED will not be limited, and it will burn out.

Put in a current limiting resistor

First, limit the current through the LED. The voltage drop across the resistor will be about 5 volts – 1.7 volts = 3.3 volts, so if we want a current of 10 milliamps through the LED, pick a resistor of 330 ohms.

![Diagram](image2)

The transistor will still saturate, pulling too much current from the CMOS.

If the beta of our transistor is about 100, then we would like a current of about 100 microamps into the base.
Put in a base resistor

If the voltage from the CMOS output is 5 volts when the output is high, the voltage drop from the base to the emitter is about .7 volts, and we want 100 microamps of current, so put in a 50 kilo-ohm resistor.

The resistor limits the current into the base, limiting the current draw from the CMOS output.

If you want to be sure the transistor stays out of saturation, pick a larger base resistor, (remember beta may vary!)

Example: find the peak of a signal

- In a communication circuit, you may not know the strength of a signal, so to detect data you need to scale your trigger by the peak value of the signal. A simple peak detector:

  Problem: the sample voltage will be .7 volts below the peak

  Problem: If there is a noise spike, the peak will be too high for a long time
Example: pull down and current limit

- Put in a pull down resistor to let the detected voltage decay in an $R_2C$ time, and a current limiting resistor to limit the pull up for short spikes. We will want $R_2C >>$ the bit time, and $R_1 << R_2$

\[ \text{Problem: the sample voltage will still be .7 volts below the peak, And this circuit might load the input too much} \]

Put in a voltage follower

- Lets put in a voltage follower, a common drain FET amplifier. The input is no longer loaded, and the voltage detected is close to the input peak, but not very accurate at low voltages. (if we used a common drain BJT, we would be closer to the input voltage). We will need $R_3 < R_1$

\[ \text{We will do this better later with a two stage amplifier and negative feedback} \]

We probably also need another voltage follower at the output.
Example: active pullup CS amplifier

- Begin the analysis by replacing M2 with a resistor of value $1/g_{m2}$
- Replace M1 with a current source of value $g_{m1}v_{in}$
- Note that this approach assumes:
  - $1/g_{m2} << r_o$
  - Low frequency operation
  - the body effect can be neglected in both transistors.

Small Signal Analysis

- The amplifier gain is the ratio of the ss output voltage to the ss input voltage:
  \[ A_c = \frac{v_{out}}{v_{in}} = -\frac{i_d}{g_{ds}} \frac{V_{gs}}{V_{gs}} = -g_{m1} \frac{g_{m2}}{V_{gs}} \]

- Taking into account the finite resistance of the FET ($r_o$) gives:
  \[ A_c = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m2} + r_o/\beta} = \frac{1}{\beta} \frac{g_{m1}}{r_o} \]
Frequency Response

To find the frequency response of the active pull up common source Amplifier, we need to put in the parasitic capacitances:

Use the Miller approximation to convert the GD capacitance to separate capacitances at the input and output.

CS Amplifier: Frequency Response

- Frequency dependence at the amplifier input
  \[ \omega_{Pin} = \frac{1}{R_s (C_{MI} + C_{g1})} \]
  \[ C_{MI} = g_{m1} \left( 1 + \frac{g_{m1}}{g_{m1}} \right) \]

- Frequency dependence at the amplifier output
  \[ \omega_{Pout} = \frac{1}{2\pi \frac{1}{2\pi \frac{C_{g2} + C_{MO} + C_{db1} + C_{db2}}{2\pi \frac{g_{m1}}{g_{m1}}}}} \]
  \[ C_{MO} = g_{m1} \left( 1 + \frac{g_{m1}}{g_{m1}} \right) \]
### Transimpedance Amplifier

The transimpedance is:

\[ A_R = \frac{v_{\text{out}}}{i_{\text{in}}} = -\frac{i_d}{g_{m2}} \frac{W_1}{W_2} L_3 \]

\[ = -\frac{W_1 L_3}{g_{m2} W_2 L_1} \]

### Source Follower

Gain:

\[ A_v = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{1}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} = \frac{1}{1 + \frac{g_{m1}}{g_{m2}}} = \frac{1}{1 + \frac{W_1 L_2}{W_2 L_1}} \]
Using a Current Source as a Load

Gain is given by:

\[ A_v = \frac{g_{m1}}{r_{o1} + r_{o2}} = \frac{-\sqrt{2\beta I_D}}{(A_1 + A_2) \cdot \sqrt{I_D}} \]

Notice that the gain can be adjusted by changing the bias current.

Current Mirror

Since \( V_{gs1} = V_{gs2} \)

\[ \frac{I_{D2}}{I_{D1}} = \frac{W_2 L_1}{W_1 L_2} \]
**Push-Pull Amplifier**

- Gain:

\[
A_v = \frac{v_{out}}{v_{in}} = \frac{-i_d \cdot \left( r_i || r_o \right)}{i_d \cdot \left( \frac{1}{g_m} \right) \cdot g_m} = -\left( g_m + g_m \right) \cdot \left( r_i \right)
\]

---

**Multistage Amplifiers**

Necessary to meet typical specifications for any of the 4 types

We have 2 flavors (NMOS, PMOS) of CS, CG, and CD and the npn versions of CE, CB, and CC (for a BiCMOS process)

What are the constraints?

1. Input/output resistance matching

2. DC coupling (no passive elements to block the signal)
Summary of Cascaded Amplifiers

General goals:

1. Boost the gain (except for buffers)
2. Optimize the input and output resistances:

<table>
<thead>
<tr>
<th></th>
<th>$R_{in}$</th>
<th>$R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage:</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Current:</td>
<td>0</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transconductance:</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Transresistance:</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Start: Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination “works”

\[ A_v = -G_{m1} \left( R_{in2} \parallel R_{out1} \right) \times (-G_{m2} R_{out2}) \]
\[ A_v = G_{m1} G_{m2} \left( R_{in2} \parallel R_{out1} \right) \left( R_{out2} \right) \]
Cascading stages

Input resistance: $\infty$

Voltage gain (2-port parameter):

$$A_v = -g_{m1} \left( r_{o1} \parallel r_{oc1} \right) \times g_{m2} \left( -r_{o2} \parallel r_{oc2} \right)$$

Output resistance:

$$R_{out} = \frac{1}{g_m + g_{mb}}$$

Multistage Current Buffers

Are two cascaded common-base stages better than one?

Input resistance: $R_{in} = R_{in1}$
**Two-Port Models**

\[ R_{\text{out}} = R_{\text{out}2} \cong r_{02} \left( 1 + g_{m2} r_{\pi2} \right) \left| R_{S2} \right| r_{oc2} \]

Output impedance of stage #1 (large)

\[ R_{\text{out}} \cong r_{02} \left( g_{m2} r_{\pi2} \right) \left| r_{oc2} = (\beta o r_{2o}) \right| r_{oc2} \]

**Common-Gate 2nd Stage**

\[ R_{\text{out}} = R_{\text{out}2} \cong r_{02} \left( 1 + g_{m2} R_{S2} \right) \left| r_{oc2} \right. \]

\[ R_{\text{out}} = R_{\text{out}2} \cong r_{02} \left( 1 + g_{m2} r_{\pi1} \right) \left| r_{oc1} \right| r_{oc2} \]
Second Design Issue: DC Coupling

Constraint: large inductors and capacitors are not available
Output of one stage is directly connected to the input of the next stage → must consider DC levels

Alternative CG-CC Cascade

Use a PMOS CD Stage: DC level shifts upward
CG Cascade: DC Biasing

Two stages can have different supply currents

Extreme case: $I_{B1AS2} = 0$ A

CG Cascade: Sharing a Supply

First stage has no current supply of its own $\rightarrow$ its output resistance is modified
The Cascode Configuration

Common source / common gate cascade is one version of a cascode (all have shared supplies)

DC bias:

Two-port model: first stage has no current supply of its own