Lecture 34: Designing amplifiers, biasing, frequency response

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Context
We will figure out more of the design parameters for the amplifier we looked at in the last lecture, and then we will do a review of the approximate frequency analysis of circuits which have a single dominant pole.

Reading
- Chapter 9, multi-stage amplifiers. The frequency analysis is in the first section of chapter 10, but we won’t go farther into chapter 10 for a while.

- The Lectures on Wednesday and Friday will be given by Joe and Jason, respectively. They will be doing several example problems.

Lecture Outline
- Example 1: Cascode Amp Design
- Example 2; CS NMOS->CS PMOS
- Review of frequency analysis (with a dominant pole)
Amplifier Schematic

Note that the backgate connection for $M_2$ is not specified: ignore $g_{m2b}$

Complete Amplifier Schematic

Goals: $g_{m1} = 1 \text{ mS}$, $R_{out} = 10 \text{ M}\Omega$

- Bias voltages derived from transistors under similar operating conditions to the transistors they supply
- Cascode current source for high $r_{oc}$
- CG output
- CS input, with low voltage gain

Current Supply Design

- High impedance current source means all of the small signal current goes to the load resistance, giving more SS voltage gain

- Output resistance goal requires large $r_{oc}$ for high gain → so we used a cascode current source

Totem Pole Voltage Supply

- DC voltages must be set for the cascode current supply transistors $M_2$ and $M_4$, as well as the gate of $M_2$
- $M_{2b}$ supplies the bias quiescent voltage for the CG stage
Miller Capacitance of Input Stage

Find the Miller capacitance for $C_{gd1}$

Input resistance to common-gate second stage is low $\Rightarrow$ gain across $C_{gd1}$ is small.

Two-Port Model with Capacitors

Miller capacitance: $C_M = (1 - A_{vC_{gd1}})C_{gd1}$

$A_{vC_{gd1}} \approx \frac{g_{m1}}{g_{m2}}$

Schematic

Goals: $g_{m1} = 1$ mS, $R_{out} = 10$ MΩ

Device Sizes

$M_1$: select $(W/L)_1 = 200/2$ to meet specified $g_{m1} = 1$ mS

$\Rightarrow$ find $V_{BIAS} = 1.2$ V

Cascode current supply devices: select $V_{SG} = 1.5$ V

$(W/L)_4 = (W/L)_B = (W/L)_3 = (W/L)_B = 64/2$
**Device Sizes**

\( M_2: \) select \((W/L)_2 = 50/2\) to meet specified \( R_{out} = 10 \text{ M\ Ohm} \)

\( \Rightarrow \) find \( V_{GS2} = 1.4 \text{ V} \)

Match \( M_2 \) with diode-connected device \( M_{2B} \).

Assuming perfect matching and zero input voltage, what is \( V_{OUT} \)?

**Two-Port Model**

Find output resistance \( R_{out} \)

\( \lambda_n = (1/20) \text{ V}^{-1}, \lambda_p = (1/50) \text{ V}^{-1} \) at \( L = 2 \mu m \) \( \Rightarrow \)

\( r_{on} = (100 \mu A / 20 \text{ V}^{-1})^{-1} = 200 \text{ k\ Ohm}, r_{op} = 500 \text{ k\ Ohm} \)

\[ g_m = \frac{2I_{DS}}{V_{GS2} - V_T} = \frac{2(100 \mu A)}{1.4V - 1W} = 500 \mu S \]

\[ g_m = \frac{2(-I_{DS})}{V_{GS2} + V_T} = \frac{2(100 \mu A)}{1.5V - 1W} = 400 \mu S \]

\[ R_{out} = r_{on} \parallel r_{on}(1 + g_{m2}R_{32}) = r_{on}(1 + g_{m3}R_{33}) \parallel r_{on}(1 + g_{m3}r_{on}) \]

**Output (Voltage) Swing**

Maximum \( V_{OUT} \)

Minimum \( V_{OUT} \)

**Voltage Transfer Curve**

Open-circuit voltage gain: \( A_v = \frac{v_{out}}{v_{in}} = -g_{m1}R_{out} \)

\[ = -10^3 \times 10^7 = \frac{dv_{out}}{dv_{in}} \text{ Ohm} \]

\( \approx -10,000 \)
Multistage Amplifier Design Example

Start with basic two-stage transconductance amplifier:

Why do this combination?

Quiescent level shifts

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
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<tbody>
<tr>
<td>CS</td>
<td>$\uparrow$ (typical)</td>
<td>$\uparrow$ (typical)</td>
</tr>
<tr>
<td>CG</td>
<td>$\uparrow$</td>
<td>$\uparrow$</td>
</tr>
<tr>
<td>CD</td>
<td>$\downarrow$ (known shift)</td>
<td>$\downarrow$ (known shift)</td>
</tr>
</tbody>
</table>

Current Supply Design

Assume that the reference is a “sink” set by a resistor

Must mirror the reference current and generate a sink for $i_{SUP2}$
Use Basic Current Supplies

DC Bias: Find Operating Points

Find $V_{BAS}$ such that $V_{OUT} = 0 \, \text{V}$

Device parameters:

- $\mu_n C_{ox} = 50 \, \mu\text{A}/\text{V}^2$
- $\mu_p C_{ox} = 25 \, \mu\text{A}/\text{V}^2$
- $V_{TH} = 1 \, \text{V}$
- $V_{TP} = -1 \, \text{V}$
- $\lambda_n = 0.05 \, \text{V}^{-1}$
- $\lambda_p = 0.05 \, \text{V}^{-1}$

Device dimensions (for “lecture” design):

- $(W/L)_n = 50/2$
- $(W/L)_p = 80/2$

Complete Amplifier Topology

Finding $R_{REF}$

Require $I_{REF} = -I_{D3} = 50 \, \mu\text{A}$

\[
V_{SG3} = -V_{TP} - \frac{-2I_{D3}}{\mu_p C_{ox} (W/L)_p}
\]

\[
V_{SG3} = -(1)(-1) + \frac{2\times 50 \mu\text{A}}{25\mu\text{A} (80/2)} = 1 + \frac{4}{40} = 1.32 \, \text{V}
\]

\[
I_{REF} = 50 \mu\text{A} = \frac{[V' - V_{SG3} - V']}{R_{ref}}
\]

\[
50 \mu\text{A} = \frac{[2.5 - 1.32] - [2.5]}{R_{ref}} \Rightarrow R_{ref} = 74 \, \text{k}\Omega
\]
DC Operating Point

\[ I_{REF} = 50 \ \mu A \]

\[ V_{MOS} = 2.5 \ \text{V} \]

\[ V_{BLIS} = \sqrt{2 I_D \frac{2 I_D}{V_{GS}^2 (W/L)}} = 1 + \frac{100 \mu A}{50 \mu A (V/2)^2} \approx 2 \ \text{V} \]

Small-Signal Device Parameters

Transistors \( M_1 \) and \( M_2 \)

\[ g_{m1} = 350 \ \mu S \quad r_{o1} = 400 \ \text{k} \Omega \]

\[ g_{m2} = 315 \ \mu S \quad r_{o2} = 400 \ \text{k} \Omega \]

Current supplies \( i_{SUP1} \) and \( i_{SUP2} \)

\[ r_{ac1} = r_{ac4} = 400 \ \text{k} \Omega \]

\[ r_{ac2} = r_{ac6} = 400 \ \text{k} \Omega \]

Two-Port Model

Find \( G_m = \frac{i_{out}}{v_{in}} \)

Output Voltage Swing

\[ V^* = 2.5 \ \text{V} \]

Transistors \( M_2 \) and \( M_6 \) will limit the output swing
Limits to Output Voltage

\[ M_6 \] will leave saturation when \( V_{\text{OUT}} \) drops to:

\[
V_{\text{OUT},\text{MIN}} = V^+ + V_{\text{SDS},\text{sat}} = -2.5 + \frac{2I_{D6}}{\mu C_{\text{ox}}(W/L)_6}
\]

\[ V_{\text{OUT},\text{MIN}} = -2.5 + 0.28 = -2.22 \text{ V} \]

\( M_2 \) will leave saturation when \( V_{\text{OUT}} \) rises to:

\[
V_{\text{OUT},\text{MAX}} = V^+ - V_{\text{SDS},\text{sat}} = 2.5 - \frac{2(-I_{D2})}{\mu C_{\text{ox}}(W/L)_2}
\]

\[ V_{\text{OUT},\text{MAX}} = 2.5 - 0.32 = 2.18 \text{ V} \]

What about \( M_4 \)?

Output Current Limits

- Positive output current (negative \( V_{\text{OUT}} \))

\[
i_{\text{OUT,MAX}} = i_{D6} - (0) = 50 \mu A = -V_{\text{OUT,MIN}} / R_L
\]

\[ V_{\text{OUT,MIN}} = -(50 \mu A)(25 \Omega) = -1.25V \]

(less negative than limit set by saturation of \( M_6 \))

- Negative output current (positive \( V_{\text{OUT}} \))

No limit on current from \( M_2 \), so voltage swing sets current limit

\[
i_{\text{OUT,MIN}} = -V_{\text{OUT,MAX}} / R_L = -(2.18V / 25\Omega) = -87.2 \mu A
\]

Output Current Swing

Load resistor: pick \( R_L = 25 \text{ k}\Omega \)

Output current:

\[ i_{\text{OUT}} = -V_{\text{OUT}} / R_L \]

\[ i_{\text{OUT}} = i_{D6} - (-i_{D2}) \]

Limits: asymmetrical

\( M_2 \): can increase \(-i_{D2}\)

\( M_6 \): can’t increase \( i_{D6} \)

Transfer Curves (for \( R_L = 25 \text{ k}\Omega \))

Loaded voltage gain:

\[ \frac{v_{\text{OUT}}}{v_{\text{IN}}} = \left( g_{m1}(R_{\text{out}}) \right) \left( g_{m2}(R_{\text{out}} + R_L) \right) = 490 \]

Loaded transconductance:

\[ \frac{i_{\text{OUT}}}{v_{\text{IN}}} = (-g_{m1}) \left( g_{m2}(R_{\text{out}} + R_L) \right) = -19.5 \text{ mS} \]
Review: Frequency Resp of Multistage Amplifiers

- We have a systematic technique to study amplifier performance (derive transfer function, study poles/zeros/Bode plots).
- In most cases, the systematic approach is too cumbersome.
- We have a good qualitative understanding of circuit performance (e.g., CS suffers from Miller effect, CD and CG are wideband stages ...)
- Open Circuit Time Constants: Analytical technique is capable of estimating only the dominant (lowest) pole ... for a restricted class of amplifiers.

The Special Case

The transfer function can have no zeroes and must have a dominant pole \( \omega_1 << \omega_2, \omega_3, \ldots, \omega_n \)

\[
H(j\omega) = \frac{H_o}{(1 + j\omega/\omega_1)(1 + j\omega/\omega_2)(1 + j\omega/\omega_n)}
\]

Factor denominator:

\[
H(j\omega) = \frac{H_o}{(1 + j\omega/\omega_1)(1 + j\omega/\omega_2)(1 + j\omega/\omega_n)}
\]

Approximating the Transfer Function

Multiply out denominator:

\[
H(j\omega) = \frac{H_o}{1 + j\omega/\omega_1}(1 + j\omega/\omega_2)(1 + j\omega/\omega_n)
\]

Since \( \omega_1 << \omega_2, \omega_3, \ldots, \omega_n \)

\[
b_1 = \frac{1}{\omega_1} + \frac{1}{\omega_2} + \ldots + \frac{1}{\omega_n} \approx \frac{1}{\omega_1}
\]

How to Find \( b_1 \)?


Result: \( b_1 \) is the sum of open-circuit time constants \( \tau_i \) which can be found by considering each capacitor \( C_i \) in the amplifier separately and finding the Thévenin resistance \( R_{\tau_i} \) of the network from the capacitor’s point of view

\[
\tau_i = R_{\tau_i} C_i
\]

\[
b_1 = \sum_{i=1}^{\infty} R_{\tau_i} C_i \rightarrow \omega_1 \approx \frac{1}{\sum_{i=1}^{\infty} R_{\tau_i} C_i}
\]
Finding the Thévenin Resistance

1. Open-circuit all capacitors (i.e.; remove them)

2. For capacitor $C_i$, find the resistance $R_{Ti}$ across its terminals with all independent sources removed (voltages shorted, currents opened) … might need to apply a test voltage and find the current in some cases.

*Insight for design:* the bandwidth of the amplifier will be limited by the capacitor that contributes the largest

$$\tau_i = R_{Ti} C_i \Rightarrow$$ not necessarily the largest $C_i$