Lecture 41: Review Frequency Response, FET physics

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Q&A about the final

Q: Are differential amplifiers going to be on the exam?  
A: No, there will not be a differential amplifier question.  
Q: Do we need to know a lot of device physics for BJTs?  
A: No, there won’t be any BJT physics  
Q: Will there be any BJT circuits questions on the exam?  
A: No, the exam will not have any BJT transistor problems.  
Q: How much of the material from before Midterm 1 will be tested in detail?  
A: Material before midterm 1 is fair game.  
Q: Also, are we responsible for Chapter 5 i.e.- digital circuits?  
A: No, nothing specifically on digital circuits or from chapter 5.

Final Exam

- Covers the course from the beginning  
- Date/Time: SATURDAY, MAY 15, 2004  8-11A  
- Location: BECHTEL auditorium  
- One page (Two sides) of notes

Last Week of Lecture

- Monday:  
  - Review of Frequency domain analysis of linear circuits, Bode plots.  
- Wednesday:  
  - Frequency Response  
  - Semiconductor materials, FET physics and models  
- Friday:  
  - Review of active linear circuits, amplifiers wrapup
**Frequency response: CS**

- When we take into account a finite source impedance in a common source amplifier, the capacitances will reduce the voltage swing at the gate at high frequencies.

**Parasitic Capacitances**

The transfer function will be a low pass filter, with a pole at the frequency determined by the source resistance and the capacitance.

**High frequency zero**

At very high frequencies, the gain flattens out again, because the capacitor couples from the gate to the drain directly, as a passive circuit.

**Magnitude Bode Plot**

- Low frequency gain
- Pole
- Unity current gain
- Zero
- $\omega_p$
- $\omega_f$
- $\omega_z$
**Miller Capacitance** $C_M$

Effective input capacitance:

$$Z_m = \frac{1}{j\omega C_M} = \frac{1}{\left(1 - A_{v,CM}^\prime\right)} \times \frac{1}{j\omega C_{gd}} = \frac{1}{j\omega \left(1 - A_{v,CM}^\prime\right) C_{gd}}$$

**Some Examples**

Common source (emitter) amplifier:

$A_{v,CM}^\prime =$ Negative, large number (-100)

$$C_M = \left(1 - A_{v,CM}^\prime\right) C_{gd} \approx 100 C_{gd}$$

→ Miller Multiplied Cap has Detrimental Impact on bandwidth

Common drain (collector) amplifier:

$A_{v,CM}^\prime =$ Slightly less than 1

$$C_M = \left(1 - A_{v,CM}^\prime\right) C_{gr} \approx 0 C_{gr}$$

“Bootstrapped” cap has negligible impact on bandwidth!

**Frequency response**

**Open Circuit Time Constants**

- For a circuit dominated by a single pole
- For each capacitor in the circuit you calculate an equivalent resistor “seen” by capacitor and form a time constant $\tau = R_i C_i$
- The dominant pole then is the sum of these time constants in the circuit

$$\omega_{p,dom} = \frac{1}{\tau_1 + \tau_2 + \cdots}$$
Equivalent Resistance “Seen” by Capacitor

- For each “small” capacitor in the circuit:
  - Open-circuit all other “small” capacitors
  - Short circuit all “big” capacitors
  - Turn off all independent sources
  - Replace cap under question with current or voltage source
  - Find equivalent input impedance seen by cap
  - Form RC time constant

Remember…

For a given capacitor:
- If the frequency is high compared to the 1/RC for the capacitor in that location in the circuit
  - That Capacitor can be modeled as a short
- If the frequency is low compared to the 1/RC for the capacitor in that location in the circuit
  - That Capacitor can be modeled by an open circuit.

Common-Drain Amplifier

\[ I_{DS} = \mu C_{on} \frac{W}{L} \frac{1}{2} (V_{DS} - V_T)^2 \]

\[ V_{DS} = V_T + \sqrt{\frac{2I_{DS}}{\mu C_{on} \frac{W}{L}}} \]

Weak \( h_{DS} \) dependence

CD Voltage Gain

\[ \frac{v_{out}}{v_{in}} \approx \frac{g_m}{g_{nb} + g_m} \approx 1 \]
CD Output Resistance

Sum currents at output (source) node:

\[ R_{\text{out}} = r_o \parallel r_{oc} = \frac{V_T}{I_i} \]

\[ i = g_a V_T + g_{ob} V_T \]

\[ R_{\text{out}} = \frac{1}{g_a + g_{ob}} \]

CD Output Resistance (Cont.)

\( r_o \parallel r_{oc} \) is much larger than the inverses of the transconductances \( \rightarrow \) ignore

Function: a voltage buffer
- High Input Impedance
- Low Output Impedance

Add capacitors

Procedure:
- Start with small-signal two-port model
- Add device (and other) capacitors

Common Gate Amplifier

DC bias:

\[ I_{SUP} = I_{BIAS} = I_{DS} \]
CG → Current buffer

\[ i_{\text{out}} = i_d = -i_i \]

\[ A_i = -1 \]

CG Output Resistance

\[ R_{\text{out}} \approx r_{oc} \parallel \left[ r_o + g_m r_s R_s \right] = r_{oc} \parallel \left[ r_o (1 + g_m R_s) \right] \]

CG Input Resistance

\[ V_{gs} = -V_i \]

We found the approximation:

\[ R_m \approx \frac{1}{g_m + g_{wb}} \]

CG Two-Port Model

The function of the CG amp was a current buffer:
- Low input impedance
- High output impedance

The only parasitic capacitances are directly across the input and output: frequency response can be directly determined.
**Single-Stage Amp Frequency Response**

- CS, CE: suffer from Miller-magnified capacitor for high-gain case
- CD, CC: Miller transformation → null capacitor → “wideband stage”
- CG, CB: no Millerized capacitor → wideband stage (for low load resistance)

**Electrostatics summary**

- In one dimension, the electrostatics equations reduce to the E field growing or diminishing depending on the net charge:
  \[
  E(x) = E(x_0) + \int_{x_0}^{x} \frac{\rho(x')}{\varepsilon} \, dx'
  \]

  Which can also be written as a differential equation for the potential (voltage).
  \[
  \frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon}
  \]

**Net Charge**

- The net charge density in a semiconductor is calculated from the number of charge carriers and fixed charges in a location:
  \[
  \rho(x) = q (p(x) - n(x) + N_d(x) - N_a(x))
  \]

- If a region does not have the right number of electrons or holes to cancel the amount of charge from the dopants, the fixed charge of the dopants will influence the electric fields.

**Thermal Equilibrium**

- A couple fundamental principles about thermal equilibrium:
  - The energy that electrons are filled up to (the Fermi level) is the same everywhere.
  - The current is zero at all points.

- So when we look at this:

- We know that the electrons are feeling a force due to the electric field, but there is also diffusion which contributes a exactly canceling amount of current! This means the diffusion constant can always be found in terms of mobility...
Total Current and Boundary Conditions

- The total current is given by the sum of drift and diffusion:

\[ J = J_{\text{drift}} + J_{\text{diff}} = q\mu n E + qD \frac{dn}{dx} \]

- In resistors, the carriers are approximately uniform and the second term is nearly zero.

- In metals, there are a very large number of carriers, in very uniform concentration, and the conduction current is quite linear with \( E \) (ohmic).

Note: Band edge diagrams

- We will often draw a diagram of the valence and conduction band edges as a function of position.

- The energy at the band edge corresponds to the potential energy that an electron has (which is the negative of the electrostatic potential). Thus the slope of the band edge with distance is the electric field.

Transport summary

- The number of majority carriers in a neutral semiconductor goes according to the number of Donors or acceptors, and the number of minority carriers is found from the law of mass action.

  - For n-type material: \( n \approx N_d - N_a \) \( p \approx \frac{n_i^2}{p} \)

  - For p-type material: \( p \approx N_a - N_d \) \( n \approx \frac{n_i^2}{p} \)

- The total current is given by the sum of drift and diffusion:

\[ J = J_{\text{drift}} + J_{\text{diff}} = q\mu n E + qD \frac{dn}{dx} \]

The Einstein relation (diffusion)

- Since the diffusion process has a fundamental relationship to the mobility in an electric field, we can find the diffusion constant in terms of the mobility \( \mu \).

\[ D_n = \left( \frac{kT}{q} \right) \mu_n \]
Carrier Concentration Versus Potential

- The carrier concentration is thus a function of potential $n_i(x) = n_i e^{(x)/V_p}$
- Check that for zero potential, we have intrinsic carrier concentration (reference).
- If we do a similar calculation for holes, we arrive at a similar equation $p_i(x) = p_i e^{-(x)/V_p}$
- Note that the law of mass action is upheld

Total Charge in Transition Region

- To solve for the electric fields, we need to write down the charge density in the transition region:

$$\rho_p(x) = q(p_i - n_i + N_d - N_a)$$

- In the p-side of the junction, there are very few electrons and only acceptors:

$$\rho_p(x) \approx \rho(x) \quad -x_p < x < 0$$

- Since the hole concentration is decreasing on the p-side, the net charge is negative:

$$N_a > p_0 \quad \rho_p(x) < 0$$

PN Junction Fields

<table>
<thead>
<tr>
<th>p-type</th>
<th>n-type</th>
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<tbody>
<tr>
<td>$N_a$</td>
<td>$N_d$</td>
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Charge on N-Side

- Analogous to the p-side, the charge on the n-side is given by:

$$\rho_n(x) \approx q(-n_i + N_d) \quad 0 < x < x_{ni}$$

- The net charge here is positive since:

$$N_d > n_0 \quad \rho_n(x) > 0$$
Accumulation

- Under a higher forward bias, the mobile carriers get pushed up against the barrier, and start to pile up in a thin layer there, the *accumulation layer*
- The bias where accumulation starts is called *flat band*

Inversion

- Under a strong reverse bias, the potential at the surface of the semiconductor, next to the oxide, can get high enough so that *holes* start to accumulate in a thin layer, the *inversion layer*
If the semiconductor is p type, rather than n type:
  - The depletion has a negative fixed charge
  - An inversion layer is an accumulation of electrons
NMOS, above threshold

N+ semiconductor

“Metal”

Insulator

Fermi level

P type semiconductor

Electrons

P type substrate

NMOS

Observed Behavior: $I_D-V_{GS}$

- Current zero for negative gate voltage
- Current in transistor is very low until the gate voltage crosses the threshold voltage of device (same threshold voltage as MOS capacitor)
- Current increases rapidly at first and then it finally reaches a point where it simply increases linearly

Variable resistor

- If the Source and Drain voltages are about the same, then the inversion charge is about the same at different positions along the gate.
- The amount of charge under the gate is that which was calculated for the MOS capacitor.
- The current from the source to the drain is given by the amount of charge, the mobility of the carriers, and the component of the electric field from the source to the drain.

Saturation

- As the Source-Drain voltage is increased, there will be a significant change in the charge at different distances along the gate.
- As the voltage across the device at the drain end is below threshold, the current is pinched off.
- If there is no current out the drain end, however, the current due to the carriers which are available from the source cause the voltage to be closer to that of the source.
- These two effects cause a small region to form near the drain which limits the current. This is called saturation.
Pinching the MOS Transistors

- When $V_{DS} > V_{DS,sat}$, the channel is “pinched” off at drain end (hence the name “pinch-off region”)
- Drain mobile charge goes to zero (region is depleted), the remaining electric field is dropped across this high-field depletion region
- As the drain voltage is increases further, the pinch off point moves back towards source

Observed Behavior: $I_D - V_{DS}$

- For low values of drain voltage, the device is like a resistor
- As the voltage is increases, the resistance behaves non-linearly and the rate of increase of current slows
- Eventually the current stops growing and remains essentially constant (current source)

“Linear” Region Current

- If the gate is biased above threshold, the surface is inverted
- This inverted region forms a channel that connects the drain and gate
- If a drain voltage is applied positive, electrons will flow from source to drain

MOSFET “Linear” Region

- The current in this channel is given by $I_{DSS} = -WV_{th}Q
- The charge proportional to the voltage applied across the oxide over threshold $Q_S = C_{ox}(V_{GS} - V_{th})$
- $V_{DS} = -WV_{th}C_{ox}(V_{GS} - V_{th})$
- If the channel is uniform density, only drift current flows
  $v_j = -\mu E_j$, $E_j = \frac{V_{DS}}{L}$
  $I_{DS} = \frac{W}{L} \mu C_{ox}(V_{GS} - V_{th})V_{DS}$ $V_{GS} > V_{th}$ $V_{DS} \approx 100 \text{mV}$
MOSFET: Variable Resistor

- Notice that in the linear region, the current is proportional to the voltage
  \[ I_{DS} = \frac{W}{L} \mu C_{ox}(V_{GS} - V_{TN})V_{DS} \]
- Can define a voltage-dependent resistor
  \[ R_m = \frac{V_{DS}}{I_{DS}} = \frac{1}{\mu C_{ox}(V_{GS} - V_{TN})} \left( \frac{L}{W} \right) = R (V_{GS}) \frac{L}{W} \]
- This is a nice variable resistor, it is electronically tunable!

Finding \( I_D = f(V_{GS}, V_{DS}) \)

- Approximate inversion charge \( Q_N(y) \): drain is higher than the source \( \rightarrow \) less charge at drain end of channel

Expected Behavior: \( I_D - V_{DS} \)

- As the drain voltage increases, the E field across the oxide at the drain end is reduced, and so the charge is less, and the current no longer increases proportionally. As the gate-source voltage is increased, this happens at higher and higher drain voltages.
  - The start of the saturation region is shaped like a parabola
Average Inversion Charge

\[
Q_N(y) = \frac{C_N(V_{GS} - V_T) + C_N(V_{GD} - V_T)}{2}
\]
\[
Q_N(y) = \frac{-C_N(V_{GD} - V_T) + C_N(V_{SD} - V_T)}{2}
\]
\[
Q_N(y) = -\frac{C_N(2V_{GS} - 2V_T) - C_NV_{SD} - V_T}{2} = -\frac{C_N(V_{GS} - V_T - \Delta V)}{2}
\]

- Charge at drain end is lower since field is lower
- Notice that this only works if the gate is inverted along its entire length
- If there is an inversion along the entire gate, it works well because \( Q \) is proportional to \( V \) everywhere the gate is inverted

Drift Velocity and Drain Current

"Long-channel" assumption: use mobility to find \( v \)

\[
v(y) = -\mu_e E(y) \approx -\mu_e (-\Delta V / \Delta y) = \frac{\mu V_{GS}}{L}
\]

And now the current is just charge per area, times velocity, times the width:

\[
I_s = W\mu_e Q_N \approx W\mu_e \left(\frac{V_{GS} - V_T - \Delta V}{2}\right)
\]
\[
I_D = \frac{W}{L} \mu_e \left(\frac{V_{GS} - V_T - \frac{V_{GS}}{2}}{2}\right)
\]

Inverted Parabolas

The Saturation Region

When \( V_{DS} > V_{GS} - V_T \), there isn’t any inversion charge at the drain … according to our simplistic model

Why do curves flatten out?

Square-Law Characteristics

Boundary: what is \( I_{DS_{SAT}} \)?
Square-Law Current in Saturation

Current stays at maximum (where $V_{DS} = V_{GS} - V_{Tb} = V_{DS,SAT}$)

$$I_D = \frac{W}{L} \mu C_{ox} (V_{GS} - V_t - \frac{V_{GS}}{2}) V_{DS}$$

$$I_{DS,sat} = \frac{W}{L} \mu C_{ox} (V_{GS} - V_t - \frac{V_{GS}}{2})(V_{GS} - V_t)$$

$$I_{DS,sat} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_t)$$

Measurement: $I_D$ increases slightly with increasing $V_{DS}$

model with linear “fudge factor”

$$I_{DS,sat} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$