Experiment 8
Multistage Amplifiers

S.-B. Suh, W.T. Yeung, J.C. Rudell, R.T. Howe and B. Nikolic

UC Berkeley EE 105
Fall 2005

1.0 Objective

In Exps. 6 and 7, we investigated the small signal properties of single stage amplifiers (e.g., common source, common drain, etc.). Now we will see how these single stage amplifiers perform together. By cascading the stages, new amplifiers with enhanced performance can be realized. We will also study the effects of loading of one stage on the other.

To show your understanding of the lab, your write-up should contain:

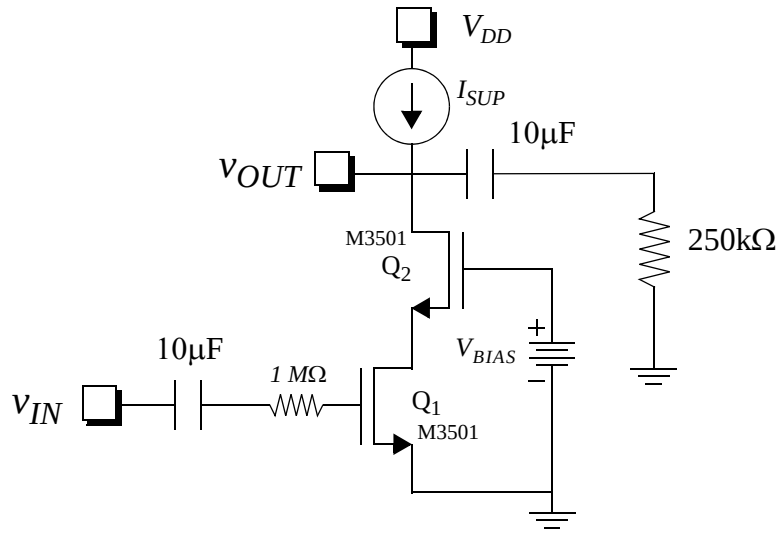
- A discussion on how single stages interact together
- A discussion on interstage loading based on 2-port models

2.0 Prelab

- H & S: Chapter 9
- For the cascode circuit in Fig. 1, hand-calculate the gain, input resistance and output resistance for a supply current of I_{SUP} = 1 mA.

  (SPICE Models: 'Lab Chip Schematics' manual)

FIGURE 1. Cascode Amplifier with Current Source Bias



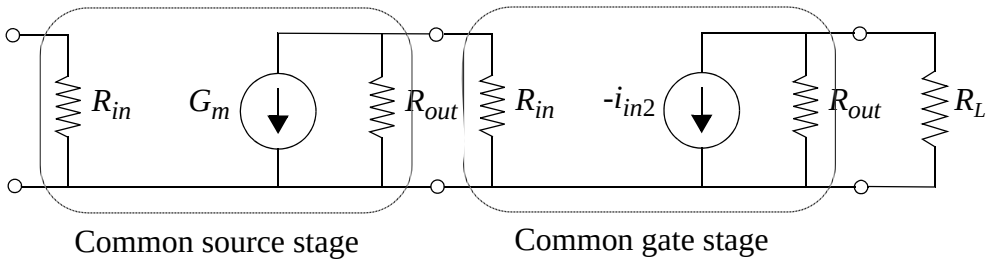
3.0 Procedure

3.1 The Cascode

The cascode amplifier is nothing more than a common source - common gate cascade. Figure 1 above shows a simplified cascode with a current source load.

The 2 port model for the cascode is shown below

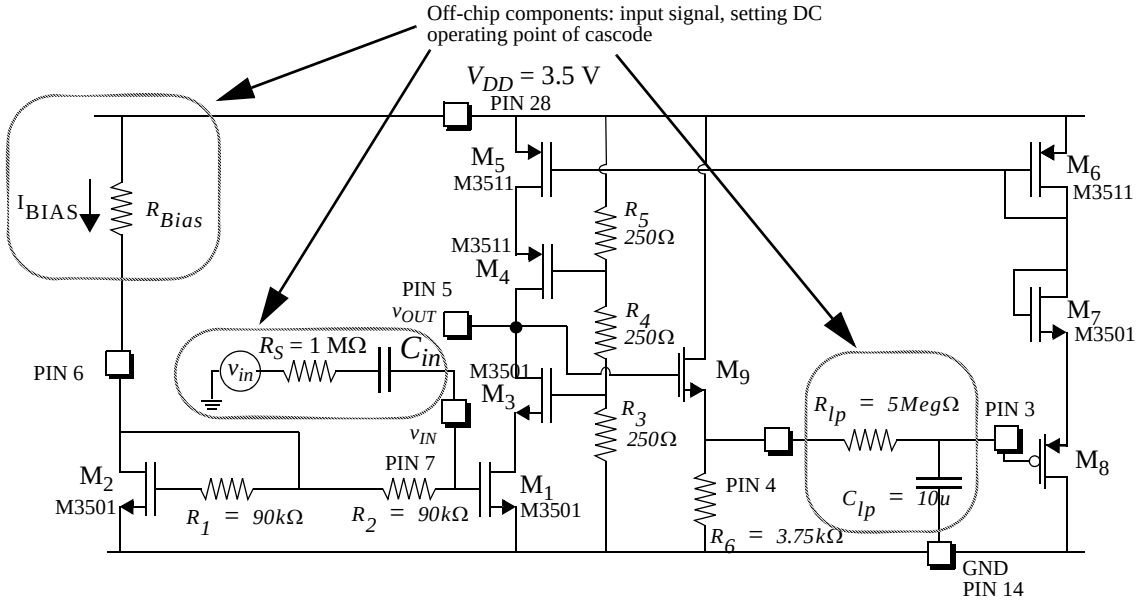
FIGURE 2. 2-Port Representation of Cascode



In your lab, the cascode circuit will include extra biasing circuits as shown in Fig. 3. These circuits make use of DC feedback (coupled through the external low-pass filter), in order to stabilize this high-gain circuit. After simplification, Fig. 3 reduces to the basic cascode amplifier in Fig. 1 for the frequencies we will be concerned with.

1. Set up the circuit from Lab Chip 5 as shown in Fig. 3. Let R_{Bias} be 10 kΩ and C_{in} be 10 μF. Let V_{CC} be set at 3.5 V. Note: The user just needs to furnish the external elements in the box. (the elements in the dashed "boxes" in Fig. 3).
2. Determine the bias current and DC voltage at V_{OUT}. Using Fig. 3, what are the maximum and minimum DC voltages that V_{OUT} can swing to while keeping all the devices in the saturation. Compare with measurements of output clipping levels.
3. Using the oscilloscope, find the gain v_{out}/v_{in}. Use a 5 kHz sine wave with an amplitude of 65 mV. If the signal at the output is clipped, decrease the input amplitude until no clipping occurs.
4. *Calculate* the input resistance and output resistance for the cascode. Using the calculated value of the input resistance, you can calculate how much of the input voltage is attenuated. Determine the gain of the cascode v_{out}/v_{in}. How does the cascode compare to the Common Source in terms of input resistance, output resistance and voltage gain? Optional: *measure* the input and the output resistances.

FIGURE 3. MOS Cascode with DC Feedback Biasing (Lab Chip 5)



Lab Tip

Find the DC voltage at v_{OUT} (PIN 5) and make sure that M_3 and M_4 are saturated. If they are not, get a new chip.The circuit takes about 10 - 20 seconds to stabilize. Be patient.

5. Perform a SPICE analysis on the cascode in Fig. 1 (the circuit in Fig. 3 is extra credit) and compare your results with simulation.

3.2 Cascading Stages

1. *While leaving the cascode intact*, build the common source as shown in Fig. 4; do not include the coupling capacitor yet. Find the bias current through R_{BIAS}. Does the DC voltage at V_{OUT} confirm the fact that $I_D = I_{BIAS}$? Find the gain of the common source.
2. Now cascade the two stages together with the use of the 10 μF coupling capacitor. What is its function? (Hint: look at the DC voltage at both sides of the capacitor) What would happen if the capacitor were not present? Change the amplitude of the sinusoid to 50 mV.
3. Find the gain for the cascade. Measure the gain v_{out1} / v_{in}. Why is it reduced?
4. Draw the 2 port models for the cascaded amplifier in Fig. 4. Comment on the overall gain and the loading between stages.

FIGURE 4. Cascode - Common Source Cascade