CMOS Amplifiers

- General Considerations
- Common-Source Stage
- Common-Gate Stage
- Source Follower
- Summary and Additional Examples

Lecture Outline

General Concepts
- Biasing of MOS Stages
- Realization of Current Sources

MOS Amplifiers
- Common-Source Stage
- Common-Gate Stage
- Source Follower

In an ideal voltage amplifier, the input impedance is infinite and the output impedance zero.
But in reality, input or output impedances depart from their ideal values.
Input / Output Impedances

- The figure above shows the techniques of measuring input and output impedances.

\[ R_x = \frac{V_x}{i_x} \]

Common-Source Stage

- \( \lambda = 0 \)
- \( A_v = -g_m R_D \)
- \( A_v = -\sqrt{2\mu_C W L} I_D R_D \)

Operation in Saturation

- Condition for \( M_1 \) in saturation
  \( V_{out} > V_{in} - V_{TH} \)
  \[ \Rightarrow V_{DD} - R_D I_D > (V_{GS} - V_{TH}) \]

- In order to maintain operation in saturation, \( V_{out} \) cannot fall below \( V_{in} \) by more than one threshold voltage.
- The condition above ensures operation in saturation.

CS Stage with \( \lambda = 0 \)

- \( A_v = -g_m R_L \)
- \( R_{in} = \infty \)
- \( R_{out} = R_L \)
CS Stage with $\lambda \neq 0$

However, channel length modulation leads to finite output resistance, $r_o$, which is in parallel with the load resistance, $R_L$.

\[ A_v = -g_m \left( R_L || r_o \right) \]
\[ R_{in} = \infty \]
\[ R_{out} = R_L || r_o \]

CS Gain Variation with Channel Length

Since $\lambda$ is inversely proportional to $L$, the intrinsic voltage gain actually becomes proportional to the square root of $L$.

[formula]

MOS Biasing

\[ \frac{R_1}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S \]
\[ I_D = \frac{1}{2} \mu \frac{C_{ox}}{L} \frac{W}{2} (V_{GS} - V_{TH})^2 \]

2 unknowns ($V_{GS}$, $I_D$), 2 equations ⇒

\[ V_{GS} = (V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left( \frac{R_1 \frac{W}{2}}{R_1 + R_2} - V_{TH} \right)} \]
\[ V_1 = \frac{1}{\mu \frac{C_{ox}}{L} \frac{W}{R_S}} \]

Voltage at X is determined by $V_{DD}$, $R_1$, and $R_2$.

$V_{GS}$ can be found using the equation above, and $I_D$ can be found by using the NMOS current equation.

Self-Biased MOS Stage

\[ I_D R_D + V_{GS} + R_S I_D = V_{DD} \]
\[ I_D = \frac{1}{2} \mu \frac{C_{ox}}{L} \frac{W}{2} (V_{GS} - V_{TH})^2 \]

The circuit above is analyzed by noting $M_1$ is in saturation and no potential drop appears across $R_G$. 

**Current Sources**

- When in saturation region, a MOSFET behaves as a current source.
- NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from $V_{DD}$ to a point (sources current).

**PMOS CS Stage with NMOS as Load**

$$A_v = -g_{m2} (r_{O1} \parallel r_{O2})$$

- Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.

**CS Stage with Current-Source Load**

$$A_v = -g_{m1} (r_{O1} \parallel r_{O2})$$

- To alleviate the headroom problem, an active current-source load is used.
- This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.

**CS Stage with Diode-Connected Load**

$$A_v = -g_{m1} \left( \frac{1}{g_{m2}} r_{O2} \parallel r_{O1} \right)$$

- Lower gain, but less dependent on process parameters.
CS Stage with Diode-Connected PMOS Device

\[ A_v = -g_{m2} \left( \frac{1}{g_{m1} \parallel r_{o1} \parallel r_{o2}} \right) \]

- Note that PMOS circuit symbol is usually drawn with the source on top of the drain.

CS Stage with Degeneration

\[ A_v = - \frac{R_D}{1 + \frac{1}{g_m}} \]
\[ \lambda = 0 \]

- Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.

Example of CS Stage with Degeneration

\[ A_v = - \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \]

- A diode-connected device degenerates a CS stage.

CS Stage with Gate Resistance

\[ V_{RG} = 0 \]

- Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.
Output Impedance of CS Stage with Degeneration

Similar to the bipolar counterpart, degeneration boosts output impedance.

\[ r_{\text{out}} \approx g_m r_O R_s + r_O \]

Output Impedance Example (I)

When \( \frac{1}{g_m} \) is parallel with \( r_{O2} \), we often just consider \( \frac{1}{g_m} \).

\[ R_{\text{out}} = r_{O1} \left(1 + g_{m1} \frac{1}{g_{m2}}\right) + \frac{1}{g_{m2}} \]

Output Impedance Example (II)

In this example, the impedance that degenerates the CS stage is \( r_O \), instead of \( \frac{1}{g_m} \) in the previous example.

\[ R_{\text{out}} \approx g_{m1} r_{O1} r_{O2} + r_{O1} \]

CS Core with Biasing

Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.
Common-Gate Stage

- Common-gate stage is similar to common-base stage: a rise in input causes a rise in output. So the gain is positive.

\[ A_v = g_m R_D \]

I/O Impedances of CG Stage

- The input and output impedances of CG stage are similar to those of CB stage.

\[ R_{in} = \frac{1}{g_m} \quad \lambda = 0 \quad R_{out} = R_D \]

Signal Levels in CG Stage

- In order to maintain M1 in saturation, the signal swing at \( V_{out} \) cannot fall below \( V_b - V_{TH} \)

CG Stage with Source Resistance

- When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.

\[ A_v = \frac{R_D}{\frac{1}{g_m} + R_S} \]
Generalized CG Behavior

When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it (at low frequencies).

- The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.

\[ R_{\text{out}} = (1 + g_m r_O) R_S + r_O \]

Example of CG Stage

Diode-connected M2 acts as a resistor to provide the bias current.

\[ \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{g_m R_D}{1 + (g_m + g_m 2) R_S} \]

\[ R_{\text{out}} \approx \left[ g_m r_{\text{on}} \left( \frac{1}{g_m 2} || R_S \right) + r_{\text{on}} \right] || R_D \]

CG Stage with Biasing

- \( R_1 \) and \( R_2 \) provide gate bias voltage, and \( R_3 \) provides a path for DC bias current of \( M_1 \) to flow to ground.

Source Follower Stage

\[ \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{R_3 \left( 1/g_m \right) \cdot g_m R_D}{R_3 \left( 1/g_m \right) + R_S \cdot g_m R_D} \]
Similar to the emitter follower, the source follower can be analyzed as a resistor divider.

In this example, $M_2$ acts as a current source.

The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.

$R_{out} = \frac{1}{g_m} || r_O || R_L \approx \frac{1}{g_m} || R_L$

$R_G$ sets the gate voltage to $V_{DD}$, whereas $R_S$ sets the drain current.

The quadratic equation above can be solved for $I_D$. 

$$I_D = \frac{1}{2} \mu_n C_A \frac{W}{L} (V_{DD} - I_D R_S - V_{TH})^2$$
Supply-Independent Biasing

If $R_s$ is replaced by a current source, drain current $I_D$ becomes independent of supply voltage.

Example of a CS Stage (I)

M1 acts as the input device and M2, M3 as the load.

Example of a CS Stage (II)

M1 acts as the input device, M3 as the source resistance, and M2 as the load.

Examples of CS and CG Stages

With the input connected to different locations, the two circuits, although identical in other aspects, behave differently.
Example of a Composite Stage (I)

By replacing the left side with a Thevenin equivalent, and recognizing the right side is actually a CG stage, the voltage gain can be easily obtained.

\[ A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \]

Example of a Composite Stage (II)

This example shows that by probing different places in a circuit, different types of output can be obtained.

\[ \frac{v_{out2}}{v_{in}} = -\frac{1}{g_{m3}} \left| \frac{r_{O3} \parallel r_{O4}}{r_{O2} + \frac{1}{g_{m1}}} \right| \]

Vout1 is a result of M1 acting as a source follower whereas Vout2 is a result of M1 acting as a CS stage with degeneration.