EECS105 Final	Name
5/12/10	SID

1	/20
2	/30
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6	/40
7	/20
8	/20
Total	

- 1. Give a short answer to each question
- a. Your friend from Stanford says that he has designed a three-stage high gain amplifier that works great, but when he puts it in unity-gain feedback he sees a big sine wave at high frequency. He thinks that maybe it's power supply noise that is getting amplified. What do you tell him?
- b. Your friend from USC is trying to make an oscillator by using feedback around a single-stage high-gain amplifier. Her circuit doesn't oscillate. Open loop, it works great as an amplifier though, with a phase shift that varies between -180 and -270 degrees from the input to the output over all frequencies. She thinks that maybe she should try to increase the gain to get it to oscillate. What do you tell her?

- c. If you measure the reverse leakage current of a diode at room temperature to be 1nA, and the increase the temperature to 85C, will the leakage current increase or decrease, and by roughly what factor chosen from this list: {a lot less than 2, roughly 2, roughly 10, a lot more than 10}
- d. Why do circuit designers like to use feedback when they make amplifiers? Give at least two reasons.

2. You have invented a new type of transistor with terminals A, B, and C. In the "active" region, defined by V_{AC} >0, V_{BC} >1, you have determined the formulas for the currents into nodes A and B are:

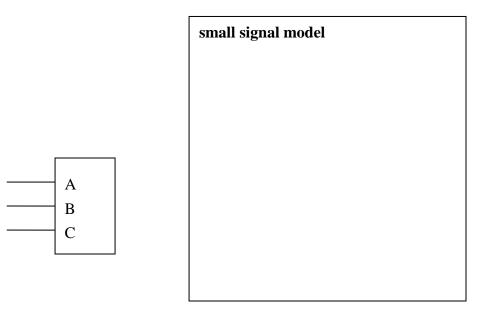
 $I_A = I_0 \alpha V_{AC}$

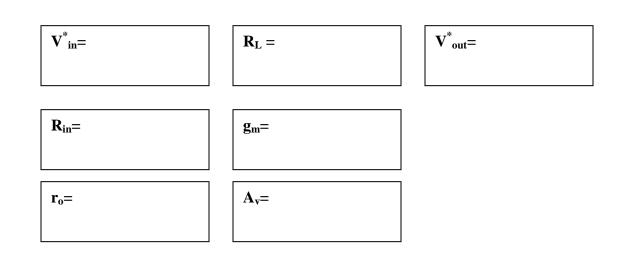
 $I_{\rm B} = I_0 \left(\beta V_{\rm AC}\right)^3 \ln(\delta V_{\rm BC})$

Where I_0 , α , β , and δ are process-related parameters. For simplicity, assume that α , β , and δ are all equal to 1 [V⁻¹], and $I_0 = 1$ mA.

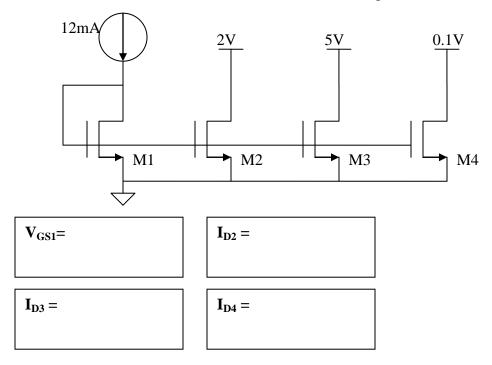
How would you wire this device up to make a simple voltage amplifier with a gain of at least 10? Draw your circuit below, using only a resistor R_L and a 10V supply. Clearly identify the input and output terminals of your amplifier. What input bias bias point (V_{in}^* and V_{out}^*) and resistor value would you pick? Hint: calculate the intrinsic gain as a function of the bias point voltages first.

At this bias point, calculate the input resistance, transconductance, and output resistance of your transistor, and the gain of your amplifier. Draw the DC small-signal model of your transistor.

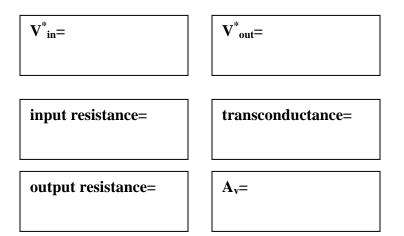




3. In the current mirror below, assume that $\mu_n C_{ox} = 200 \text{uA/V}^2$, $\lambda = 0.1/\text{V}$, and $V_{\text{TN}} = 1\text{V}$. All transistors have W/L = 100u/1u. Calculate the gate bias voltage V_{GS1} resulting from the input current. Calculate the currents flowing in the drains of the other transistors. All calculations should be accurate to a few percent.



4. Given the spice input and a portion of the hspice output below, find the bias point (V^{*} in and out), transconductance, input resistance and output resistance of the transistor, and the voltage gain of this circuit. Answers should be accurate to within a few %.



```
[ Hspice input deck]
* Common Emitter test deck
Vcc cc 0 3
Vin in 0 dc 0.6
.model npn npn bf=100 IS=1e-15 vaf=50
Q1 out in 0 npn
Rc cc out 100k
.op
.options post
.end
[Portion of hspice output]
subckt
element 0:q1
model 0:npn
        138.7999n
 ib
         14.1533u
 ic
 vbe
        600.0000m
 vce 1.5847
vbc -984.6662m
 vs
          -1.5847
 power
          22.5116u
 betad 101.9693
         550.6107u
 gm
         185.0998k
 rpi
          Ο.
 rx
           3.6023x
 ro
          0.
 cpi
 cmu
           Ο.
          Ο.
 cbx
 CCS
           Ο.
 betaac 101.9179
         87.6324g
 ft
```

5. For the circuit below, find the operating point voltages and currents I_B , and I_C . Calculate the DC gain from point A to point B. Calculate the DC gain from point B to point C. Assume $I_S=4x10^{-15}$ A, $\beta=100$, and $V_A=100V$. Answers should be accurate to **10%**.

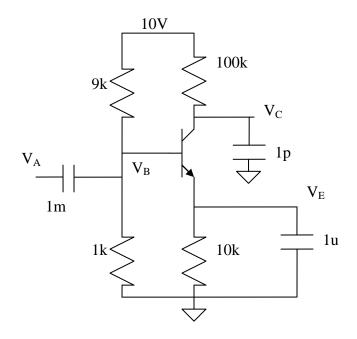
$\mathbf{V}_{B}^{*} =$	$\mathbf{V}_{C}^{*} =$	$\mathbf{V}_{\mathrm{E}}^{*} =$	
I [*] _B =	I [*] _C =	DC gain, A->B =	DC gain, B->C =

For what range of frequency does the gain from A->B become approximately one? (for example "X rad/sec and below", or "X to Y rad/sec")

Frequency range:

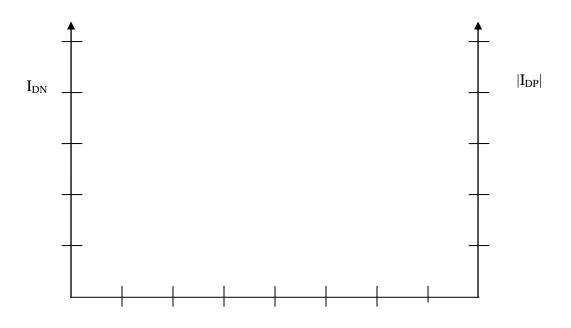
What is the frequency at which the gain from B to C is **10 times greater** than the DC value above? What is the maximum gain from A to C?

Freq for 10x DC gain B to C:	max gain:
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On the next page, draw a Bode plot of the transfer function from A to C.

6. You have a CMOS inverter with $(W/L)_N = 10u/1u$ and $(W/L)_P = 20u/1u$ running from a 4V supply. Assume that $\mu_n C_{ox} = 200uA/V^2$, $\mu_p C_{ox} = 100uA/V^2$, $\lambda_N = \lambda_P = 0.1/V$, and $V_{TN} = 1V$, $V_{TP} = -1V$. Carefully plot the drain current vs. output voltage for the NMOS device when $V_{IN} = 2V$. On the same plot, carefully draw the magnitude of the PMOS drain current vs. the output voltage when $V_{IN} = 2V$. (10pts)



What is the DC output value with this input? At this operating point, what region of operation is each transistor in (off, linear, saturation)?

$V_{out}(2V) =$	NMOS region	PMOS region

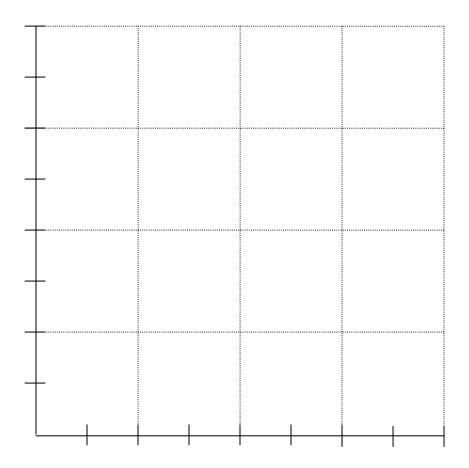
For this region of operation, estimate the gain at this operating point, and the *approximate* output voltage limits ($V_{out,min}$ and $V_{out,max}$), and the corresponding input min and max.

gain =	V _{out,min} =	V _{out,max} =
	V _{in,max} =	V _{in,min} =

What is the range of input voltages for which the DC output is V_{DD} ? What is the range of input voltages for which the DC output is 0?

V_{in} range for $Vout = V_{DD}$	V_{in} range for Vout = 0

On the next page, plot the DC voltage transfer curve of this inverter (10pts). LABEL YOUR AXES CLEARLY!



Note: everyone knows roughly what this curve looks like. You get points for showing me that you know *exactly* what it looks like (at least in the regions described on the previous page). Be neat, and label things clearly!

7. The inverter in the previous problem is used to switch a capacitive load. The total output capacitance is 1pF. Up to time t=0, the input to the amplifier is 0, and the output is V_{DD} . At time t=0 the input switches instantaneously to V_{DD} . What is the initial rate of change of the output voltage just after t=0? How long does it take for the output to fall 400mV (to V_{DD} -400mV)?

dV_{out}/dt (t=0) =	$t_{fall 400mV} =$

What is the differential equation that describes the output voltage when $V_{out} < V_{DD}/$ 10? How long does it take for the output to fall from $V_{DD}/10=400mV$ to approximately $V_{DD}/27=400mV/2.7$? Your answers should be accurate to 10%.

Differential equation	
Time to fall by a factor of 2.7 from 400mV:	

8. For the circuit below, what condition must be satisfied for the circuit to oscillate when you close the loop (short V_{FB} to V_{IN})?

condition for oscillation

For some value of C_{FB} and R_{FB} , you plot the open-loop transfer function from V_{IN} to V_{FB} . You find that there is a pole at $\omega = 1/(R_{FB} C_{FB})$ that is substantially lower than all of the other poles in the system. You also find that at the frequency where the phase crosses -360, the gain is about 50. Will the system oscillate if you close the loop? If yes, how would you change C_{FB} to stop it from oscillating, and why would that work?

Will it oscillate?

If so, how and why change C_{FB}?

For some different values of C_{FB} and R_{FB} , you plot the open-loop transfer function and find that at the frequency where the phase crosses -360 the gain is about 0.1. Will the system oscillate if you close the loop? If yes, how would you change C_{FB} to stop it from oscillating, and why would that work?

