UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105 Prof. Pister
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Names:
SIDs:

Lab 9 – Prelab

1. Download lab9part0 and run the simulation. Record the voltages that you expect to see in part 0 of the lab where you test your transistors.

2. Download lab9part1 and run the simulation. Click on the output node to plot that voltage vs. Vin. What input bias voltage do you need to get high gain? What is the range of output voltages for which the gain is high (this is useful during the lab – if you see the output outside of this range you know that you're not in the high-gain region).

3. Download lab9part2 and run the simulation. Click on the output voltage to get a bode plot. Right-click on the left axis and select "manual limits". Select "logarithmic" instead of "decibels". What is the low-frequency gain and the pole frequency for this amplifier? What DC bias did I use to get that gain? Increase the DC bias by 50mV and re-run the simulation. How much did the gain change?

4. Download lab9part3and run the simulation. Click on the nodes labeled gate, out1, out2, and out3 to display each of those waveforms. Estimate the gain to out1, out2, and out3. (Hint: the input sine wave has an amplitude of 100mV and a frequency of 1kHz, so the rate of change near zero crossings is $(100\text{mV})(2\pi 10^3) = 600\text{V/s}$. Use the mouse to zoom in and measure the maximum rate of change of the other voltages. The gain is the ratio of the rates of change.)

5. Download lab9part4 and run the simulation Why do you think that V(gate) looks more triangular than the others?

6. Download lab9part5 and run the simulation. What is the magnitude and phase of the low frequency gain?