Laboratory 6: Multi-Stage Amplifier Design Project

1. Introduction

In this lab you will design, build and demonstrate a multi-stage amplifier using the BS170 NMOS transistor and the BS250 PMOS transistor meeting the following set of specifications. This lab has three phases: hand design, SPICE simulation and lab verification. You must write a complete laboratory report describing your efforts.

2. Specifications

In the previous lab, you designed a common-source amplifier having a maximum bandwidth of 20 kHz. We are now interested in designing an amplifier with more than 10x the bandwidth. The design specifications for this lab are shown in Table 1. The input attenuation network is similar to the previous lab, but its resistance was increased by 10 times (Figure 1).

Parameter	Specification
Mid-band gain ($\|A_{mid}\|$)	>50 V/V
High -3dB frequency (f_H)	>350 kHz
Low -3dB frequency (f_L)	<300 Hz
Output swing (undistorted)	>3 V_{pp}
Supply voltage (V_{dd})	15 V
Output load (C_L)	1 nF
Input attenuation network	1kΩ /100kΩ

Table 1: Design specifications

Moreover, we want to minimize the power consumption of the circuit. Component values are to be chosen by you to meet the specifications. The topology of the amplifier will be a folded cascode followed by a common drain stage, and all the stages are directly coupled. Like in the previous lab, the mid-band gain is measured between the amplifier output and the attenuation network output.

All resistors and capacitors must be standard 10% values (no parallel/series combination).

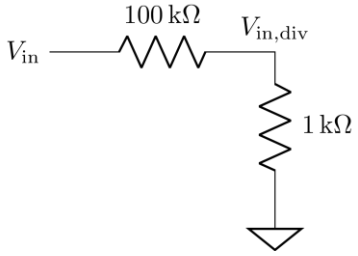

Figure 1: Input attenuation network

3. Design guidelines

Bandwidth improvement

In order to achieve this, we need to change the topology of the circuit from the first lab. Recall that the bandwidth of the common source amplifier was limited by the output resistance of R_D. We can add a common drain output stage (Figure 2), which will have an output resistance approximated by $1/g_m$. By choosing g_m correctly, the output stage bandwidth can be greatly increased:

$$f_{out} = \frac{g_m}{2\pi C_L}$$

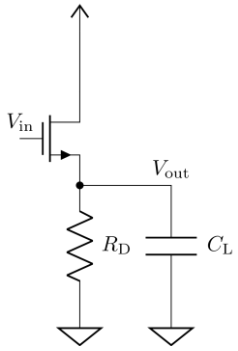

Figure 2: Common drain stage

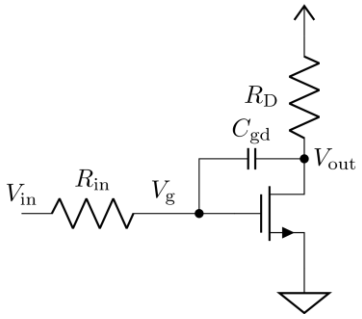

Figure 3: Common source stage Miller effect

As we increase the bandwidth of the output stage, we now need to take care of the Miller effect (Figure 3). In order to make the Miller effect more apparent, in this lab we increased the resistance of the input attenuation network.

You can show that the frequency of the pole caused by the Miller effect, combined with the input Thévenin equivalent resistance is:

$$f_{in} = \frac{1}{2\pi R_{in} C_{Miller}}$$

with

$$C_{Miller} = C_{gd}(1+A_{V1})$$

where A_{V1} is the voltage gain of the common source stage. Because we want large gain and bandwidth, we need to reduce the voltage gain of the first stage. The common drain output stage has a voltage gain of approximately 1, so we could add a common gate stage in between to take care of the voltage gain. Because we want to also experiment with PMOS, in this lab the common gate stage will use BS250. This NMOS common-source and PMOS common-gate configuration is called *folded cascode*.

The complete amplifier schematic is shown in Figure 4. It contains an attenuation network like the previous lab, and the required gain is the output voltage divided by the input voltage after the attenuation network:

$$|A| = \frac{v_{\text{out}}}{v_{\text{i,div}}}$$

Note that the values of R_{G1} and R_{G3} are already provided.

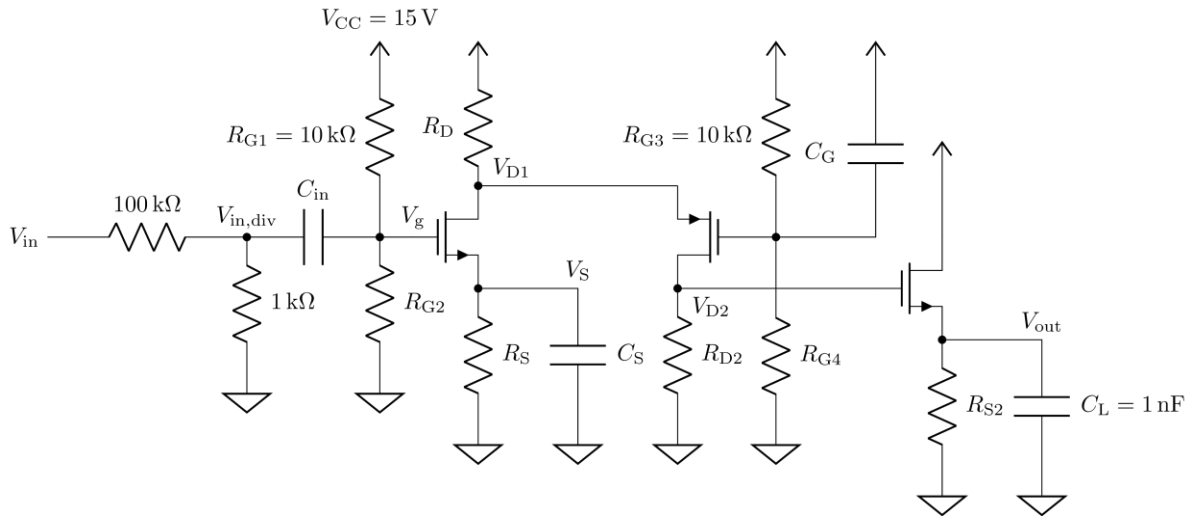

Figure 4: Common source amplifier schematic

Biasing circuit

The biasing circuit provides two functions: it sets the transistor gain gm and current ID, and also provides stability to the transistor bias. In order to have good stability, you can choose V_S between 2V and 5V, and V_{D1} between 10V and 13V.

Next, you can show that the voltage gain of the common-source stage will be approximately

$$A_{V1} = -\frac{g_{m1}}{g_{m2}}$$

while the voltage gain of the common-gate stage is approximately

$$A_{V2} = g_{m2} R_{D2}$$

In order to maximize output swing, the output of the common-gate stage V_{D2} should be roughly between ground and V_{D1}.

Finally, the total gain will be given by $A_{V1}A_{V2}$ since the common-drain stage has near to unity gain.

Transfer function

The bypass and decoupling capacitors (C_S and C_{in}, respectively) will determine the low frequency response of the amplifier, similar to the previous lab. In addition, there is an additional decoupling capacitor C_G which has an effect similar to C_S.

As mentioned previously, when designing for a higher bandwidth several factors will limit the upper cutoff frequency of the amplifier:

- The first pole is caused by the output stage and the load capacitor. Increasing g_{m3} will increased the pole frequency at the expense of power consumption.
- The second pole is caused by the Miller effect. It is mitigated by lowering A_{V1}.
- The third pole occurs in the intermediate stage on the V_{D2} node. The output resistance of the common gate stage is approximately R_{D2}, and it drives the gate-drain capacitance of both the second and third FETs.

$$f_{int} = \frac{1}{2\pi R_{D2} 2C_{gd}}$$

If you encounter that f_{int} is limiting your bandwidth, you will need to play with the ratio between g_{m1} and g_{m2}, to balance the Miller effect and the third pole frequency.

4. Simulation

For this project, you may use either HSPICE or LTspice. The BS170 transistor can be described with the following model, which was improved from the previous lab:

```
.SUBCKT BS170 1 2 3
* 1=drain  2=gate  3=source
Cgs  2 3 12.3E-12
Cgd1 2 4 27.4E-12
Cgd2 1 4 6E-12
M1 1 2 3 3 MOST1
M2 4 2 1 3 MOST2
D1 3 1 Dbody
.MODEL MOST1 NMOS(Level=3 Kp=0.065 Rs=20m Vto=2 Rd=1.186 gamma=0)
.MODEL MOST2 NMOS(VTO=-4.73 Kp=0.065 Rs=20m gamma=0)
.MODEL Dbody D(Is=125f N=1.023 Rs=1.281 Ikf=18.01 Cjo=46.3p M=.3423
+            Vj=.4519 Bv=60 Ibv=10u Tt=161.6n)
.ENDS
```

The BS250 PMOS model is the following:

```
.SUBCKT BS250P 1 2 3
*1=drain 2=gate 3=source
Cgs 2 3 20.1E-12
Cgd1 2 4 57.1E-12
Cgd2 1 4 5E-12
M1 1 2 3 3 MOST1
M2 4 2 1 3 MOST2
D1 1 3 Dbody
.MODEL MOST1 PMOS(LEVEL=3 VTO=-2.7 KP=0.025 RD=4.014 RS=20m gamma=0)
.MODEL MOST2 PMOS(VTO=2.43 KP=0.025 RS=20m gamma=0)
.MODEL Dbody D(CJO=53.22E-12 VJ=0.5392 M=0.3583 IS=75.32E-15 N=1.016 RS=1.245
+ TT=86.56n BV=45 IBV=10u)
.ENDS
```

You are encouraged to first simulate a two-stage common-source/common-drain amplifier, in order to understand the Miller effect.

Simulate both the DC operating point, as well as the AC transfer function (both magnitude and phase). A transient analysis can be used to verify the output swing specification.

5. Lab

In lab you will verify your design (both hand calculations and SPICE simulations). After implementing your circuit, you should verify the design parameters and specifications using relevant measurements. In particular, make sure you measure the DC bias operating point (drain current and gate voltage), as well as the AC characteristics such as gain, output swing, low frequency cutoff and high frequency cutoff. Make sure you minimize any parasitic capacitances in your circuit, which will be especially important for the high frequency cutoff. During lab you may find that you need to iterate your design, for example if the gain is not large enough. In this case you should calculate or simulate the changes to describe their effect.

6. Report

Your report should be a concise yet comprehensive description and evaluation of your design, simulation and laboratory measurements. The report should contain no more than 12 pages of text and figures and should include proper caption and formatting.

Your report should contain the sections listed in Table 2.

Section	Weight
Introduction	10%
Hand design	30%
Simulation	20%
Experimental results	30%
Summary	10%

Table 2: Laboratory report sections

The introduction should include a description of how you approached the design problem and what trade-offs in the specifications you first encountered.

In the hand design section you should explain how you solved the design constraints, using equations where appropriate. Clearly explain how you designed both the operating bias point, and well and the frequency response. There is no need to derive the results shown in class, but you should show the equations in variable form before evaluating. Include a summary of the specifications achieved by the hand design.

The SPICE section should contain a description of the simulated circuit (either a netlist or a LTspice screenshot) as well as figures showing the simulation results. Include a summary of the simulated specifications.

In the experimental results, show the relevant measurements (multimeter, oscilloscope plots, etc.) proving that the circuit behaves as intended. If you changed any value from the hand design, you should justify in this section.

In the summary, include a table that compares the specified parameters from the hand design, the SPICE simulation and the lab measurements. Briefly explain any discrepancies.