EE105
Microelectronic Devices and Circuits: MOSFET

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Simplest Model of MOSFET (from EE16B)

N-type MOSFET (NMOS)

\[ V_{\text{gate}} = V_{GS}, \quad V_{DS} > 0, \quad I_{DS} > 0 \]

Case 1. \( V_{\text{gate}} < V_{th,N} \)

Case 2. \( V_{\text{gate}} > V_{th,N} \)

P-type MOSFET (PMOS)

\[ V_{\text{gate}} = V_{SG}, \quad V_{SD} > 0, \quad I_{SD} > 0 \]

Case 1. \( V_{\text{gate}} < V_{th,P} \)

Case 2. \( V_{\text{gate}} > V_{th,P} \)

Note bubbles

\( V_{SG} \) and \( V_{gate} \)

\( V_{th,n} \neq V_{th,p} \)

"OFF" State

Open Circuit

"ON" State

Short Circuit
CMOS Inverter

Positive Power Supply

PMOS

why is the PMOS Drain here?

NMOS

Ground

V_{in} = V_{gs} of NMOS

1. When V_{in} is high
   - V_{in} = V_{DD} > V_{th,n}
   - NMOS is ON
   - V_{out} = 0 \rightarrow "Low"

   \[ V_{sg}(PMOS) = V_{DD} - V_{DD} = 0 \]
   \[ < V_{th,p} \]
   - PMOS is OFF

2. V_{in} is "Low"
   - V_{in} = 0 = V_{gs}(NMOS)
   \[ < V_{th,n} \]
   - NMOS is OFF

   \[ V_{sg} = V_{DD} - 0 = V_{DD} > V_{th,p} \]
   - PMOS is ON
   - V_{out} = V_{DD} = "High"
CMOS NAND Gate

A = "1", B = "1"
Both NMOS’s are ON

\[ V_{out} = 0 \text{V} \Rightarrow "0" \]

A = "0" or B = "0"

\[ \Rightarrow V_{out} = V_{DD} \Rightarrow "1" \]

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<th>B</th>
<th>out = AB</th>
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More Circuit Symbol for NMOS

4 terminal including Body (Arrow pointing to channel indicating substrate is p-type)

Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)

Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Note in NMOS
1. Drain voltage is always more positive than Source voltage
2. Current always flows from Drain to Source
More Circuit Symbol of PMOS

4 terminal including Body
(Arrow pointing away from channel indicating substrate is n-type)

Modified circuit symbol with arrow on source
(Arrow indicating direction of current flow)

Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

Note in PMOS
1. Source voltage is always more positive than Drain voltage
2. Current always flows from Source to Drain
3. Source is usually drawn on top so current flows downward (convention)
MOSFET Device Structure

- MOSFET: metal-oxide-semiconductor field effect transistor
- Typically
  - Channel length: $L \sim < 10 \text{ nm}$ to $0.35 \text{ μm}$,
  - Channel width: $W \sim 0.05 \text{ μm}$ to $100 \text{ μm}$,
  - Oxide thickness: $t_{ox} \sim 1$ to $10 \text{ nm}$
MOS Capacitor

0. \( V_{\text{gate}} \leq 0 \Rightarrow \text{MOS like parallel plate} \)
\[ C = C_{\text{ox}} = \frac{E_{\text{ox}}}{t_{\text{ox}}} \quad \text{per unit area} \quad \left[ \frac{\text{F}}{\text{m}^2} \right] \]

1. \( V_{\text{gate}} < V_{\text{th,N}} \)
   "like" reverse-biased p-n junction
   \[ C = \left[ \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{dep}}} \right] = \frac{C_{\text{ox}}C_{\text{dep}}}{C_{\text{ox}} + C_{\text{dep}}} \]
   \[ \frac{1}{C_{\text{ox}}} \quad \frac{1}{C_{\text{dep}}} \]

2. \( V_{\text{gate}} > V_{\text{th,N}} \)
   "OFF" \quad C \quad "ON"
\[ C = C_{\text{ox}} \quad \text{n-channel is formed} \]
NMOSFET (or simply NMOS)

- N-channel MOSFET
  - Current conducted by electrons
- 3 terminal device
  - Source (S): n+ (heavily n-type)
  - Drain (D): n+
  - Gate (G): metal deposited on insulator above channel
- Substrate (called “Body”) is a 4th terminal
  - Substrate is p-doped
- Electrons is induced in channel when a positive gate voltage is applied
- Electrons moves from Source to Drain
  - Current flows from D to S

\[ V_{GS} \quad V_{DS} \]
Creating a “Channel” for Current Flow

MOS is a capacitor across an insulator (oxide). When a positive voltage is applied at Gate, electrons are induced under the gate.

At "threshold", sufficient number of electrons form a "channel" between Source and Drain, forming a conductive channel.

Total charge in the channel:

$$|Q| = C_{ox} \cdot WL \cdot (v_{GS} - V_t)$$

where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ is oxide capacitance per unit area

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} \text{ F/m}$$

$W$ : gate width

$L$ : gate length

$V_t$ : Threshold voltage

$\varepsilon_{GS} - V_t \equiv V_{OV}$ is called "Overdrive Voltage"
\[ J = \sigma \cdot E = \left( nq \cdot \mu_n \right) \left( \frac{V_{DS}}{L} \right) \]

\[ E = \frac{V_{DS}}{L} \]

\[ Q = C \cdot \Delta V \]

\[ \text{MOS Capacitance} = \frac{1}{C_{OX}} \left( V_{GS}-V_{T} \right) \cdot W \cdot L \]

\[ \text{area} \]

\[ \text{[cm}^2\text{]} \]

\[ \text{conductivity} \]

\[ \frac{A}{\text{cm}^2} \]

\[ \frac{V_{DS}}{L} \]

\[ \text{area of channel} \]

\[ I_{DS} = J \cdot t_{ch} \cdot W \]

\[ = \left( nq \cdot \mu_n \right) \left( \frac{V_{DS}}{L} \right) t_{ch} \cdot W \]

\[ = C_{OX} \left( V_{GS}-V_{T} \right) \cdot \frac{W}{L} \cdot \frac{W}{t_{ch}} \]

\[ \text{MOS capacitance} \]

\[ \frac{I_{DS}}{W \cdot L} \]

\[ \text{area} \]

\[ \text{[cm}^2\text{]} \]

\[ \text{[co} \text{u} \text{t}] \]

\[ n \]

\[ \text{I}_{DS} = \frac{I_{DS}}{W \cdot L} \]

\[ \mu_n C_{OX} \left( V_{GS}-V_{T} \right) \left( \frac{W}{L} \right) \cdot V_{DS} \]

\[ \text{”Aspect ratio”} \]

\[ \text{Equivalent resistance} \]

\[ R_{ch} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\mu_n C_{OX} \left( V_{GS}-V_{T} \right) \left( \frac{W}{L} \right)} \]

\[ \text{geometry} \]

\[ \text{gate bias} \]
Large-Signal Model

(usually used to solve DC bias voltage and current)
When $v_{OV} = v_{GS} - V_t > 0$, a channel is formed between Source and Drain.

Linear charge density in channel:

$$\frac{|Q|}{L} = C_{ox} W \cdot v_{OV}$$

Electric field along the channel

$$|E| = \frac{v_{DS}}{L}$$

Drain current = charge density x velocity:

$$i_D = \frac{|Q|}{L} v_n = \frac{|Q|}{L} \mu_n |E| = C_{ox} W \cdot v_{OV} \mu_n \frac{v_{DS}}{L}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS}$$

At small $v_{DS}$, the transistor is like a gate-controlled variable resistor.
Current at Small $v_{DS}$

$$i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS}$$

$$= k'_n \frac{W}{L} v_{OV} v_{DS}$$

$$= k_n v_{OV} v_{DS}$$

where

$k'_n = \mu_n C_{ox}$: process transconductance parameter

$k_n = \mu_n C_{ox} \left( \frac{W}{L} \right)$: MOSFET transconductance parameter

MOSFET behaves like a linear resistor

$$r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{k_n v_{OV}}$$

Resistance value can be changed by gate voltage (overdrive voltage)
Triode Region \( (v_{DS} < v_{OV}) \)

As \( v_{DS} \) increases, the potential in the channel is no longer a constant. Assume the channel is \( v(x) \):

\[
i_D = C_{ox} W (v_{GS} - v(x) - V_t) v_n(x)
\]

\[
v_n(x) = \mu_n |E(x)| = \mu_n \frac{dv(x)}{dx}
\]

Note: \( i_D \) is still constant along the channel (think Kirchhoff's Current Law)

Integrate along the channel

\[
\int_{x=0}^{x=L} i_D dx = \int_{x=0}^{x=L} \left( C_{ox} W (v_{GS} - v(x) - V_t) \mu_n \frac{dv(x)}{dx} \right) dx
\]

Change of variable on right-hand side: \( x \rightarrow v \)

\[
i_D L = \int_{v=0}^{v=v_{DS}} \left( C_{ox} W (v_{OV} - v) \mu_n \right) dv
\]

\[
i_D = \mu_n C_{ox} \frac{W}{L} \left( v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)
\]
\[ I_D = I_{DS} = \mu n C_{ox} \left( \frac{W}{L} \right) (V_{gs} - V_{tn}) \cdot V_{ds} \]

small \( V_{ds} \)

E field constant

\[ E = \frac{V_{ds}}{L} \]

channel potential

\[ I_D = \mu n C_{ox} W (V_{gs} - V_{xc} - V_{tn}) \frac{dV_{gs}}{dx} \]

constant for a given \( V_{ds} \)

Want \( I_{ds}, V_{ds} \)

KCL, \( I_D = \text{constant} \)

\[ \int_0^L I_D \cdot dx = I_D \cdot L = \mu n C_{ox} W \int_0^L (V_{gs} - V_{xc} - V_{tn}) \frac{dV_{gs}}{dx} \cdot dx \]

\[ U_{cl} = V_{ds} \]

\[ U_{ov} = V_{gs} - V_{tn} \]

\[ = \mu n C_{ox} W \int_0^{V_{ds}} (U_{ov} - V) \cdot dU \]

\[ = \mu n C_{ox} W \left[ U_{ov} \cdot V_{ds} - \frac{1}{2} V^2 \right]_{U_{ds}}^{V_{ds}} \]

\[ = \mu n C_{ox} W \left[ U_{ov} V_{ds} - \frac{1}{2} V_{ds}^2 \right] \]

Check \( V_{ds} \ll U_{ov} \)

\[ I_D \to \mu n C_{ox} \frac{W}{L} \cdot U_{ov} \cdot V_{ds} \text{ same expression} \]

\[ I_D = \mu n C_{ox} \left( \frac{W}{L} \right) (U_{ov} V_{ds} - \frac{1}{2} V_{ds}^2) \]
Triode Region \((v_{DS} < v_{OV})\)

When \(0 \leq v_{DS} \leq v_{OV}\)

\[
i_D = \mu_n C_{ox} \frac{W}{L} v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2
\]

This is called the "Triode Region"
Pinch-Off

The channel potential at the drain side is \( v_{DS} \).
When \( v_{DS} = v_{OV} \), the local charge density there
\[
\frac{|Q|}{\text{area}} = C_{ox} \left( v_{GS} - v_{DS} - V_t \right) = C_{ox} \left( v_{OV} - v_{DS} \right) = 0
\]
So the channel is "pinched off" near the Drain.
Once the channel is pinched off, the drain current remains constant:
\[
i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2
\]
This region, \( v_{DS} > v_{OV} \), is called "Saturation"
Saturation Region \((v_{DS} > v_{OV})\)

When \(0 \leq v_{DS} \leq v_{OV}\)

\[
i_D = \mu_n C_{ox} \frac{W}{L} \left( v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)
\]

This is called the "Triode Region"

When \(v_{DS} > v_{OV}\),

\[
i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2
\]

This is called "Saturation Region"
Full I-V Curves of NMOSFET

\[ v_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) V_{OV}^2 \]

\[ v_D \leq v_{OV} \quad \text{T} \quad \text{Triode region} \]

\[ v_D \geq v_{OV} \quad \text{S} \quad \text{Saturation region} \]

\[ v_{DS} = v_{OV} \]

\[ i_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) v_{DS}^2 \]

\[ v_{GS} = V_m + V_{OV} \]

\[ v_{GS} = V_m + V_{OV3} \]

\[ v_{GS} = V_m + V_{OV2} \]

\[ v_{GS} = V_m + V_{OV1} \]

\[ v_{GS} \leq v_m \quad \text{(Cutoff)} \]

\[ V_m : \text{threshold voltage of NMOS} \]
Drain Current vs Gate Voltage

In Saturation Region

\[ i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2 \]

\[ = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_m)^2 \]

To experimentally determine \( V_m \):
Measure and plot \( \sqrt{i_D} \) versus \( v_{GS} \)

\[ \sqrt{i_D} = \sqrt{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_m)} \]

\( V_m = \) intercept with horizontal axis
PMOSFET (or simply PMOS)

- **P-channel MOSFET**
  - Current conducted by holes

- **3 terminal device**
  - Source (S): p+ (heavily p-type)
  - Drain (D): p+
  - Gate (G): metal deposited on insulator above channel

- **Substrate (called “Body”)** is a 4th terminal
  - Substrate is n-doped

- Holes is induced in channel when a negative gate voltage is applied

- Holes moves from Source to Drain
  - Current flows from S to D
CMOS (Complementary MOS)

- CMOS is the prevalent IC technology today
- Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a “well”
- PMOS is placed in an “n well” here.
- Alternatively, NMOS can be placed in p well