Summary

\[ I_D = M_n C_{ox} \left( \frac{W}{L} \right) \left( U_{ov} U_{DS} - \frac{1}{2} U_{DS}^2 \right) \]

Threshold Voltage, \( V_{th,n} \)

\[ \frac{\partial I_D}{\partial U_{DS}} = 0 \]

\[ U_{ov} - U_{DS} = 0 \]

when \( U_{DS} = U_{ov} \)

\[ = U_{GS} - V_{th,n} \]

Electron density per \( \text{um}^2 \)

\[ n(x) = C_{ox} \left( U_{GS} - U(x) - V_{th,n} \right) \]

\[ = C_{ox} \left( U_{ov} - U(x) \right) \]

"Pinch-off" the channel

Triode

\[ I_D,_{sat} = \frac{1}{2} M_n C_{ox} \left( \frac{W}{L} \right) U_{ov}^2 \]

\[ I_D = M_n C_{ox} \left( \frac{W}{L} \right) \left( U_{ov} U_{DS} - \frac{1}{2} U_{DS}^2 \right) \]
Pinch-Off

The channel potential at the drain side is \( v_{DS} \).

When \( v_{DS} = v_{OV} \), the local charge density there

\[
\left| \frac{Q}{\text{area}} \right| = C_{ox} \left( v_{GS} - v_{DS} - V_t \right) = C_{ox} \left( v_{OV} - v_{DS} \right) = 0
\]

So the channel is "pinched off" near the Drain.

Once the channel is pinched off, the drain current remains constant:

\[
i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2 = \bar{I}_{D, \text{sat}}
\]

This region, \( v_{DS} > v_{OV} \), is called "Saturation"
Saturation Region \((v_{DS} > v_{OV})\)

When \(0 \leq v_{DS} \leq v_{OV}\)

\[
i_D = \mu_n C_{ox} \frac{W}{L} \left( v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)
\]

This is called the "Triode Region"

When \(v_{DS} > v_{OV}\),

\[
i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2
\]

This is called "Saturation Region"
Full I-V Curves of NMOSFET

- Triode region: \( v_{DS} \leq v_{OV} \)
- Saturation region: \( v_{DS} \geq v_{OV} \)

\[ i_D = \frac{1}{2} k_n \left( \frac{W}{L} \right) V_{OV}^2 \]

\[ v_{DS} = v_{OV} \]

\[ v_{GS} = V_m + V_{OV} \]

\( V_m \): threshold voltage of NMOS
Drain Current vs Gate Voltage

\[ i_D, \ \Delta V_D, \ \Delta V_{GS} = \Delta V_{OV} + \Delta V_{tn} \]

In Saturation Region

\[ i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2 \]

\[ = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_m)^2 \]

To experimentally determine \( V_m \):

Measure and plot \( \sqrt{i_D} \) versus \( v_{GS} \)

\[ \sqrt{i_D} = \sqrt{\frac{1}{2} \mu_n C_{ox} \frac{W}{L}} (v_{GS} - V_m) \]

\( V_m = \) intercept with horizontal axis
PMOSFET (or simply PMOS)

- **P-channel MOSFET**
  - Current conducted by holes
- **3 terminal device**
  - Source (S): p+ (heavily p-type)
  - Drain (D): p+
  - Gate (G): metal deposited on insulator above channel
- **Substrate (called “Body”)** is a 4th terminal
  - Substrate is n-doped
- **Holes is induced in channel when a negative gate voltage is applied**
- **Holes moves from Source to Drain**
  - Current flows from S to D

\[ I_D = \frac{V_W}{L} \left( V_G - \frac{1}{2} V_{DS}^2 \right) \]

For \( \text{PMOS} \) often use 3x width for
CMOS (Complementary MOS)

- CMOS is the prevalent IC technology today
- Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a “well”
- PMOS is placed in an “n well” here.
- Alternatively, NMOS can be placed in p well