University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 120: Signals and Systems
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Direct-Form Realization of Discrete-Time Systems

A causal, linear, time-invariant, discrete-time system can be described by the difference equation:

$$\sum_{k=0}^{N} a_k y[n-k] = \sum_{k=0}^{M} b_k x[n-k] \; , \tag{1}$$

where $x[n]$ is the input and $y[n]$ is the output. We can solve (1) for $y[n]$ to obtain:

$$y[n] = \frac{1}{a_0}\left\{ \sum_{k=0}^{M} b_k x[n-k] - \sum_{k=1}^{N} a_k y[n-k] \right\} \; , \tag{2}$$

which shows that the output $y[n]$ is a weighted sum of $x[n-k], k \geq 0$, the inputs at present and past times, minus a weighted sum of $y[n-k], k > 0$, the outputs at past times.

Form (2) of the difference equation suggests an obvious realization of the system called Direct Form Type I, which is shown in Fig. 1. The elements labeled "S" represent one-sample delays, and are realized using shift registers.
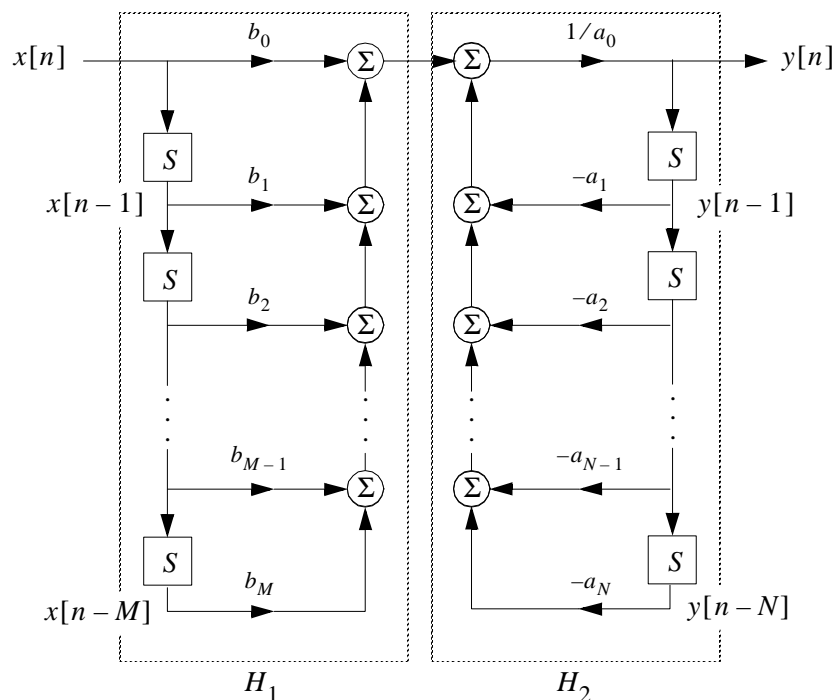

Fig. 1. Direct-form Type I realization of the system described by (1).

We can observe that in Direct form Type I, the overall LTI system H is formed as a cascade of a non-recursive LTI system H_1 and a recursive LTI system H_2. Since these two LTI systems commute, we can reverse the order of H_1 and H_2, obtaining the realization shown in Fig. 2. Examining the system of Fig. 2, we see that each pair of delay elements contains an identical signal, and can be replaced by a single delay element. This leads to the Direct Form Type II realization shown in Fig. 2. Fig. 2 has been drawn under the assumption that $N > M$, in which case, the system requires N delay elements. The case $M \geq N$ is also possible. In general, the Direct Form Type II realization requires $\max(M, N)$ delay elements.
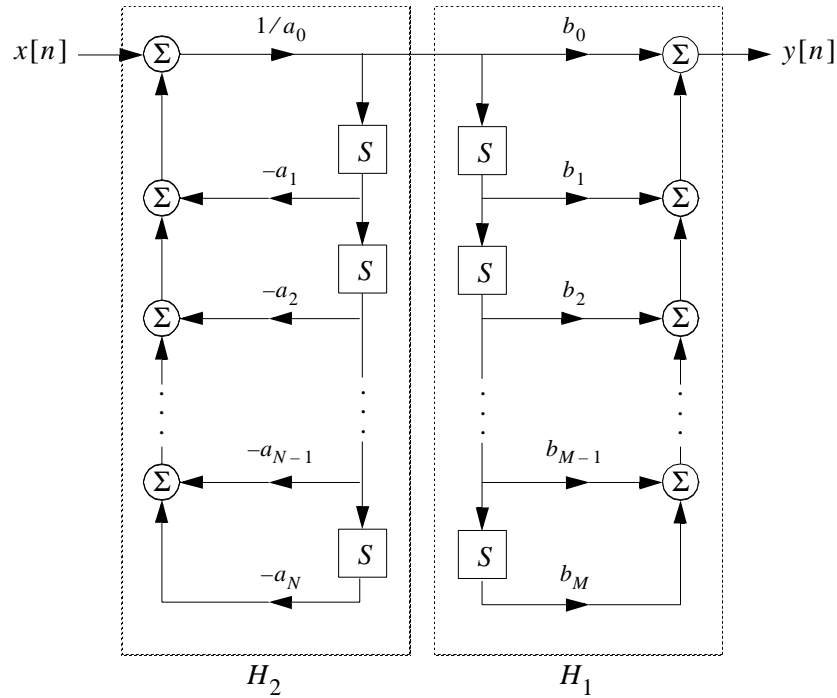

Fig. 2. Realization of the system described by (1), obtained by reversing the order of H_1 and H_2 in Fig. 1.
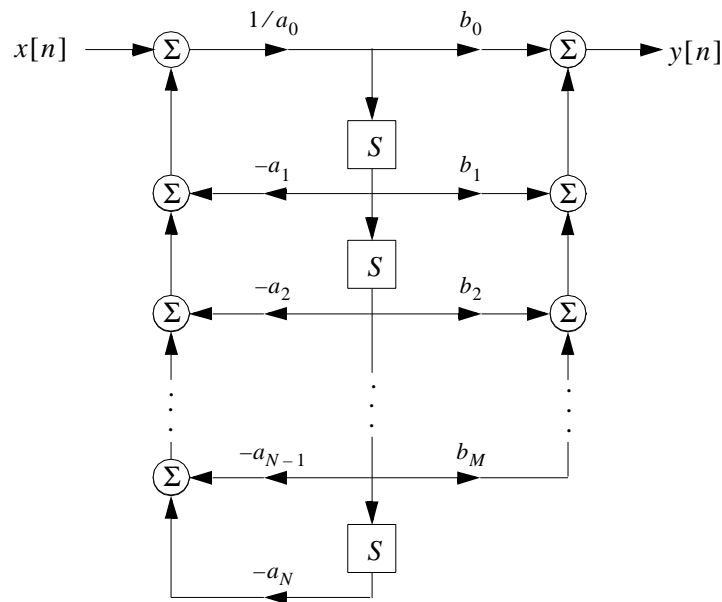

Fig. 3. Direct form Type II realization of the system described by (1), obtained from system of Fig. 2 by merging delay elements.