UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

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INTEGRATED CIRCUIT DEVICES
EECS130, Fall 2006

T.A.s:
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LECTURES
Tuesday and Thursday – 3:30 to 5:00pm in Cory

DISCUSSIONS
Section 101 – Monday 9-10 am, 293 Cory
Section 102 – Wednesday 12-1 pm, 289 Cory
Section 103 – Friday 3-4 pm, 299 Cory

Each student must attend one of these sections. T.A.s will review important concepts covered in
the lectures, lead the discussion of homework, work through sample problems, and present
supplementary materials.

OFFICE HOUR
Professor and T.A.s’ office hour will be announced on EE130 homepage.

TEXT

REFERENCES (On reserve at the Engineering Library)
1. R. S. Muller and T. I. Kamins with Mansun Chan, *Device Electronics for Integrated
   Circuits*, 3rd Edition; Wiley and Sons, Publisher.
   McGraw-Hill.
   (Many students found this series to be very helpful. It is written in clear language.)
5. A. S. Grove, *Physics and Technology of Semiconductor Devices*. (This book also excels
   in clear explanations)
   selling text in its field, this book is at a lower level of difficulty than the others)
COURSE OBJECTIVE
   a. To develop a physical understanding of three important devices: the pn junction, the MOS transistor, and the bipolar transistor.
   b. To explore the general skills for analyzing and designing semiconductor devices.

PREREQUISITES
EECS 40 or EECS 100: Simple pn-junction and MOSFET theory and MOSFET circuit applications. It is assumed that the students know the concept of energy levels in hydrogen atoms.

RELATION TO OTHER COURSES
EECS 105 – The first four weeks of EECS 105 presents a preview or a condensed version of EECS 130
EECS 130 is a prerequisite for EECS 231 (Solid State Devices)
EECS 130 is also helpful (but not a prerequisite) for IC analysis and design courses such as EECS 140, 141, and 142, as well as for the microfabrication technology course EECS 143

CONTENTS:
   A. Review of Semiconductor Properties (2-3 weeks)
      Bond picture, electrons, holes, band picture, density of states, electron statistics, Fermi level, mobility, diffusion, and recombination.
   B. Fabrication Technology (1 week)
      Crystal growth, thermal oxidation, lithography and pattern transfer, dopant addition and diffusion, and chemical vapor deposition.
   C. PN Junction (3 weeks)
      Field and potential in step PN junctions, minority and majority currents, junction capacitance, device model, SCL generation and recombination current.
   D. MOS Devices (4 weeks)
      MOS diodes, flat-band, enhancement, depletion, inversion, CCS, MOSFET I-V characteristics, speed, device model, MOS technology, memory, and CMOS.
   E. Metal-Semiconductor Contact (1 week)
      Energy diagram at interface, I-V characteristics, ohmic contact.
   F. Bipolar Transistor (2 weeks)
      Structure and operation, emitter and base efficiencies, current gain, transit time, device model, built-in field, regions of operations, Ebers-Moll model, IC transistors.
   G. Novel Device Concepts (1 week)
      New device designs/concepts that are being actively explored by various research groups.

HOMEWORK, EXAM & GRADES
Homework will be assigned every Tuesday and will be due the following Tuesday in class. Discussion and collaboration, as opposed to copying, of homework is encouraged. In other words, you are encouraged to discuss the homework with your classmates but you must write your own derivations and do your own calculations, etc. We encourage cooperation rather than competition. Percentages are as follows:

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<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Homework</td>
<td>20%</td>
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<tr>
<td>Two Midterm Exams</td>
<td>20% (each)</td>
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<tr>
<td>Design Project</td>
<td>15%</td>
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<tr>
<td>Final Exam</td>
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http://www.eecs.berkeley.edu/Policies/acad.dis.shtml

EE 130 Home Page:
http://www-inst.eecs.berkeley.edu/~ee130/fa06/