EECS130
Integrated Circuit Devices

Professor Ali Javey
10/25/2007

MOSFETs – Lecture 3

Reading: Chapter 17
Announcements

• The next HW set is due on Thursday of next week.
Quantitative $I_D$-$V_{DS}$ Relationships – 1st attempt

“Square Law”

$$I_D = \frac{Z\mu_n}{L} C_{ox} \left[ (V_G - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \text{for} \quad 0 < V_{DS} < V_{DS,\text{sat}} \quad ; \quad V_G > V_T$$

$I_D$ will increase as $V_{DS}$ is increased, but when $V_G - V_{DS} = V_T$, pinch-off occurs, and current saturates when $V_{DS}$ is increased further. This value of $V_{DS}$ is called $V_{DS,\text{sat}}$, i.e., $V_{DS,\text{sat}} = V_G - V_T$ and the current when $V_{DS} = V_{DS,\text{sat}}$ is called $I_{DS,\text{sat}}$.

$$I_{D,\text{sat}} = \frac{Z \mu C_{ox}}{2L} (V_G - V_T)^2 \quad \text{for} \quad V_D > V_{DS,\text{sat}} \quad ; \quad V_G > V_T$$

Here, $C_{ox}$ is the oxide capacitance per unit area, $C_{ox} = \varepsilon_{ox} / x_{ox}$
The PMOS IV is qualitatively similar to the NMOS IV, but the current is about half as large. Why?
Accumulation vs. depletion mode MOSFET

Enhancement Mode: Transistor is OFF at $V_g = 0$
Depletion Mode: Transistor is ON at $V_g = 0$

Question: How can you control $V_t$?
Question

Plot the $I_D$ vs. $V_{DS}$ characteristics for an NMOS with the following parameters:

- Substrate doping: $10^{16}$ cm$^{-3}$. Oxide thickness = 100 nm
- Gate width = 15 μm; Gate length = 1 μm. Assume $\mu_n = 500$ cm$^2$/Vs

1. Find $C_{ox}$: $C_{ox} = \varepsilon_{ox} / x_{ox} = 33.3$ nF/cm$^2$

2. Find $V_T$: $V_T = 2\phi_F + x_{ox} \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \sqrt{\frac{2qN_A}{\varepsilon_{Si}}} 2\phi_F = 2.15$ V

3. Find $I_D - V_{DS}$ for different values of $V_G$ and plot the graph
Question

Plot the $I_D$ vs. $V_{DS}$ characteristics for an NMOS with the following parameters:

- Substrate doping: $10^{16}$ cm$^{-3}$. Oxide thickness = 100 nm
- Gate width = 15 μm; Gate length = 1 μm. Assume $\mu_n = 500$ cm$^2$/Vs
Effective Mobility

Surface scattering reduces the mobility of the carriers in a MOSFET device as compared to a bulk Si. This is in part due to the gate induced field acceleration of the carriers toward the “rough” Si/SiO₂ interface.
Interface roughness and mobility

Charges carriers are scattered near the surface due to this interface roughness.
Effective Mobility

- phonon scattering
- coulombic scattering
- surface roughness scattering

\((V_g + V_t + 0.2 \text{ V})/6T_{oxe}\) can be shown to be the average vertical electric field in the inversion layer.

Empirically, we often see:

\[
\mu_n = \frac{\mu_0}{1 + \theta(V_G - V_T)}
\]
The variation in mobility as a function of $V_G - V_T$ has profound effect on the I-V characteristics.
Problem with the “Square Law” Approach

- Assumes that gate charge is purely balanced by inversion charge
- Ignores variation in depletion width with length
MOSFET I-V – Bulk Charge Theory

• Accounting for the depletion width, we have:

\[ Q_{inv}(y) = -C_{ox}(V_G - V_T - \phi) + qN_A[W(y) - W_T] \]

\[ W(y) = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{qN_A}}(2\phi_F + \phi) \]

\[ W_T = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{qN_A}}(2\phi_F) \]

• So, we finally find (again in the linear region):

\[ I_D = -\frac{Z}{L} \mu_n C_{ox} \left[(V_G - V_T)W_D - \frac{V_D^2}{2} - \frac{4}{3}V_W\phi_F \left(1 + \frac{V_D}{2\phi_F}\right)^{\frac{3}{2}} - \left(1 + \frac{3V_D}{4\phi_F}\right)\right] \]
Threshold and Subthreshold

\[ I_D = \mu_{\text{eff}} C_G \frac{W}{L'} (V_{GS} - V_T) V_{DS} \]

\[ = \frac{V_{DS}}{R_{CH}} \]

slope gives mobility

mobility degradation at high \( V_{GS} \)

\( V_{DS} \) small

actual

subthreshold conduction

\( V_T \)

intercept gives \( V_T \)
**Subthreshold Current**

- The leakage current that flows at $V_g < V_t$ is called the subthreshold current. Previously we had assumed that current is zero, but in reality that’s not the case.

![Graph showing $I_{ds}$ vs $V_{gs}$ for PMOS and NMOS with $V_{DS} = 0.05V, 1.2V$]

- The current at $V_{gs} = 0$ and $V_{ds} = V_{dd}$ is called $I_{off}$.

*Intel, T. Ghani et al., IEDM 2003*

90nm technology.
Gate length: 45nm for NMOS, 50nm for PMOS
• Subthreshold current $\propto n_s$ (surface inversion carrier concentration)

• $n_s \propto e^{q\phi_s/kT}$

• $\phi_s$ (surface potential) varies with $V_g$ through a capacitor network

\[
\frac{d\phi_s}{dV_g} = \frac{C_{\text{oxe}}}{C_{\text{oxe}} + C_{\text{dep}}} = \frac{1}{\eta}
\]

In subthreshold, $\phi_s = \text{constant} + V_g/\eta$
Subthreshold Leakage Current

\[ I_{ds} \propto n_s \propto e^{q\tan g V_g / n T} \propto e^{q(\text{constant} + V_g / \eta)} / kT \propto e^{qV_g / \eta kT} \]

\[ \frac{C_{ox}}{C_{dep}} \]

\[ V_G \]

\[ \varphi_s \]

\[ \eta = 1 + \frac{C_{dep}}{C_{oxe}} \]

- Subthreshold current changes 10x for \( \eta \cdot 60mV \) change in \( V_g \).

Reminder: 60mV is \((\ln 10) \cdot kT / q\)

- Subthreshold swing, \( S \): the change in \( V_{gs} \) corresponding to 10x change in subthreshold current. \( S = \eta \cdot 60mV \), typically 80-100mV
Subthreshold Leakage Current

- Practical definition of $V_t$: the $V_{gs}$ at which $I_{ds} = 100 \text{nA} \times \frac{W}{L}$

$$\Rightarrow I_{\text{subthreshold}}(nA) \approx 100 \times \frac{W}{L} \times e^{q(V_g-V_t)\eta kT} = 100 \times \frac{W}{L} \times 10^{(V_g-V_t)/S}$$

$I_{off}(nA) = 100 \times \frac{W}{L} \times 10^{-V_t/s}$ is determined only by $V_t$ and subthreshold swing.
Subthreshold Swing ($S$)

- Smaller $S$ is desirable (lower $I_{off}$ for a given $V_t$). Minimum possible value of $S$ is 60mV/dec.

- What are 3 ways to lower swing? $S = 60mV \cdot \left(1 + \frac{C_{dep}}{C_{oxe}}\right)$

- Limitations
**Velocity Saturation**

\[
v = \frac{\mu_s \varepsilon}{1 + \frac{\varepsilon}{\varepsilon_{sat}}}
\]

\[\varepsilon \ll \varepsilon_{sat} : v = \mu_s \varepsilon\]

\[\varepsilon \gg \varepsilon_{sat} : v = \mu_s \varepsilon_{sat}\]

- velocity saturation has large and deleterious effect on the \(I_{on}\) of MOSFETS