Announcements

- The next HW set is due on Thursday.
- Midterm 2 is next week!!!!
Threshold and Subthreshold

\[ I_D = \mu_{\text{eff}} C_G \frac{W}{L'} (V_{GS} - V_T) V_{DS} \]

\[ = \frac{V_{DS}}{R_{CH}} \]

slope gives mobility

mobility degradation at high \( V_{GS} \)

\( V_{DS} \) small

actual

subthreshold conduction

intercept gives \( V_T \)
Subthreshold Current

- The leakage current that flows at $V_g < V_t$ is called the subthreshold current. Previously we had assumed that current is zero, but in reality that’s not the case.

![Graph showing $I_{ds}$ vs $V_{gs}$ for PMOS and NMOS with $V_{ds}$ between -1.2 to 1.2 V and $V_{ds}$ between 0.05V to 1.2V.]

- The current at $V_{gs} = 0$ and $V_{ds} = V_{dd}$ is called $I_{off}$.

Intel, T. Ghani et al., IEDM 2003
90nm technology.
Gate length: 45nm for NMOS, 50nm for PMOS
• Subthreshold current $\propto n_s$ (surface inversion carrier concentration)

• $n_s \propto e^{q\phi_s/kT}$

$\phi_s$ (surface potential) varies with $V_g$ through a capacitor network

$\frac{d\phi_s}{dV_g} = \frac{C_{oxe}}{C_{oxe} + C_{dep}} = \frac{1}{\eta}$

In subthreshold, $\phi_s = \text{constant} + V_g/\eta$
**Subthreshold Leakage Current**

\[ I_{ds} \propto n_s \propto e^{q\varphi_s / kT} \propto e^{q(\text{constant} + V_{gs} / \eta) / kT} \propto e^{qV_{gs} / \eta kT} \]

\[ I_{ds} \propto e^{qV_{gs} / \eta kT} \]

\[ \eta = 1 + \frac{C_{dep}}{C_{oxe}} \]

- Subthreshold current changes 10x for $\eta \cdot 60 mV$ change in $V_g$.
  
  Reminder: $60 mV$ is $(\ln 10) \cdot kT / q$

- Subthreshold swing, $S$: the change in $V_{gs}$ corresponding to 10x change in subthreshold current. $S = \eta \cdot 60 mV$, typically 80-100mV
Subthreshold Leakage Current

• Practical definition of $V_t$: the $V_{gs}$ at which $I_{ds} = 100 \text{nA} \times \frac{W}{L}$

$$\Rightarrow I_{subthreshold} (nA) \approx 100 \times \frac{W}{L} \times e^{q(V_g - V_t) \eta kT} = 100 \times \frac{W}{L} \times 10^{(V_g - V_t) / S}$$

$I_{off} (nA) = 100 \times \frac{W}{L} \times 10^{-V_t / S}$

is determined only by $V_t$ and subthreshold swing.
**Subthreshold Swing (S)**

- Smaller S is desirable (lower $I_{\text{off}}$ for a given $V_t$). Minimum possible value of S is 60mV/dec.

- What are 3 ways to lower swing?  
  
  $$S = 60mV \cdot \left(1 + \frac{C_{\text{dep}}}{C_{\text{oxe}}} \right)$$

- Limitations
Subthreshold Swing ($S$)

The theoretical limit for $S$ for a MOSFET is 60 mV/decade. New device concepts are being explored to make new generation of transistors that beat the 60 mV/decade limit.
Velocity Saturation

\[ v = \frac{\mu_s E}{1 + \frac{E}{E_{sat}}} \]

- velocity saturation has large and deleterious effect on the \( I_{on} \) of MOSFETS
Velocity Saturation

As the channel length, L, is reduced while the supply voltage is not, the tangential electric field will increase, and the carrier velocity may saturate. $\varepsilon_c \approx 10^4 \, \text{V/cm}$ for electrons. Hence for N-channel MOSFET with $L < 1 \, \mu m$, velocity saturation causes the channel current to reach saturation before $V_D = V_G - V_T$. Instead of $I_{DSAT}$ being proportional $(V_G - V_T)^2$ it is linearly proportional to $(V_G - V_T)$ and is approximately given by

$$I_{D_{sat}} = W C_{ox} (V_G - V_T)v_{sat}$$

where $v_{sat}$ is the carrier saturation velocity.
Measured MOSFET IV – Velocity Saturation

What is the main difference between the $V_g$ dependences of the long- and short-channel length IV curves?
Ballistic Devices

- If the channel is short enough (below the mean free path length scales), then the carriers can travel from source to drain without going through any significant scattering events. This is called ballistic transport. Carriers can often gain an average velocity over $v_{\text{sat}}$. This phenomena is known as velocity overshoot.

- State-of-the-art Si MOSFETs are operating at $\sim 40\%$ the ballistic limit.
Series Resistance of S/D

- So far we have been assuming that there is no potential drop in S/D. For miniaturized/scaled devices that is not the case and the parasitic resistance of S/D plays an important role in the IV characteristics.
Series resistance is highly undesirable and can cause severe performance degradation.
**MOSFET Technology Scaling**

**Technology Scaling – Small is Beautiful**

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<td>0.5 μm</td>
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<td>0.18 μm</td>
<td>0.13 μm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
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- New technology node every three years or so. Defined by minimum metal line width.
- All feature sizes, e.g. gate length, are ~70% of previous node.
MOSFET Technology Scaling

Research Options:
Non-planar Tri-gate
III-V, CNT, NW
**$V_t$ Roll-off**

- $V_t$ roll-off: $V_t$ decreases with decreasing $L_g$.
- It determines the minimum acceptable $L_g$ because $I_{off}$ is too large if $V_t$ becomes too small.

*K. Goto et al., (Fujitsu) IEDM 2003*  
65nm technology. EOT=1.2nm, $V_{dd}=1V$
Why Does $V_t$ Decrease with $L$? – Potential Barrier Concept

- When $L$ is small, smaller $V_g$ is needed to reduce the barrier to 0.2V, i.e. $V_t$ is smaller.
- $V_t$ roll-off is greater for shorter $L$
Energy-Band Diagram from Source to Drain

- \( L \) dependence

- \( V_{ds} \) dependence
Reducing the Gate Insulator Thickness and $T_{oxe}$

- Oxide thickness has been reduced over the years from 300nm to 1.2nm.
- Why reduce oxide thickness?
  - Larger $C_{ox}$ to raise $I_{on}$
  - Reduce subthreshold swing
  - Control $V_t$ roll-off
- Thinner is better. However, if the oxide is too thin
  - Breakdown due to high electric field
  - Leakage current
Tunneling Leakage Current

- For SiO₂ films thinner than 1.5nm, tunneling leakage current has become the limiting factor.
- HfO₂ has several orders lower leakage for the same EOT.
Replacing $\text{SiO}_2$ with $\text{HfO}_2$---High-\textit{k} Dielectric

- $\text{HfO}_2$ has a relative dielectric constant ($k$) of $\sim 24$, six times large than that of $\text{SiO}_2$.
- For the same EOT, the $\text{HfO}_2$ film presents a much thicker (albeit a lower) tunneling barrier to the electrons and holes.
- $\text{Toxe}$ can be further reduced by introducing metal-gate technology since the poly-depletion effect is eliminated.

(After W. Tsai et al., IEDM'03)
Challenges of High-K Technology

• The challenges of high-k dielectrics are
  – chemical reactions between them and the silicon substrate and gate,
  – lower surface mobility than the Si/SiO₂ system
  – too low a $V_t$ for P-channel MOSFET (as if there is positive charge in the high-k dielectric).

• A thin SiO₂ interfacial layer may be inserted between Si-substrate and high-k film.