EECS130
Integrated Circuit Devices

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MOSFETs– Lecture 5
Announcements

• HW7 set is due now

• HW8 is assigned, but will not be collected/graded.
MOSFET Technology Scaling

Technology Scaling – Small is Beautiful

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</thead>
<tbody>
<tr>
<td>Technology Generation</td>
<td>0.5 μm</td>
<td>0.35 μm</td>
<td>0.25 μm</td>
<td>0.18 μm</td>
<td>0.13 μm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
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- New technology node every three years or so. Defined by minimum metal line width.
- All feature sizes, e.g. gate length, are ~70% of previous node.
$V_t$ Roll-off

- $V_t$ roll-off: $V_t$ decreases with decreasing $L_g$.
- It determines the minimum acceptable $L_g$ because $I_{off}$ is too large if $V_t$ becomes too small.

K. Goto et al., (Fujitsu) IEDM 2003  65nm technology. EOT=1.2nm, $V_{dd}=1$V
Why Does $V_t$ Decrease with $L$? – Potential Barrier Concept

- When $L$ is small, smaller $V_g$ is needed to reduce the barrier to 0.2V, i.e. $V_t$ is smaller.
- $V_t$ roll-off is greater for shorter $L$
Energy-Band Diagram from Source to Drain

- L dependence

- $V_{ds}$ dependence

$V_{ds} = 0$

$V_{ds} = V_{dd}$

long channel

short channel
How to Reduce $W_{\text{dep}}$

- $W_{\text{dep}}$ can be reduced by increasing $N_{\text{body}}$

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_{\text{body}}2\varepsilon_s2\phi_B}}{C_{ox}} = V_{fb} + 2\phi_B + \frac{2\varepsilon_s2\phi_B}{C_{ox}W_{\text{dep}}}$$

- If $N_{\text{body}}$ is increased, $C_{ox}$ should be increased in order to keep $V_t$ the same.
- $W_{\text{dep}}$ can be reduced in proportion to $T_{ox}$. 
Reducing the Gate Insulator Thickness and $T_{\text{oxe}}$

- Oxide thickness has been reduced over the years from 300nm to 1.2nm.
- Why reduce oxide thickness?
  - Larger $C_{\text{ox}}$ to raise $I_{\text{on}}$
  - Reduce subthreshold swing
  - Control $V_t$ roll-off
- Thinner is better. However, if the oxide is too thin
  - Breakdown due to high electric field
  - Leakage current
Tunneling Leakage Current

• For SiO$_2$ films thinner than 1.5nm, tunneling leakage current has become the limiting factor.
• HfO$_2$ has several orders lower leakage for the same EOT.
Replacing $SiO_2$ with $HfO_2$---High-$k$ Dielectric

- $HfO_2$ has a relative dielectric constant ($k$) of ~24, six times large than that of $SiO_2$.
- For the same EOT, the $HfO_2$ film presents a much thicker (albeit a lower) tunneling barrier to the electrons and holes.
- $Toxe$ can be further reduced by introducing metal-gate technology since the poly-depletion effect is eliminated.

(After W. Tsai et al., IEDM'03)
Challenges of High-K Technology

• The challenges of high-k dielectrics are
  – chemical reactions between them and the silicon substrate and gate,
  – lower surface mobility than the Si/SiO$_2$ system
  – too low a $V_t$ for P-channel MOSFET (as if there is positive charge in the high-k dielectric).

• A thin SiO$_2$ interfacial layer may be inserted between Si-substrate and high-k film.
More Scalable Device Structures

- Vertical Scaling is important. For example, reducing $T_{ox}$ gives the gate excellent control of Si surface potential.
- But, the drain could still have more control than the gate along another leakage current path that is some distance below the Si surface. (Right figure.)
Ultra-Thin-Body (UTB) MOSFET

- MOSFET built on very thin silicon film on an insulator (SiO₂).
- Since the silicon film is very thin, perhaps less than 10nm, no leakage path is very far from the gate.
**New Structure I—Ultra-Thin-Body MOSFET**

- The subthreshold leakage is reduced as the silicon film is made thinner.

\[
\begin{align*}
T_{ox} &= 1.5\text{nm}, \quad N_{sub} = 1\times10^{15}\text{cm}^{-3}, \\
V_{dd} &= 1\text{V}, \quad V_{gs} = 0
\end{align*}
\]
Preparation of Silicon-on-Insulator (SOI) Substrate

- Initial Silicon wafer A and B
- Oxidize wafer A to grow SiO2
- Implant hydrogen into wafer A
- Place wafer A, upside down, over wafer B.
- A low temperature annealing causes the two wafers to fuse together.
- Apply another annealing step to form H₂ bubbles and split wafer A.
- Polish the surface and the SOI wafer is ready for use.
- Wafer A can be reused.
Due to the high cost of SOI wafers, only some microprocessors, which command high prices and compete on speed, have embraced this technology.

In order to benefit from the UTB concept, Si film thickness must be aggressively reduced to $\approx L_g/4$. 
New Structure II--Multi-Gate MOSFET and FinFET

• The second way of eliminating deep leakage paths is to provide gate control from more than one side of the channel.
• The Si film is very thin so that no leakage path is far from one of the gates.
• Because there are more than one gates, the structure may be called multi-gate MOSFET.
FinFET

- One multi-gate structure, called **FinFET**, is particularly attractive for its simplicity of fabrication.
- Called FinFET because its silicon body resembles the back fin of a fish.
- The channel consists of the two vertical surfaces and the top surface of the fin.

**Question:** What is the channel width, $W$?

**Answer:** The sum of twice the fin height and the width of the fin.
**FinFET Process Flow**

1. **SOI Substrate**
2. **Fin Patterning**
3. **Poly Gate Deposition/Litho**
4. **Gate Etch**
5. **Spacer Formation**
6. **S/D Implant + RTA**
7. **Silicidation**

- **BOX**
- **Si Fin**
- **Si$_3$N$_4$ Spacer**
- **Resist**
- **Poly**
- **NiSi**
Variations of FinFET

- **Tall FinFET** has the advantage of providing a large $W$ and therefore large $I_{on}$ while occupying a small footprint.
- **Short FinFET** has the advantage of less challenging lithography and etching.
- **Nanowire FinFET** gives the gate even more control over the silicon wire by surrounding it.
Tall FinFET with $L_g = 10\text{nm}$

B. Yu et al., IEDM 2002
Nanowire FinFET

5nm Gate Length
F. Yang et al., 2004 VLSI Tech Symp.
Device Simulation and Process Simulation

- **Device Simulation**
  - Commercially available computer simulation tools can solve all the equations presented in this book simultaneously with few or no approximations.
  - Device simulation provides quick feedback about device design before long and expensive fabrication.

- **Process Simulation**
  - Inputs to process simulation: lithography mask pattern, implantation dose and energy, temperatures and times for oxidization and annealing steps, etc.
  - The process simulator generates a 2-D or 3-D structures with all the deposited or grown and etched thin films and doped regions.
  - This output may be fed into a device simulator as input together with applied voltages.
Example of Device Simulation---

Density of Inversion Charge in the Cross-Section of a FinFET Body

- The inversion layer has a significant thickness ($T_{ch}$).
- There are more subthreshold inversion electrons at the corners.

C.-H. Lin et al., 2005 SRC TECHCON
Example of Process Simulation

- FinFET Process

The small figures only show 1/4 of the complete FinFET—the quarter farthest from the viewer.

Manual, Taurus Process, Synopsys Inc.