UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering and Computer Sciences

INTEGRATED CIRCUIT DEVICES
EECS130 Fall 2009

Prof. Chenming Hu, 502 Cory Hall, (510) 642-3393, hu@eecs.berkeley.edu
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LECTURES
Tuesday and Thursday – 12:30 to 2pm in 241Cory

DISCUSSIONS
Section 101: Monday 9:00-10:00A, 521 Cory
Section 102: Wednesday 12:00-1:00P, 285 Cory
Each student must attend one of these sections. TAs will review selected topics introduced in the lectures, lead the discussion of homework, work through sample problems, and present supplementary materials.

Q&A SESSIONS
Tuesday 5:00-6:00, Hogan Room, 521 Cory Hall
OFFICE HOURS
Professor Hu: Thursday 5-6pm, 502 Cory Hall (Office Hour)
Shijing Yao: Monday 10:00A-11:00A, 557 Cory
Sriramkumar: Monday 11:00A-12:00P, 557 Cory

TEXT
"Modern Semiconductor Device for Integrated Circuits" Chenming Hu, Prentice Hall, 2009.

COURSE OBJECTIVE
a. To develop a sound understanding of devices such as the pn junction, the bipolar transistor and especially the MOS transistor, as well as solar cells and imagers.
b. To develop the general skills for analyzing and designing semiconductor devices.
PREREQUISITES
EECS 40 or EECS 100: Basic concepts of circuits, energy levels in hydrogen atoms, and electrons as particles and waves.
RELATION TO OTHER COURSES
EECS 105 – The first four weeks of EECS 105 presents a preview or a condensed version of EECS 130
EECS 130 is a prerequisite for the following courses: EECS131: Semiconductor Electronics (may be taken concurrently) and EECS231: Solid State Devices
EECS 130 is also helpful (but not a prerequisite) for IC analysis and design courses such as EECS 140, 141, and 142, as well as for the microfabrication technology course EECS 143

CONTENTS:

A. Review of Semiconductor Properties (2 weeks)
Bond picture, electrons, holes, band picture, density of states, electron statistics, Fermi level, mobility, diffusion, and recombination.

B. Fabrication Technology (1 week)
Crystal growth, thermal oxidation, lithography and pattern transfer, dopant addition and diffusion, and chemical vapor deposition.

C. PN Junction (3 weeks)
Field and potential in step PN junctions, minority and majority currents, junction capacitance, device model, SCL generation and recombination current, applications to solar cells and light emitting diodes.

D. Metal-Semiconductor Contact (1 week)
Energy diagram at interface, I-V characteristics, ohmic contact.

E. MOS Devices (5 weeks)
MOS diodes, flat-band, enhancement, depletion, inversion, CCS, MOSFET I-V characteristics, speed, device model, MOS technology, memory, and CMOS.

F. Bipolar Transistor (2 weeks)
Structure and operation, emitter and base efficiencies, current gain, transit time, device model, built-in field, regions of operations, Ebers-Moll model, IC transistors.

HOMEWORK, EXAM & GRADES

Homework will be assigned every Thursday and will be due the following Thursday in class. Discussion and collaboration, as opposed to copying, of homework is encouraged. In other words, you are encouraged to discuss the homework with your classmates but you must write your own derivations and do your own calculations, etc. Do not hesitate to ask Prof. Hu and or the T.A.s for clarifications and hints for the homework problems during Discussion Session and Office hours.

We encourage cooperation rather than competition. Percentages are as follows:

- Homework 20%
- Two Midterm Exams 20% (each)
- Design Project 15%
- Final Exam 25%

REFERENCES (On reserve at the Engineering Library)

1. R. S. Muller and T. I. Kamins with Mansun Chan, Device Electronics for Integrated Circuits, 3rd Edition; Wiley and Sons, Publisher.
2. B. L. Anderson and R. L. Anderson, Fundamentals of Semiconductor Devices, McGraw-Hill.
3. R. F. Pierret, G. W. Neudeck, Modular Series on Solid State Devices, Vol. 1, 2, 3, 4, 7. (Many students found this series to be very helpful. It is written in clear language.)
4. R. F. Pierret, Semiconductor Device Fundamentals, Addison Wesley, 1996.
5. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, Prentice Hall (This book is at a lower level of difficulty than the others)

EECS Department Policy on Academic Dishonesty:

http://www.eecs.berkeley.edu/Policies/acad.dis.shtml
EE 130 Home Page: http://www-inst.eecs.berkeley.edu/~ee130