Lecture #23

ANNOUNCEMENTS

• Quiz #5 will be given at the beginning of class on Thursday (4/17)
  – topics to be covered: BJT transient response, MOS band diagrams
  – closed book; 5 pages of notes + calculator allowed

OUTLINE

• MOS non-idealities (cont.)
• \( V_T \) adjustment
• MOSFET structure and operation

Reading: Course Reader Chapter 3.1
(Textbook Chapters 18.3, 17.1-2)

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Poly-Si Gate Depletion

• A heavily doped film of polycrystalline silicon (poly-Si) is typically employed as the gate-electrode material in modern MOS devices.

\[ \text{NMOS} \]
\[
\begin{array}{c}
N^+ \text{ poly-Si} \\
P^+ \text{ poly-Si} \\
P^- \text{ poly-Si} \\
\end{array}
\]

\[ \text{PMOS} \]
\[
\begin{array}{c}
P^+ \text{ poly-Si} \\
N^- \text{ poly-Si} \\
N^+ \text{ poly-Si} \\
\end{array}
\]

– There are practical limits to the electrically active dopant concentration (usually less than \( 1 \times 10^{20} \text{ cm}^{-3} \))
  => The gate must be considered as a semiconductor, rather than a metal
How can gate depletion be minimized?

- MOS Band Diagram with Gate Depletion

Si biased to inversion:

- $V_G$ is effectively reduced:
  \[ Q_{\text{inv}} = C_{\alpha} (V_G - V_{\text{poly}} - V_T) \]
  \[ W_{\text{poly}} = \sqrt{\frac{2 \varepsilon_{\text{Si}} V_{\text{poly}}}{qN_{\text{poly}}}} \]

- How can gate depletion be minimized?

- Gate Depletion Effect

Gauss’s Law dictates

\[ W_{\text{poly}} = \frac{\varepsilon_{\text{SiO}_2} C_{\alpha} C_{\text{poly}}}{qN_{\text{poly}}} \]

- $t_{\alpha}$ is effectively increased:

\[ C = \left( \frac{1}{C_{\alpha}} + \frac{1}{C_{\text{poly}}} \right)^{-1} = \left( \frac{t_{\alpha}}{\varepsilon_{\text{SiO}_2}} + \frac{W_{\text{poly}}}{\varepsilon_{\text{Si}}} \right)^{-1} \]

\[ = \frac{\varepsilon_{\text{SiO}_2}}{t_{\alpha} + (W_{\text{poly}} / 3)} \]

\[ Q_{\text{inv}} = (V_G - V_T) \cdot \frac{\varepsilon_{\text{SiO}_2}}{t_{\alpha} + (W_{\text{poly}} / 3)} \]
Example: GDE

$V_{ox}$, the voltage across a 2 nm thin oxide, is 1 V. The $n^+$ poly-Si gate active dopant concentration $N_{poly}$ is $8 \times 10^{19} \text{ cm}^{-3}$ and the Si substrate doping concentration $N_A$ is $10^{17} \text{ cm}^{-3}$.

Find (a) $W_{poly}$, (b) $V_{poly}$, and (c) $V_G$.

**Solution:**

(a) $W_{poly} = \varepsilon_{ox} \rho_{ox} / qN_{poly} = \varepsilon_{ox} V_{ox} / t_{ox} qN_{poly}$

$$= \frac{3.9 \times 8.85 \times 10^{-14} \text{ (F/cm)} \cdot 1 \text{ V}}{2 \times 10^{-7} \text{ cm} \cdot 1.6 \times 10^{-19} \text{ C} \cdot 8 \times 10^{19} \text{ cm}^{-3}}$$

$$= 1.3 \text{ nm}$$

(b) $W_{poly} = \sqrt{\frac{2\varepsilon_{Si} V_{poly}}{qN_{poly}}}$

$$V_{poly} = qN_{poly} W_{poly}^2 / 2\varepsilon_{Si} = 0.11 \text{ V}$$

(c) $V_G = V_{FB} + 2\psi_B + V_{ox} + V_{poly}$

$$V_{FB} = -\left[\frac{E_G}{2q} + \frac{kT}{q} \ln \left(\frac{N_A}{n_i}\right)\right] = -0.98 \text{ V}$$

$$V_G = -0.98 \text{ V} + 0.84 \text{ V} + 1 \text{ V} + 0.11 \text{ V} = 0.97 \text{ V}$$

*Is the loss of 0.11V significant?*
The average inversion-layer location below the Si/SiO₂ interface is called the inversion-layer thickness, $T_{\text{inv}}$.

$$T_{\text{inv}} = t_{\text{ox}} + \frac{W_{\text{poly}}}{3} + \frac{T_{\text{inv}}}{3}$$ at $V_G = V_{dd}$

$(V_G + V_T)/T_{\text{ox}}$ can be shown to be the average electric field in the inversion layer. $T_{\text{inv}}$ of holes is larger than that of electrons because of the difference in effective masses.
**Effective Oxide Capacitance**

\[ T_{oxe} = t_{ox} + W_{poly} / 3 + T_{inv} / 3 \]

\[ Q_{inv} = C_{oxe} (V_G - V_T) \]

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**V_T Adjustment by Ion Implantation**

- In modern IC fabrication processes, the threshold voltages of MOS transistors are adjusted by ion implantation:
  - A relatively small dose \( N_i \) (units: ions/cm\(^2\)) of dopant atoms is implanted into the near-surface region of the semiconductor
  - When the MOS device is biased in depletion or inversion, the implanted dopants add to the dopant-ion charge near the oxide-semiconductor interface.

\[ \Delta V_T = -qN_i \frac{C_{ox}}{C_{ox}} \quad N_i > 0 \text{ for donor atoms} \]
\[ \quad N_i < 0 \text{ for acceptor atoms} \]
**V_T Adjustment by Back Biasing**

- In some IC products, $V_T$ is dynamically adjusted by applying a back bias:
  - When a MOS capacitor is biased into inversion, a pn junction exists between the surface and the bulk.
  - If the inversion layer contacts a heavily doped region of the same type, it is possible to apply a bias to this pn junction.

![Diagram of MOS capacitor with p-type Si, N+ poly-Si, and SiO2 layers with annotations](image)

- $V_G$ biased so surface is inverted
- Inversion layer contacted by N+ region
- Bias $V_C$ applied to channel
  - Reverse bias $V_B-V_C$ applied between channel & body

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**Effect of $V_{CB}$ on $V_s$, $V_T$**

- Application of reverse bias -> non-equilibrium
  - 2 Fermi levels (one for n-region, one for p-region)
    - Separation = $qV_{BC} \Rightarrow V_s$ increased by $V_{CB}$
  - Reverse bias widens $W_{d}$, increases $Q_{dep}$
    - $Q_{inv}$ decreases with increasing $V_{CB}$, for a given $V_{GB}$

$$V_T = V_{FB} + V_C + 2\psi_B + \sqrt{2qN_A\varepsilon_S(2\psi_B + V_{CB})} \over C_{ox}$$

Spring 2003  
EE130 Lecture 23, Slide 11

Spring 2003  
EE130 Lecture 23, Slide 12
In 1935, a British patent was issued to Oskar Heil. A working MOSFET was not demonstrated until 1955.

Modern Field Effect Transistor (FET)

- An electric field is applied normal to the surface of the semiconductor (by applying a voltage to an overlying electrode), to modulate the conductance of the semiconductor

→ Modulate drift current flowing between 2 contacts ("source" and "drain") by varying the voltage on the "gate" electrode

N-channel MOSFET:
MOSFET $I$-$V$ Characteristic

Basic n-channel MOSFET structure and $I$-$V$ characteristics

What is desirable: large $I_{on}$, small $I_{off}$

Two ways of representing a MOSFET:

Circuit Symbol  Simple Switch

Source  Drain  Gate  Source  Drain  Gate

Spring 2003  EE130 Lecture 23, Slide 15
Enhancement Mode vs. Depletion Mode

- Enhancement mode:
  - For current to flow, $V_{GS} > V_T$
  - Enhancement mode: $V_T > 0$
  - Depletion mode: $V_T < 0$
    - Transistor is ON when $V_G=0V$

- Depletion mode:
  - For current to flow, $V_{GS} < V_T$
  - Enhancement mode: $V_T < 0$
  - Depletion mode: $V_T > 0$
    - Transistor is ON when $V_G=0V$

N-channel vs. P-channel

<table>
<thead>
<tr>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>N+ poly-Si</td>
<td>P+ poly-Si</td>
</tr>
<tr>
<td>N+</td>
<td>P+</td>
</tr>
<tr>
<td>P-type Si</td>
<td>n-type Si</td>
</tr>
</tbody>
</table>

- For current to flow, $V_{GS} > V_T$
- Enhancement mode: $V_T > 0$
- Depletion mode: $V_T < 0$
  - Transistor is ON when $V_G=0V$

- For current to flow, $V_{GS} < V_T$
- Enhancement mode: $V_T < 0$
- Depletion mode: $V_T > 0$
  - Transistor is ON when $V_G=0V$
When $V_g = V_{dd}$, the NFET is on and the PFET is off.
When $V_g = 0$, the PFET is on and the NFET is off.

A CMOS inverter is made of a PFET pull-up device and a NFET pull-down device.
This two-input NAND gate and many other logic gates are extensions of the basic inverter.