Chapter 3
Silicon Device Fabrication Technology

Over 10^{15} transistors (or 100,000 for every person in the world) are manufactured every year.

VLSI (Very Large Scale Integration)
ULSI (Ultra Large Scale Integration)

Variations of this versatile technology are used for flat-panel displays, micro-electro-mechanical systems (***MEMS***), and even DNA chips for DNA screening...

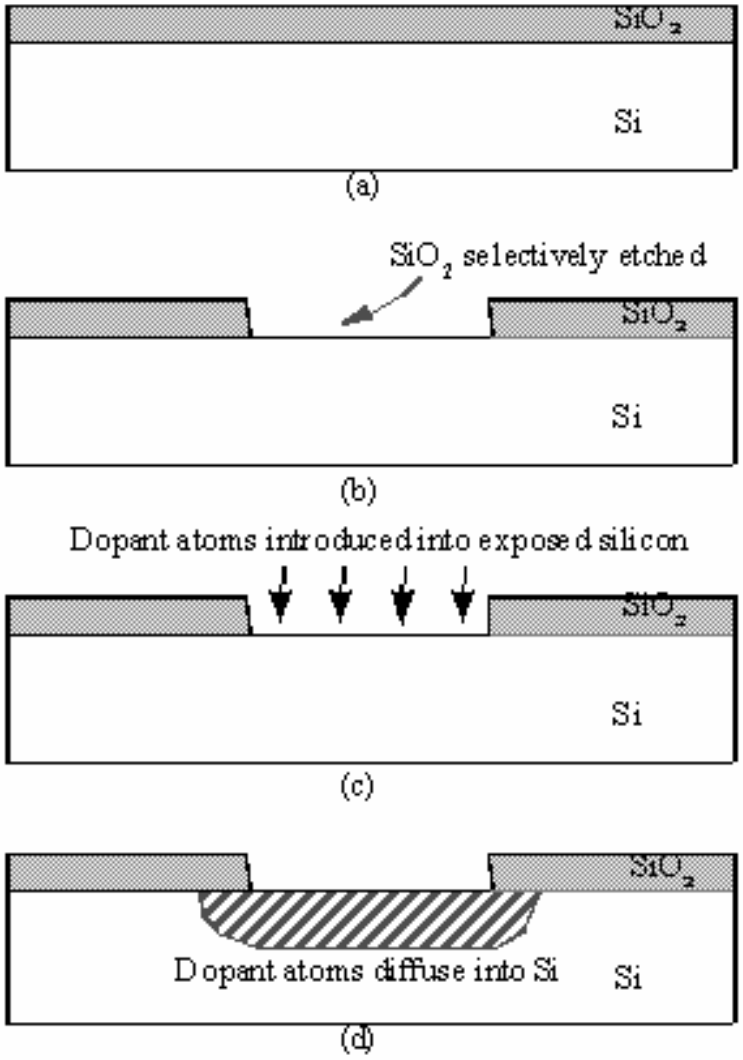
3.1 Introduction to Device Fabrication

Oxidation

Lithography & Etching

Ion Implantation

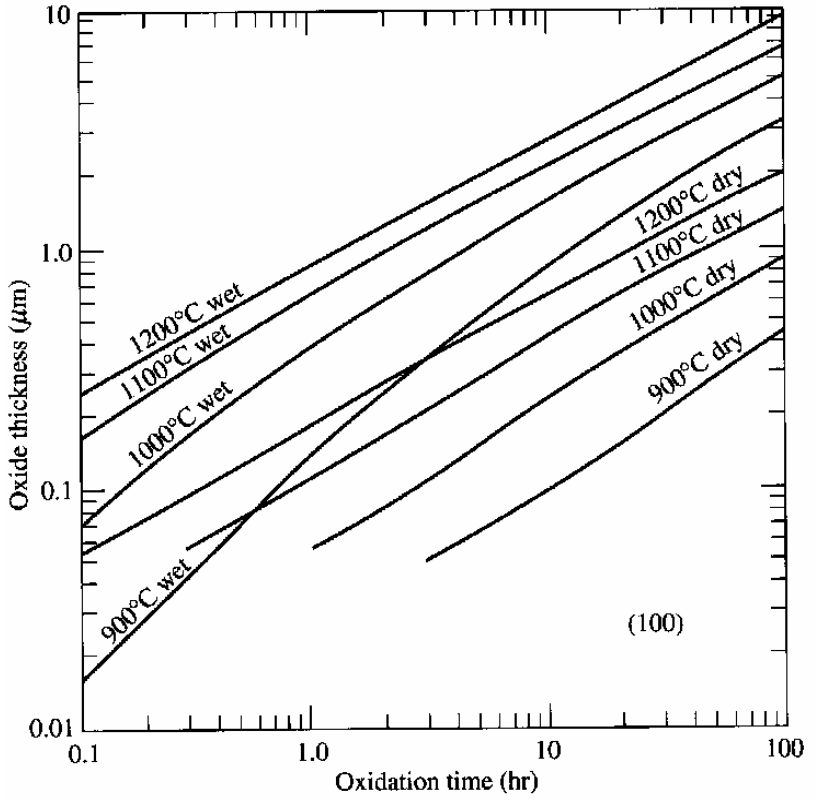
Annealing & Diffusion



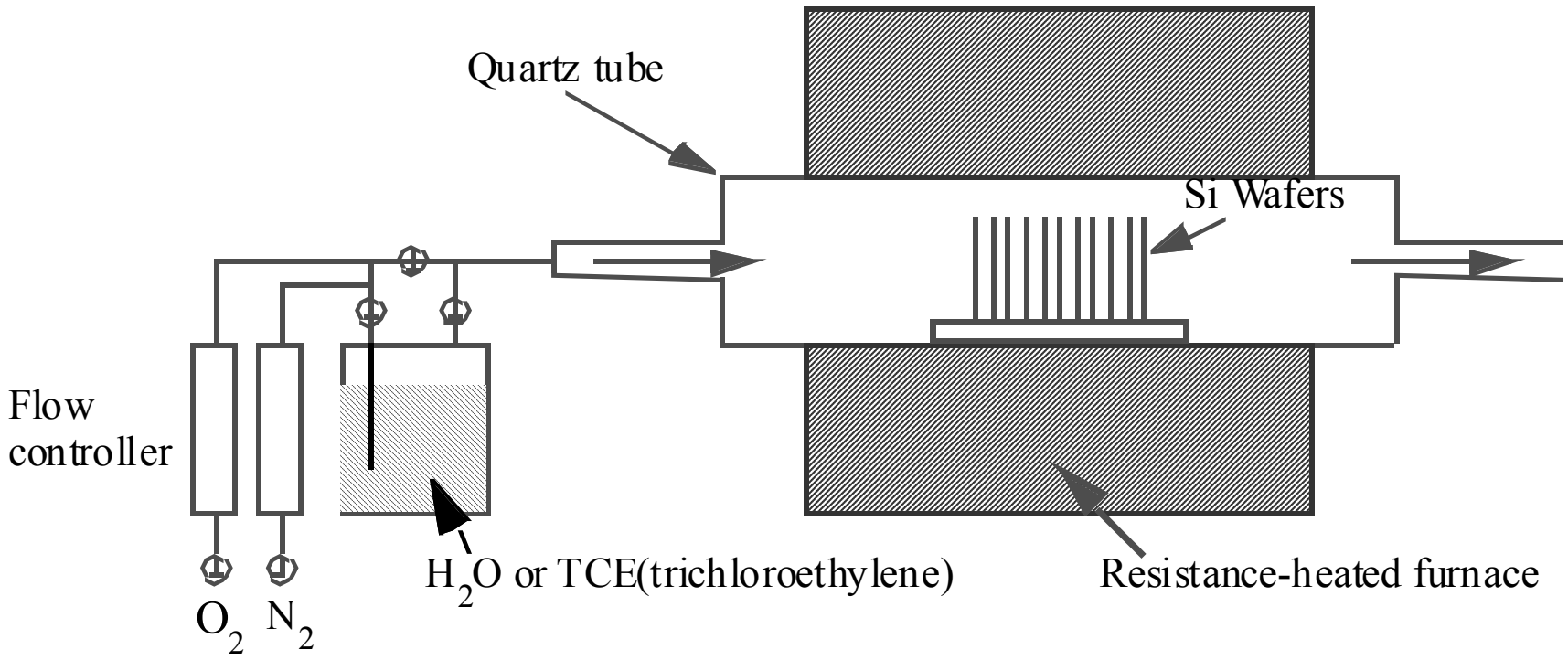
3.2 Oxidation of Silicon

Dry Oxidation : $Si + O_2 \rightarrow SiO_2$

Wet Oxidation : $Si + 2H_2O \rightarrow SiO_2 + 2H_2$



3.2 Oxidation of Silicon



3.2 Oxidation of Silicon

EXAMPLE : Sequential Oxidation

(a) How long does it take to grow 0.1μm of dry oxide at 1000 °C ?

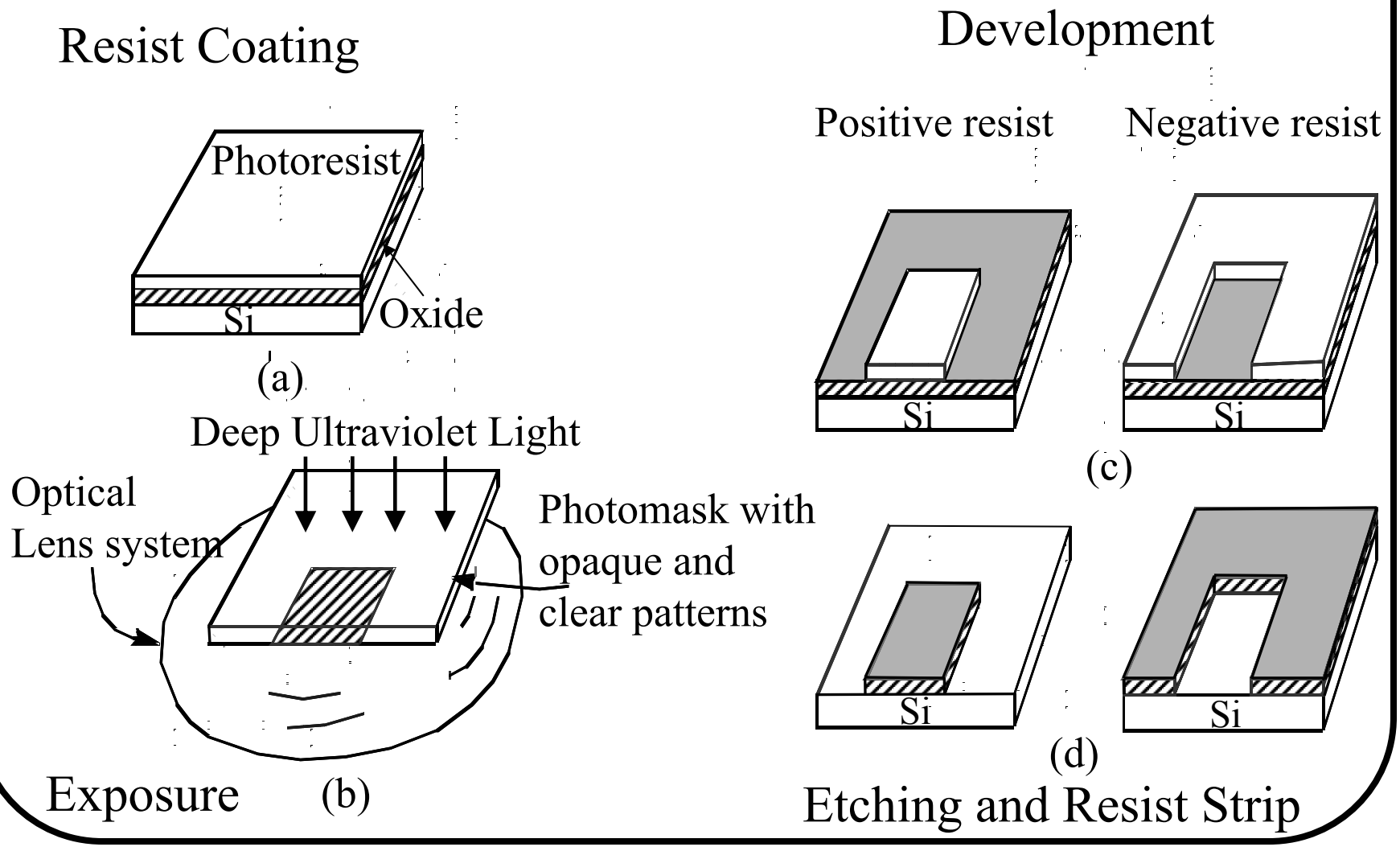
(b) After step (a), how long will it take to grow an additional 0.2μm of oxide at 900 °C in a wet ambient ?

Solution:

(a) From the "1000°C dry" curve in Slide 3-3, it takes 2.5 hr to grow 0.1μm of oxide.

(b) Use the "900°C wet" curve only. It would have taken 0.7hr to grow the 0.1 μm oxide and 2.4hr to grow 0.3 μm oxide from bare silicon. The answer is 2.4hr–0.7hr = 1.7hr.

3.3 Lithography



3.3 Lithography

Wafers are being loaded into a stepper in a clean room.

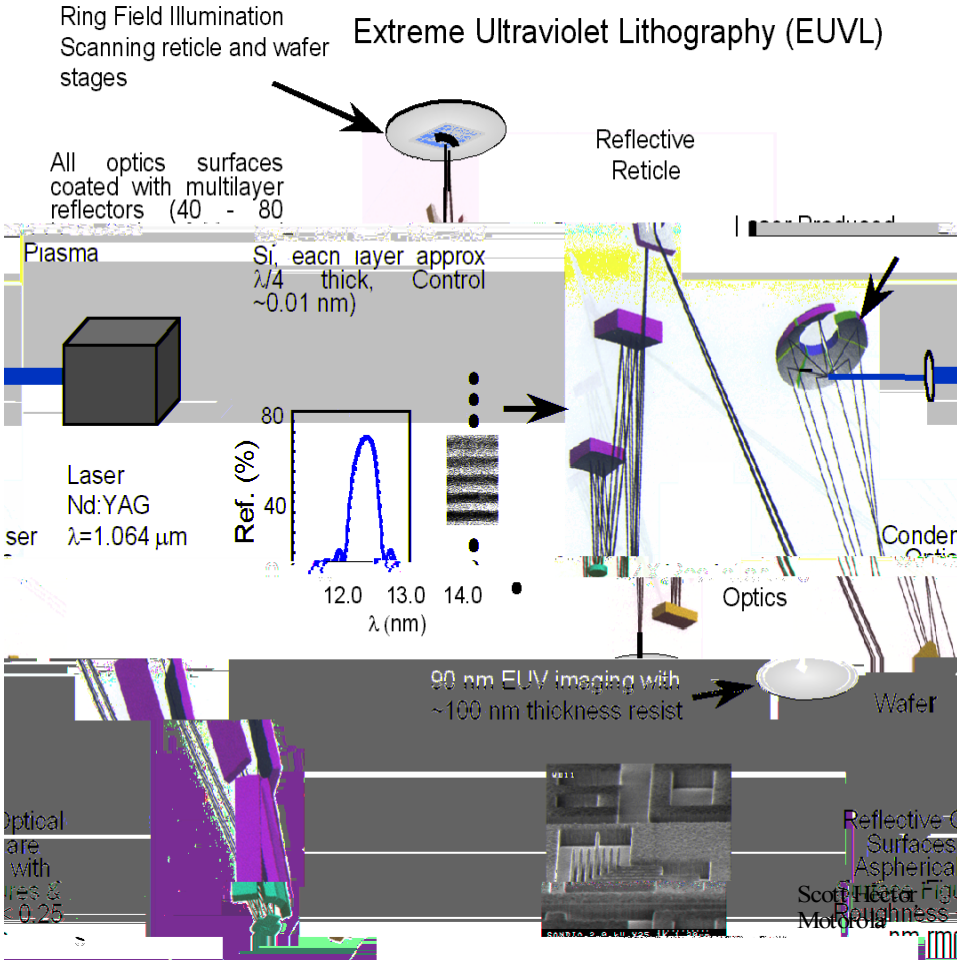
3.3 Lithography

Advanced Lithography Technology

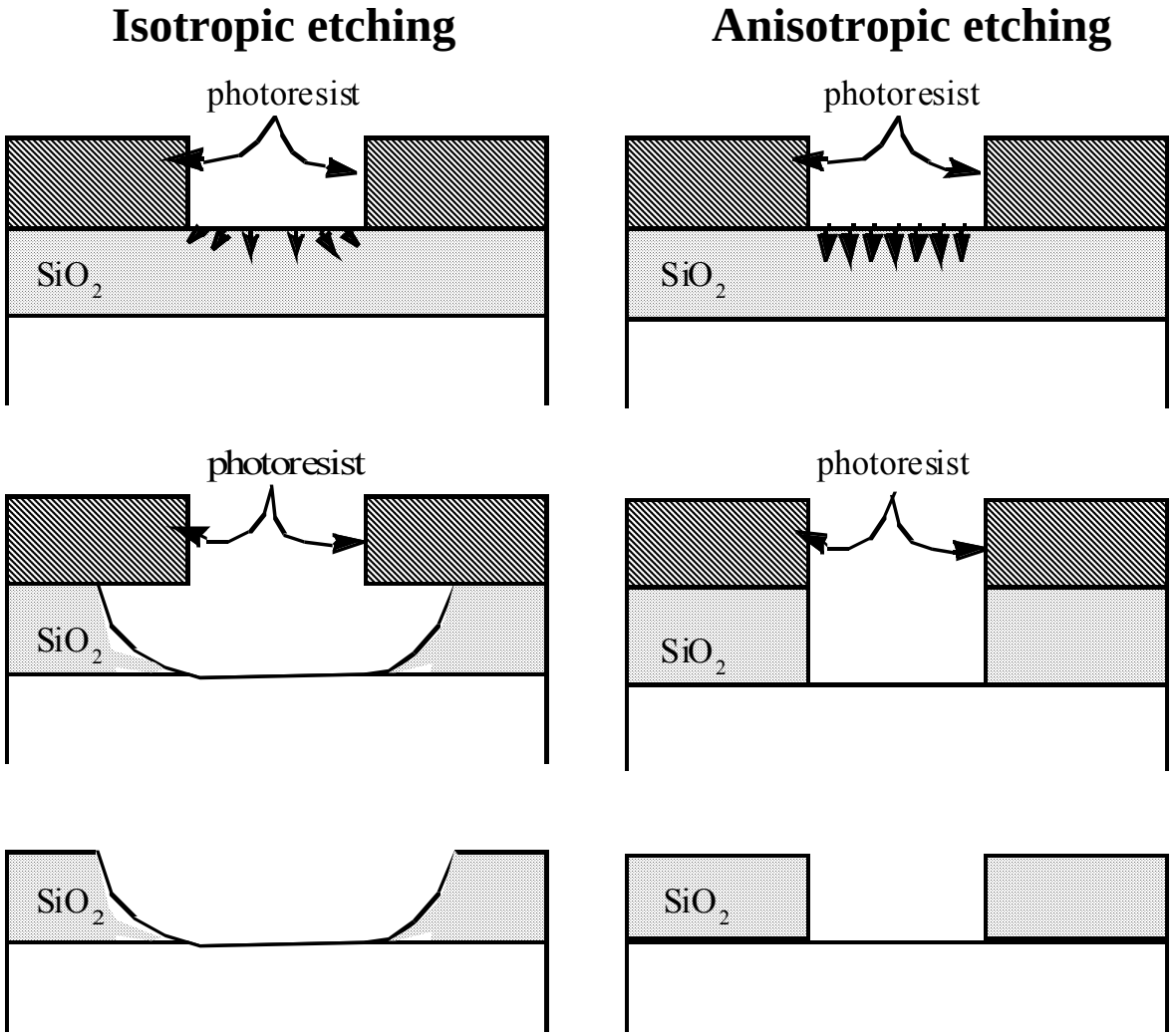
- ***Electron Projection Lithography*** : Exposes a complex pattern using mask and electron lens as is done in optical lithography.

- ***Extreme UV Lithography*** : Uses 13 nm wavelength (used to be called soft x-ray lithography).

Extreme UV Lithography

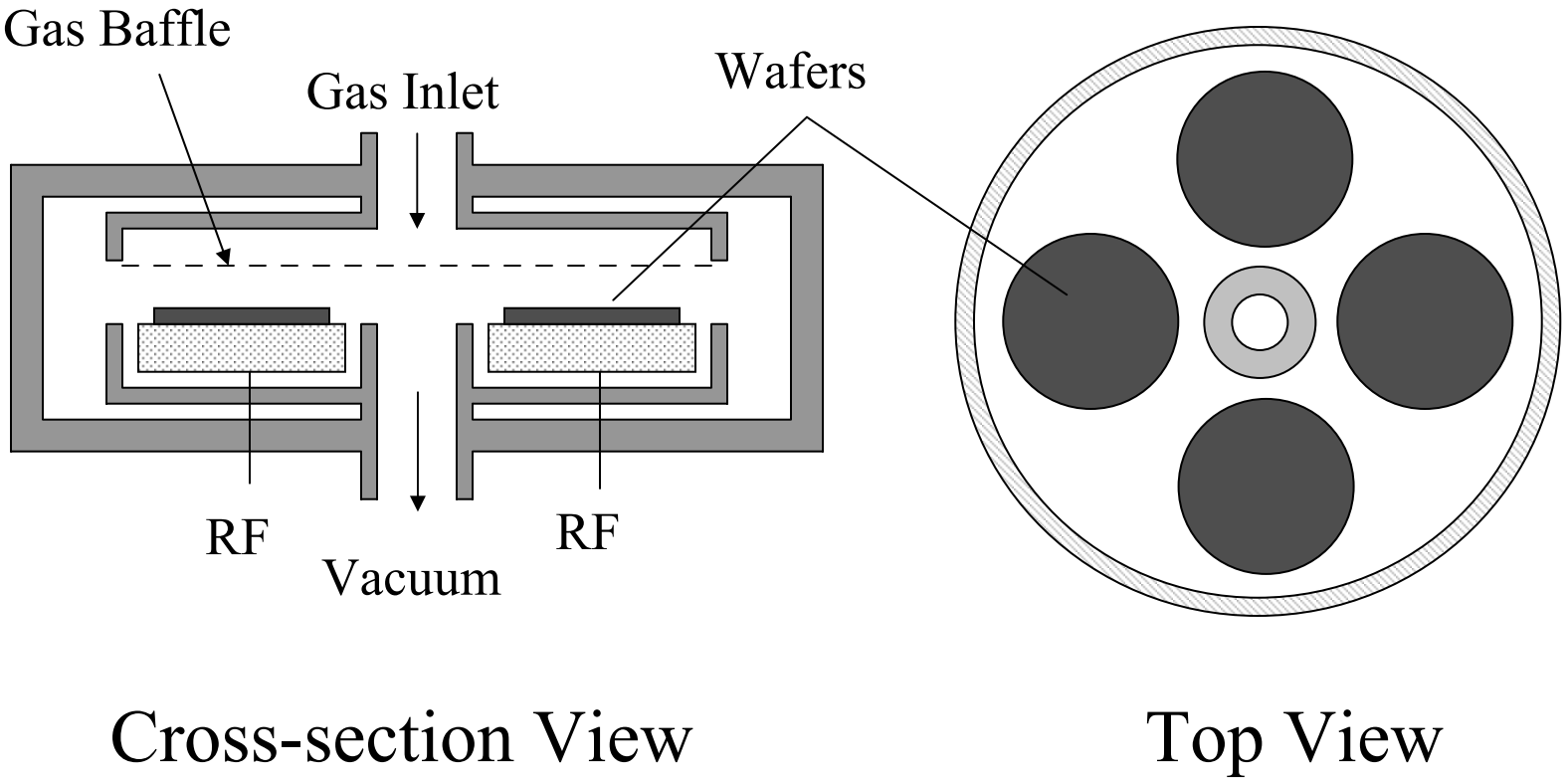


3.4 Pattern Transfer–Etching

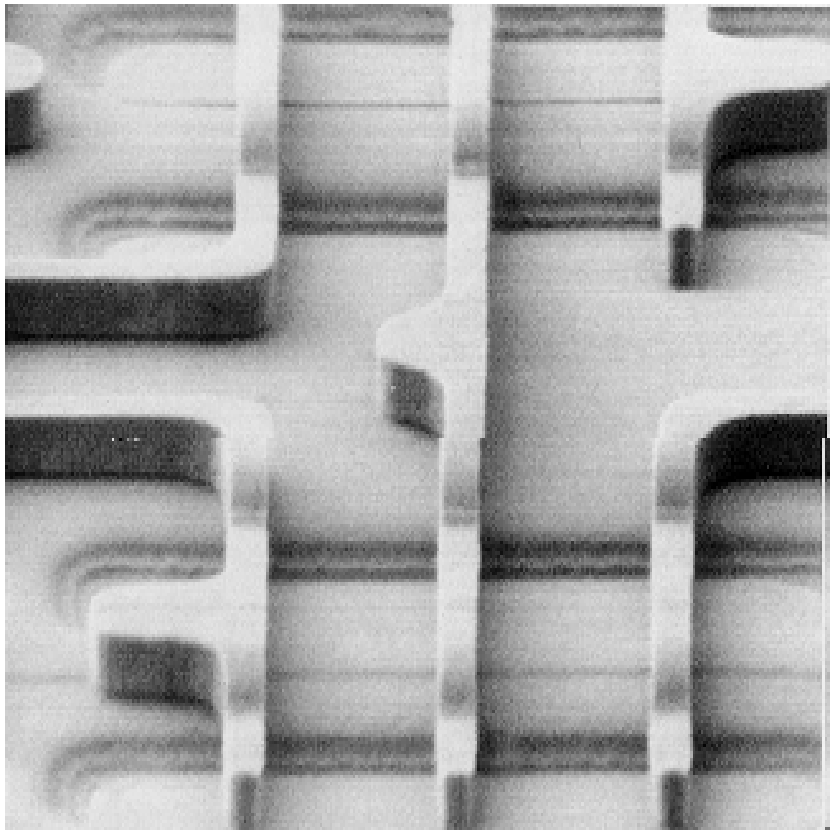


3.4 Pattern Transfer–Etching

Reactive-Ion Etching Systems



Scanning electron microscope view of a plasma-etched 0.16 μm pattern in polycrystalline silicon film.



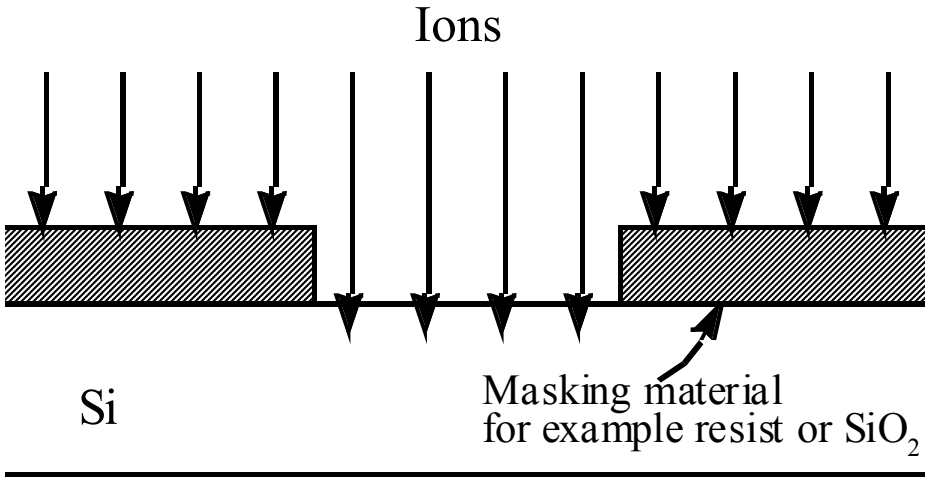
3.4 Pattern Transfer–Etching

Dry Etching (also known as Plasma Etching, or Reactive-Ion Etching) is anisotropic.

- Silicon and its compounds can be etched by plasmas containing F.
- Aluminum can be etched by Cl.
- Some concerns :
  - Selectivity and End-Point Detection
  - Plasma Process-Induced Damage or Wafer Charging Damage and Antenna Effect

3.5 Doping

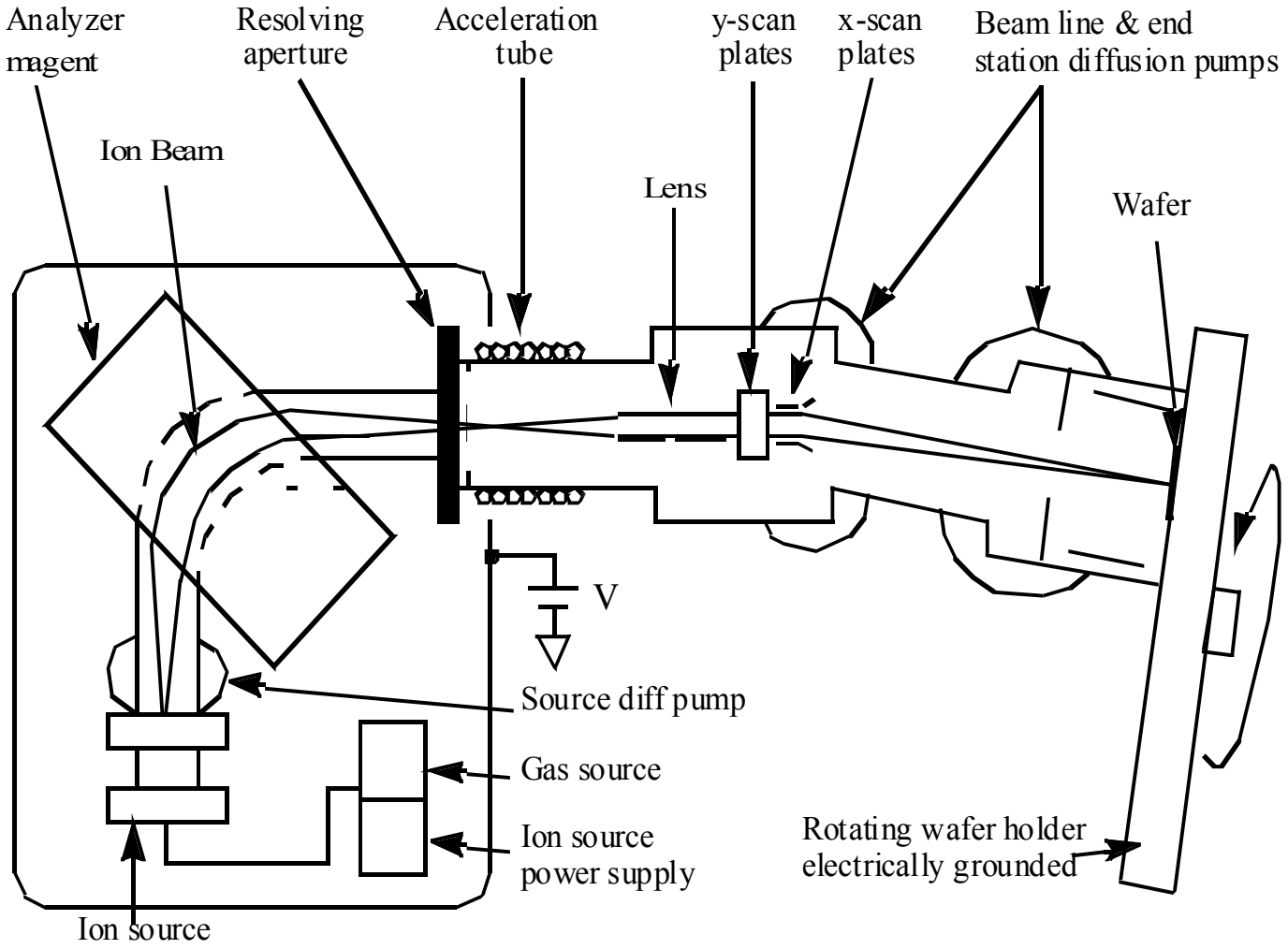
3.5.1 Ion Implantation



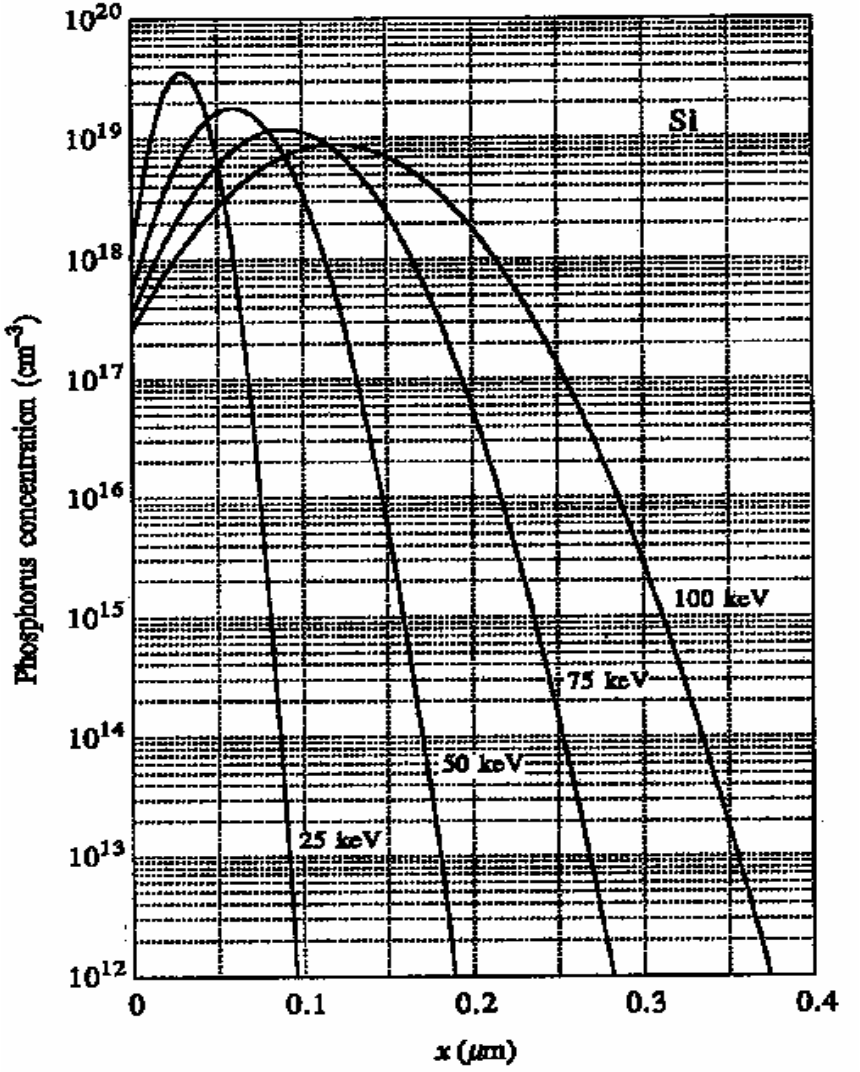
- The dominant doping method
- Excellent control of **dose** (cm^{-2})
- Good control of implant depth with energy (KeV to MeV)
- Repairing crystal damage and dopant activation requires annealing, which can cause dopant diffusion and loss of depth control.

3.5.1 Ion Implantation

Schematic of an Ion Implanter



3.5.1 Ion implantation



Phosphorous Density Profile after Implantation

3.5.1 Ion Implantation

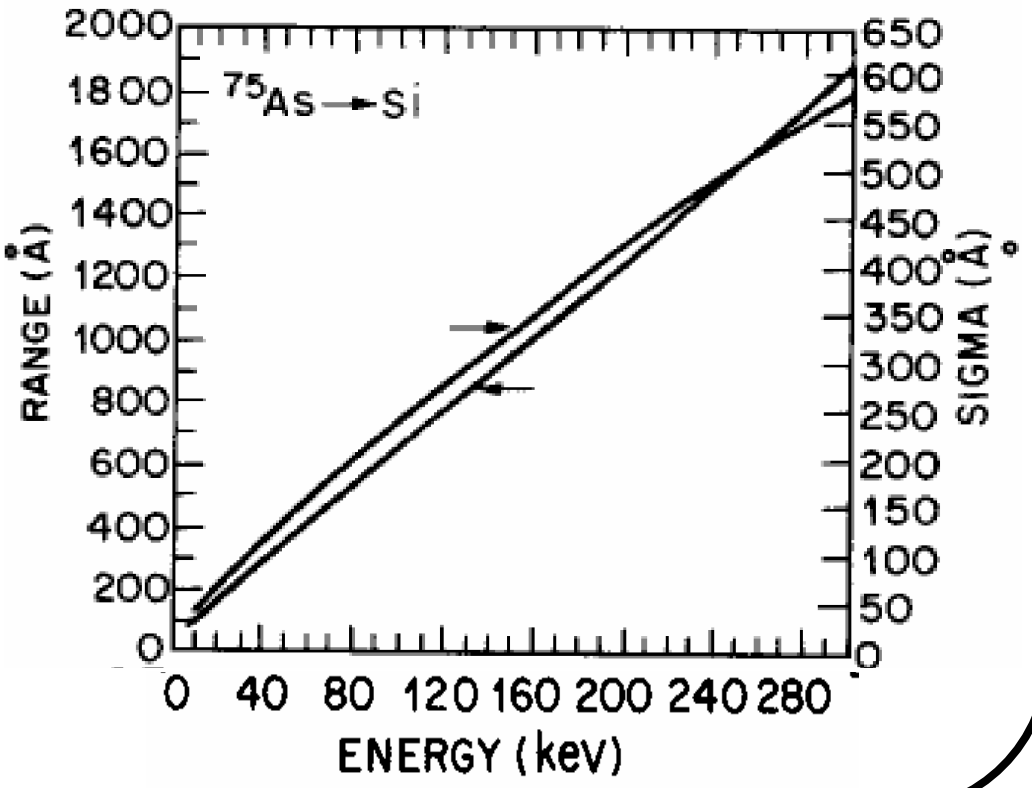
Model of Implantation Doping Profile (Gaussian)

$$N(x) = \frac{N_i}{\sqrt{2\pi}\cdot(\Delta R)} \cdot e^{-(x-R)^2/2\Delta R^2}$$

N_i : dose (cm^{-2})

R : range or depth

ΔR : spread or sigma



3.5 Doping

Other Doping Methods

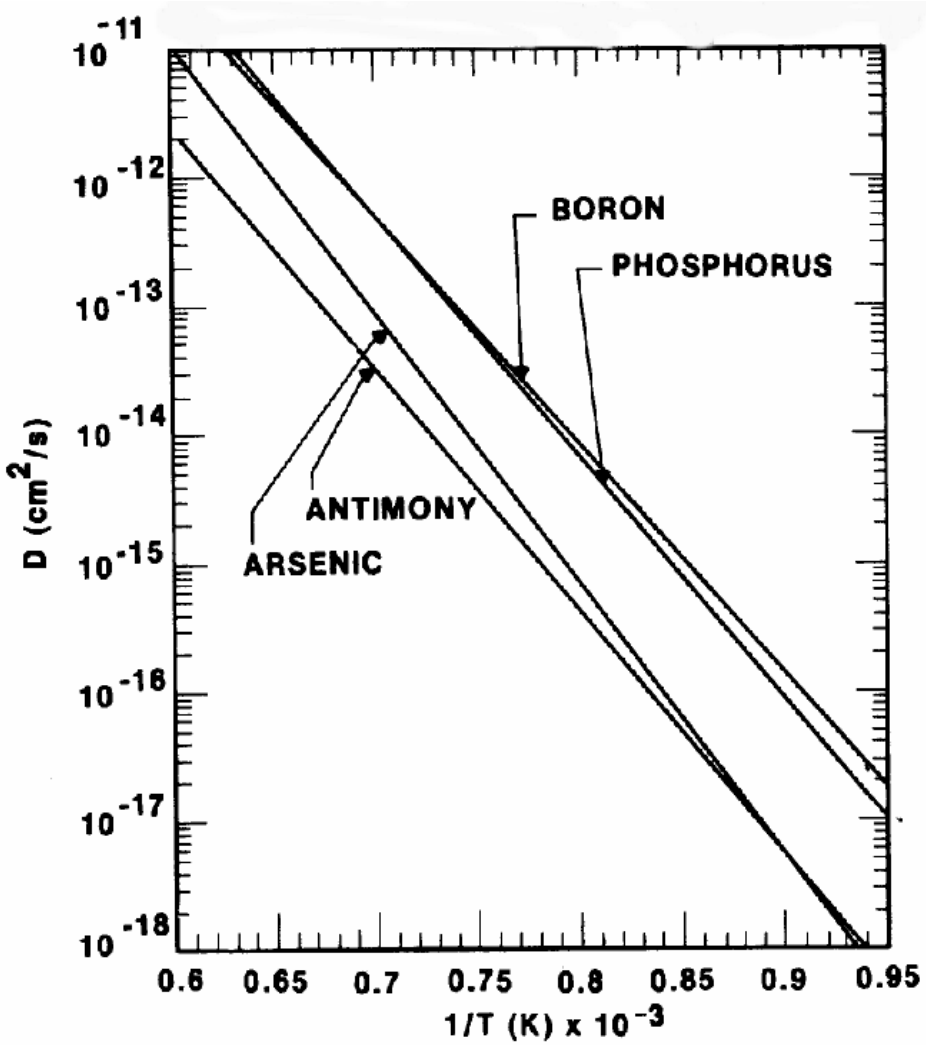
- ***Gas-Phase Doping*** : Used to dope Si with P using $POCl_3$.

- ***Solid-Source Doping*** : Dopant diffuses from a doped solid film (SiGe or oxide) into Si.

- ***In-Situ Doping*** : Used to dope deposited films during film deposition.

3.6 Dopant Diffusion

3.6 Dopant Diffusion



D increases with increasing temperature.

Some applications need very deep junctions (high *T*, long *t*). Others need very shallow junctions (low *T*, short *t*).

3.6 Dopant Diffusion

Shallow Junction and Rapid Thermal Annealing

• After ion implantation, thermal annealing is required. Furnace annealing causes too much diffusion of dopant for some applications.

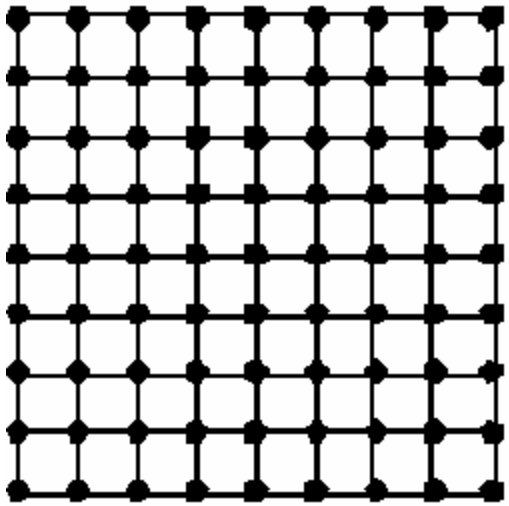
• In rapid thermal annealing (RTA), the wafer is heated to high temperature in seconds by a bank of heat lamps.

Also RTO (oxidation), RTCVD (chemical vapor deposition), RTP (processing).

3.7 Thin-Film Deposition

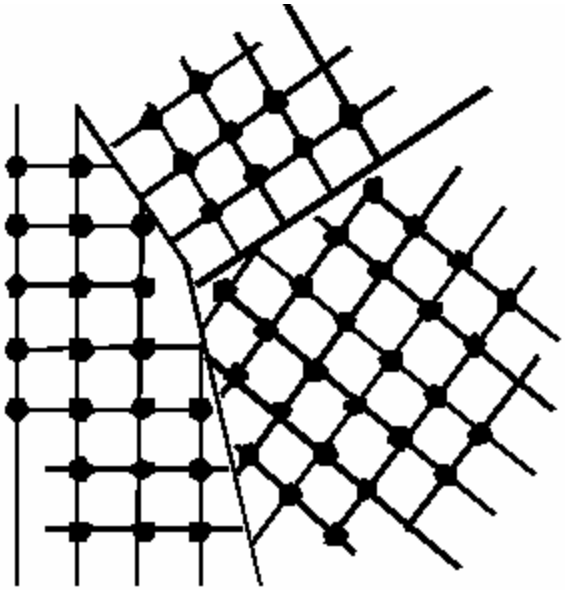
Three Kinds of Solid

Crystalline



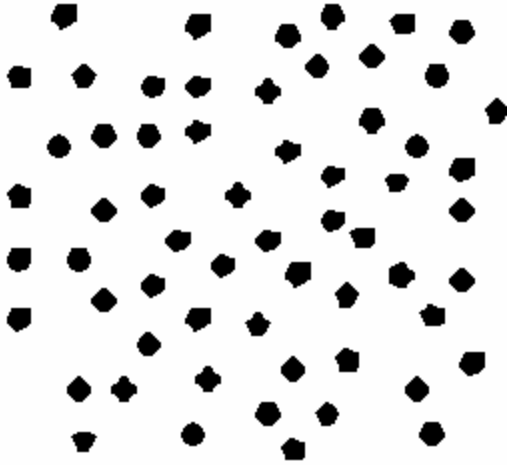
Silicon wafer

Polycrystalline



Thin film of Si or metal.

Amorphous



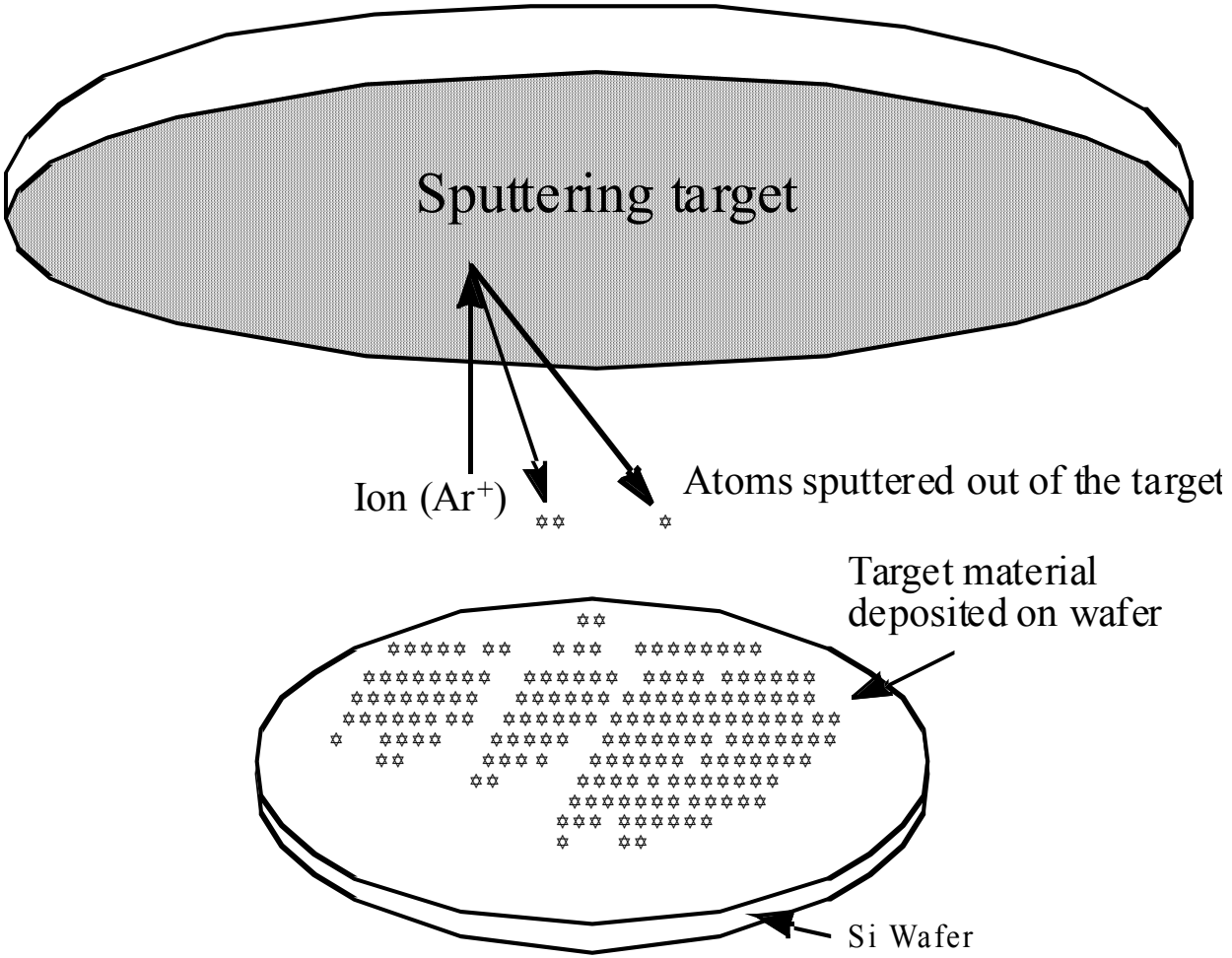
Thin film of SiO_2 or Si_3N_4.

3.7 Thin-Film Deposition

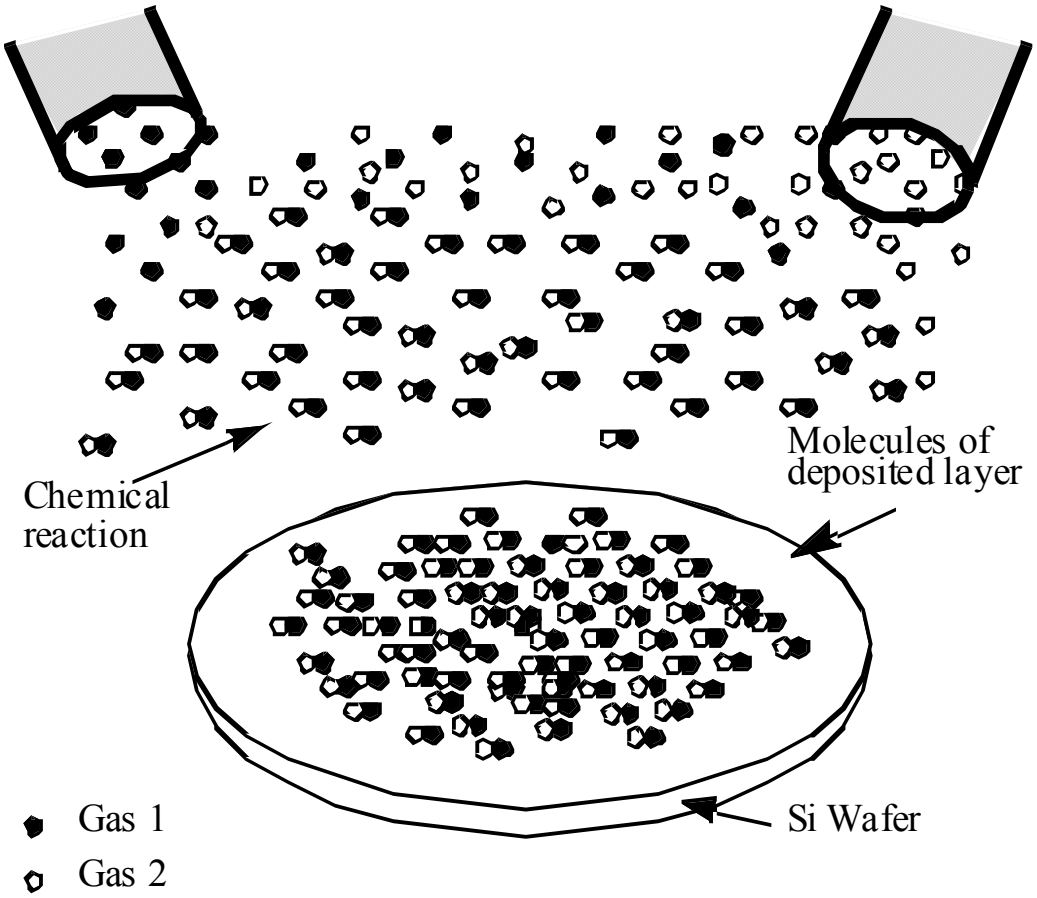
- Metal layers for device interconnect
- Inter-metal dielectric
- Poly-Si for transistor gate
- Barrier against interdiffusion
- Encapsulation

3.7.1 Sputtering

Schematic Illustration of Sputtering Process



3.7.2 Chemical Vapor Deposition (CVD)



Thin film is formed from gas phase components.

3.7.2 Chemical Vapor Deposition (CVD)

Two types of CVD equipment:

- **LPCVD (Low Pressure CVD)** : Good uniformity. Used for poly-Si, oxide, nitride.

- **PECVD (Plasma Enhanced CVD)** : Low temperature process and high deposition rate. Used for PE-oxide, PE-nitride, etc.

Chemical Reactions of LPCVD

Poly-Si : $SiH_4\ (g) \longrightarrow Si\ (s) + 2H_2\ (g)$

Nitride : $3SiH_2Cl_2\ (g)+4NH_3\ (g) \longrightarrow Si_3N_4\ (s)+6HCl(g)+6H_2\ (g)$

Oxide :

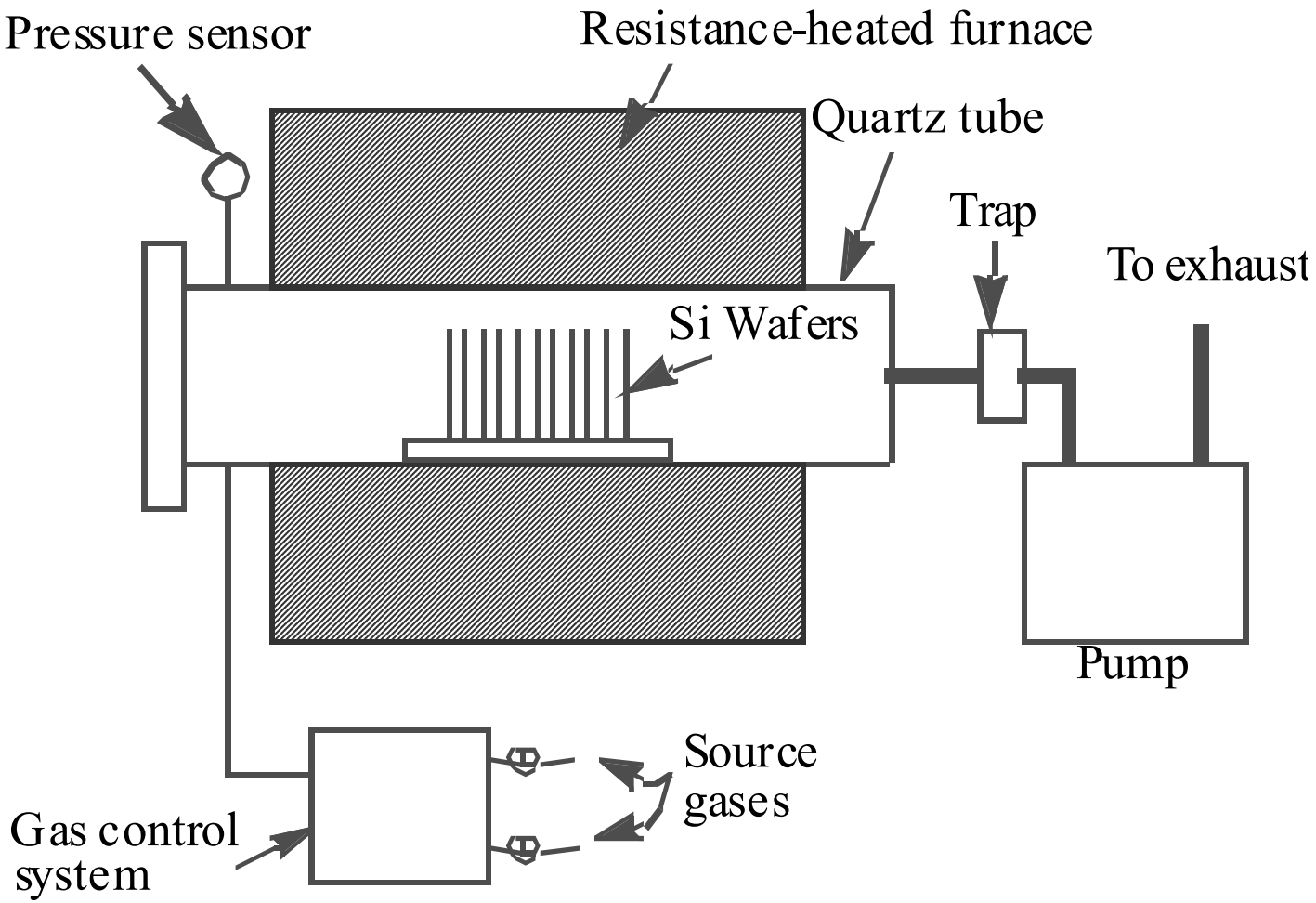
(1) LTO (Low Temperature Oxide)

$SiH_4\ (g) + O_2\ (g) \longrightarrow SiO_2\ (s) + 2H_2\ (g)$

(2) HTO (High Temperature Oxide)

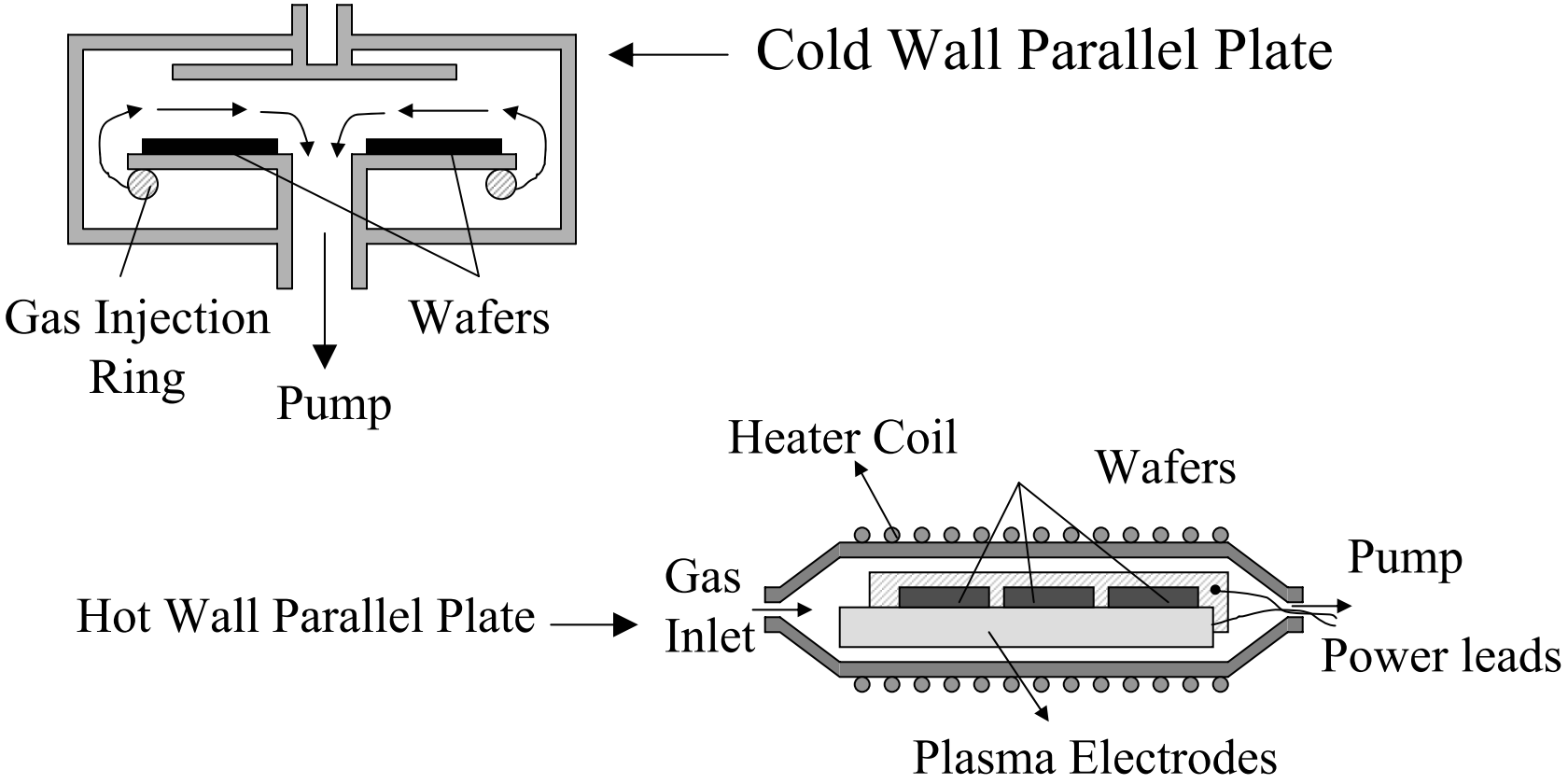
$SiH_2Cl_2\ (g)+2N_2O\ (g) \longrightarrow SiO_2\ (s)+2HCl\ (g)+2N_2\ (g)$

3.7.2 Chemical Vapor Deposition (CVD)



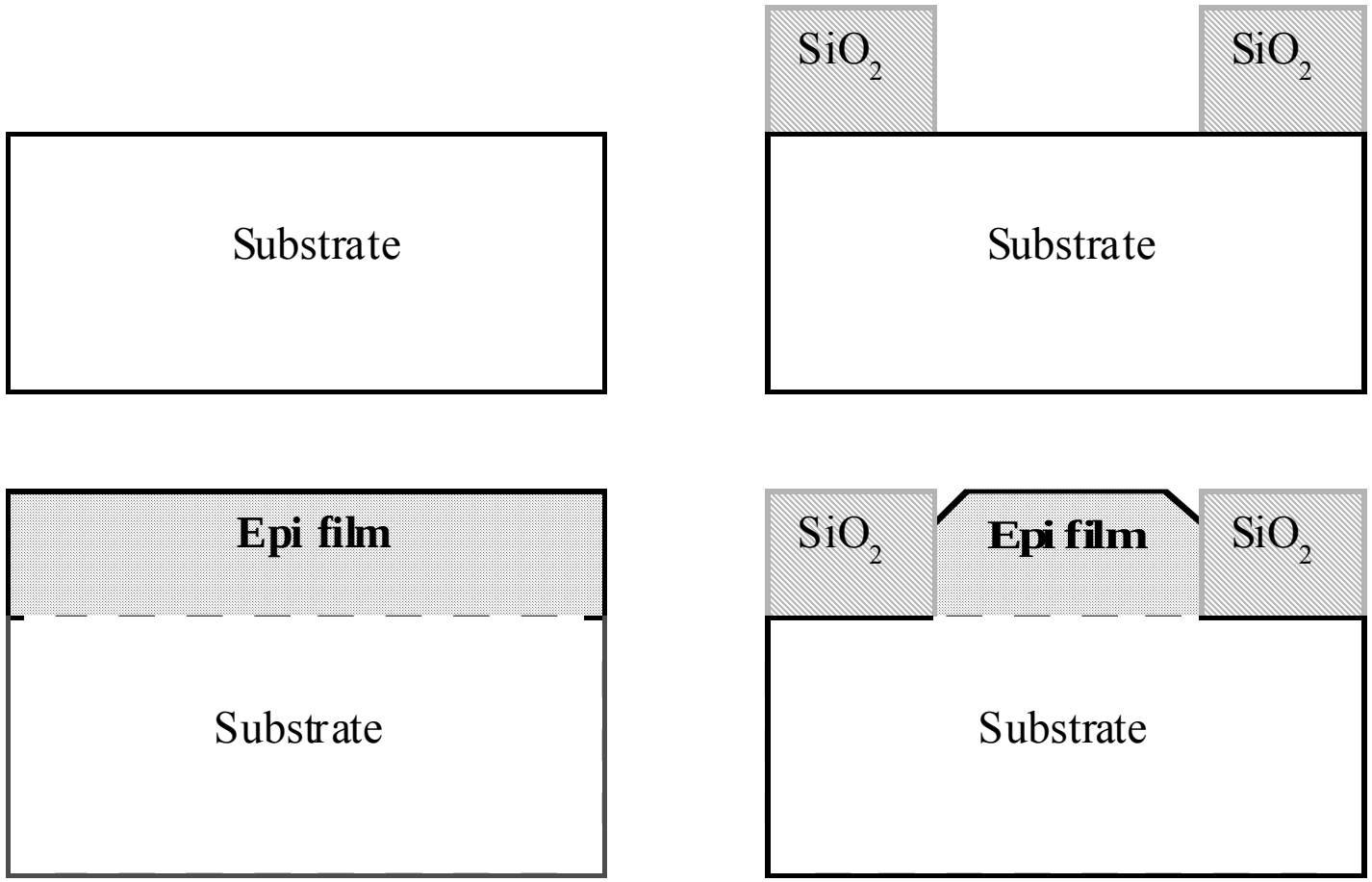
LPCVD Systems

3.7.2 Chemical Vapor Deposition (CVD)

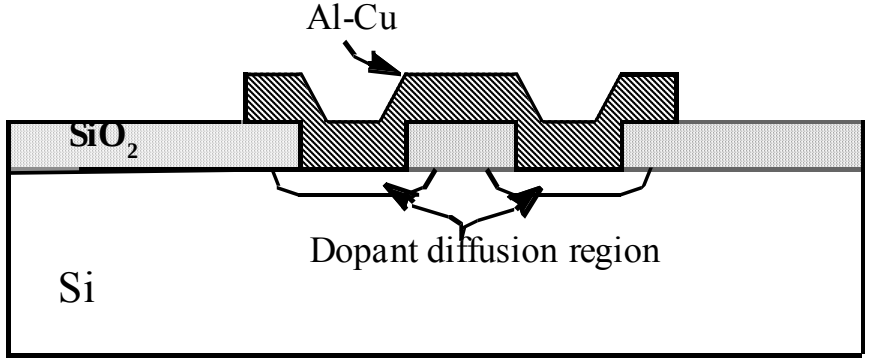


PECVD Systems

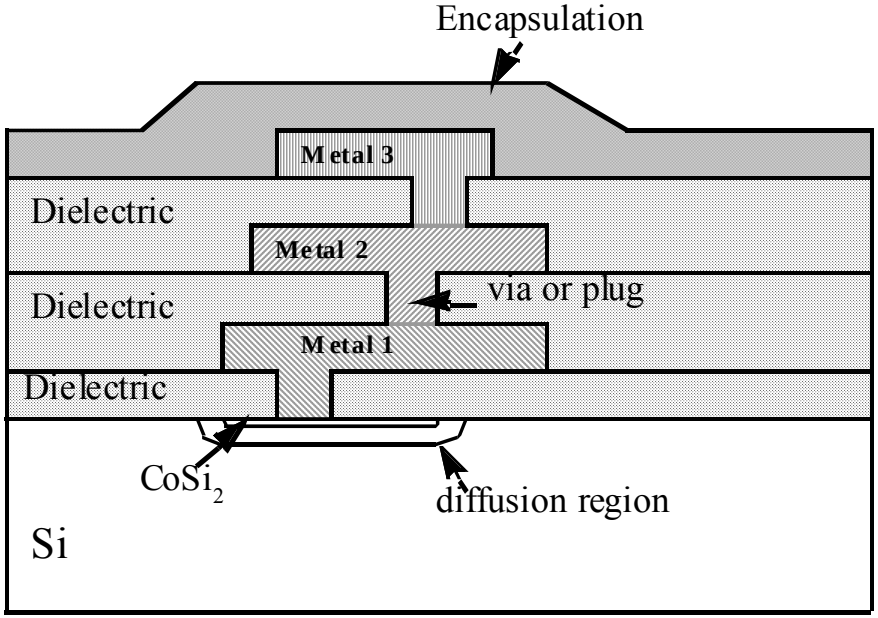
3.7.3 Epitaxy *(Deposition of Single-Crystalline Film)*



3.8 Interconnection–The Back-end Process



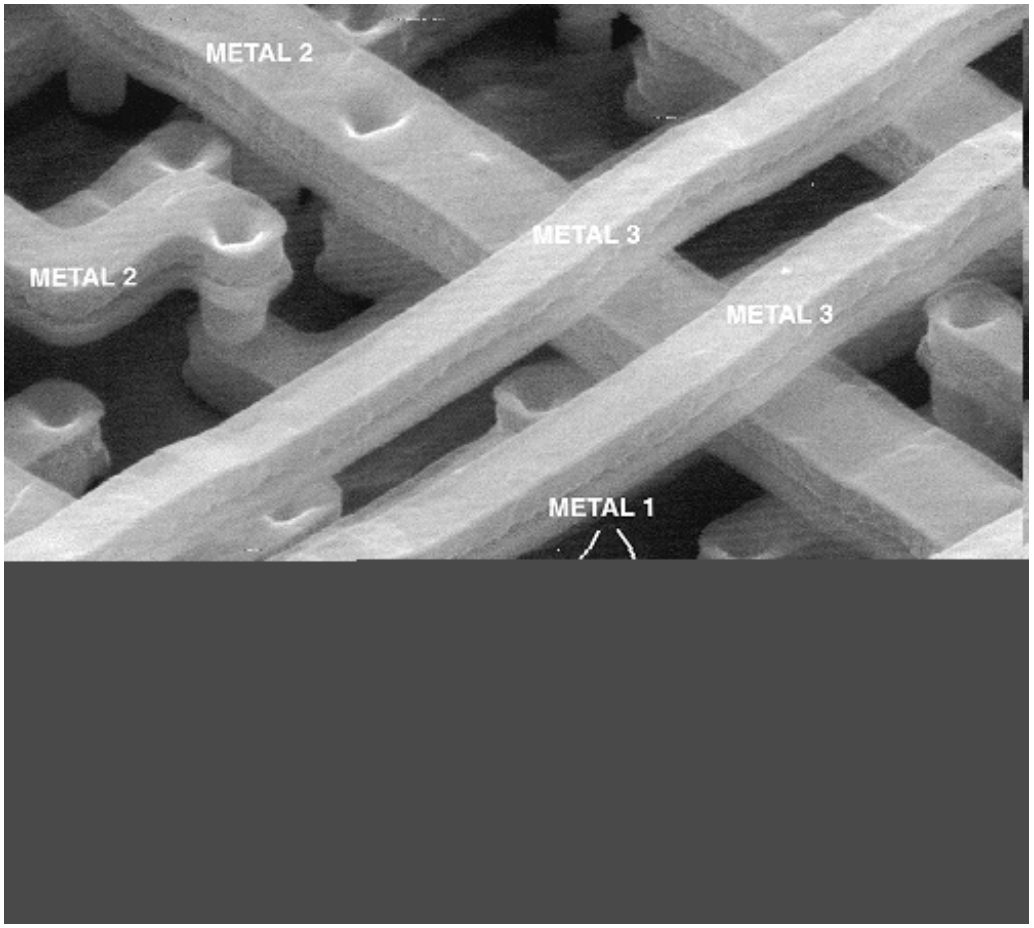
(a)



(b)

3.8 Interconnection–The Back-end Process

Multi-Level Metallization



Sun Microsystems Ultra Sparc Microprocessor

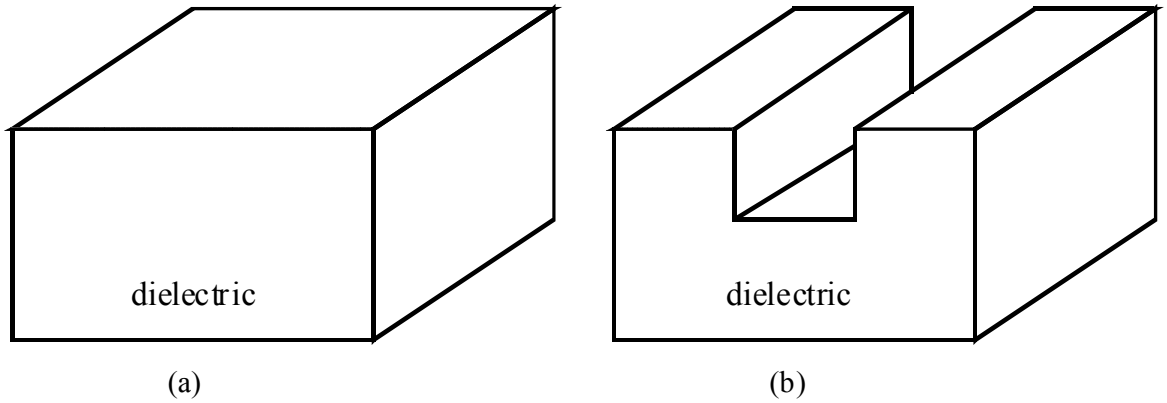
3.8 Interconnection–The Back-end Process

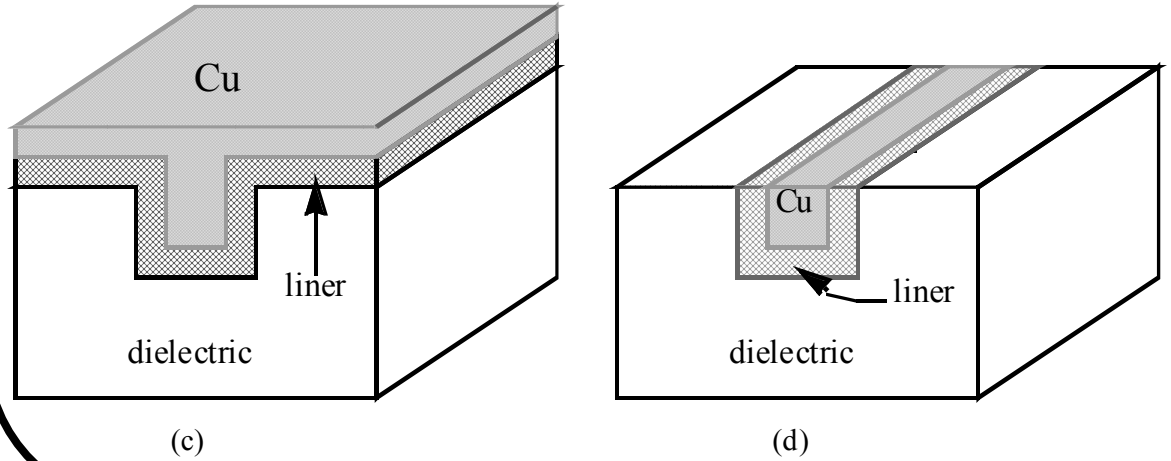
Copper Interconnect

- Al interconnect develops voids from electromigration.
- Cu has excellent electromigration reliability and 40% lower resistance than Al.
- Because dry etching of copper is difficult (copper compounds tend to be non-volatile), copper patterns may be defined by a ***damascene*** process.

3.8 Interconnection–The Back-end Process

Copper Damascene Process





Barrier liner prevents Cu diffusion.

Chemical-Mechanical Polishing (CMP) removes unwanted materials.

3.8 Interconnection–The Back-end Process

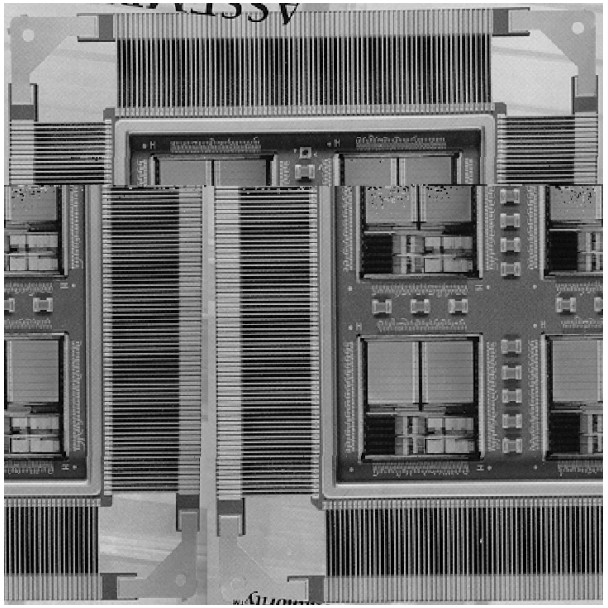
Planarization

- A flat surface is highly desirable for subsequent lithography and etching.

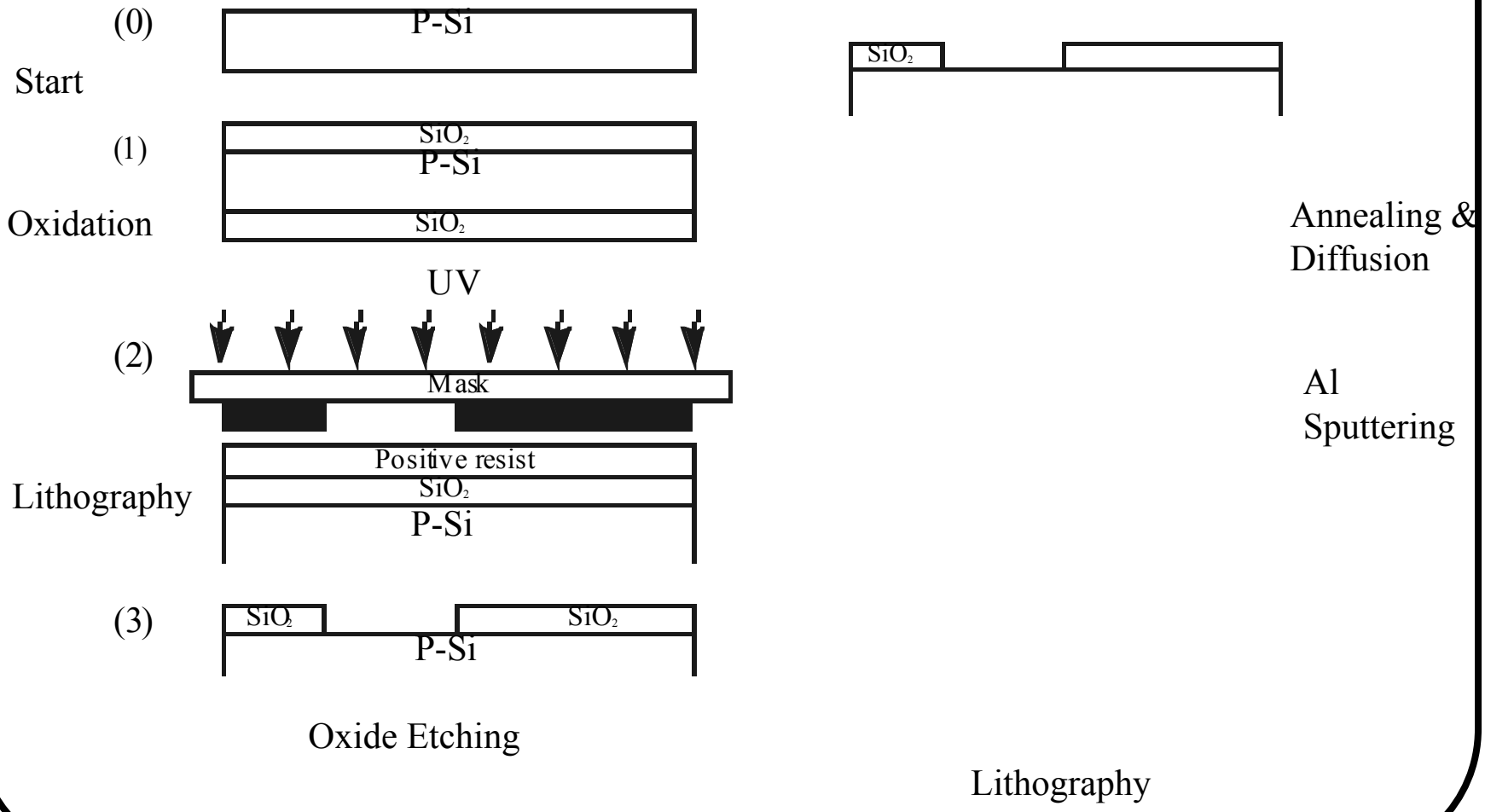
- CMP (Chemical-Mechanical Polishing) is used to planarize each layer of dielectric in the interconnect system.

3.9 Testing, Assembly, and Qualification

- Wafer acceptance test
- Die sorting
- Wafer sawing or cutting
- Packaging
- Flip-chip solder bump technology
- Multi-chip modules
- Burn-in
- Final test
- Qualification

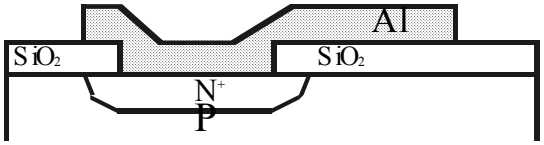


3.10 Chapter Summary–A Device Fabrication Example

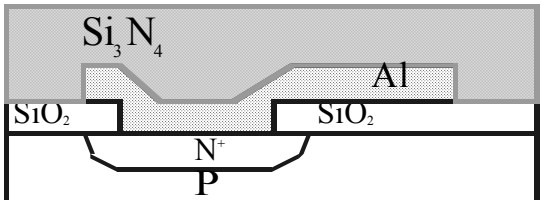


3.10 Chapter Summary–A Device Fabrication Example

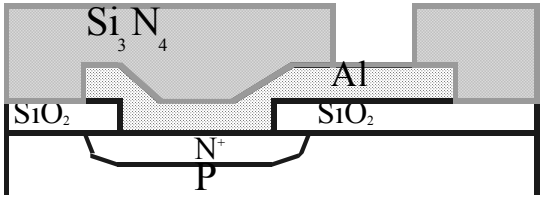
(8) Metal etching



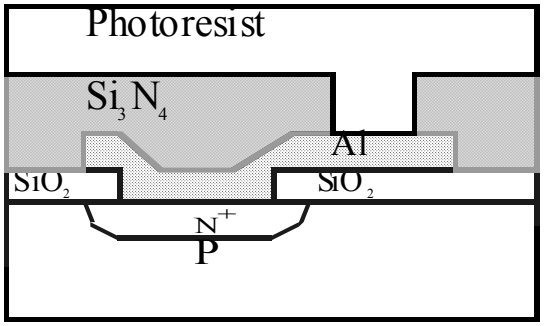
(9) CVD nitride deposition



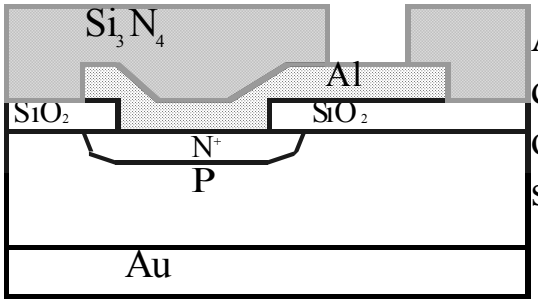
(10) Lithography and bonding window etching



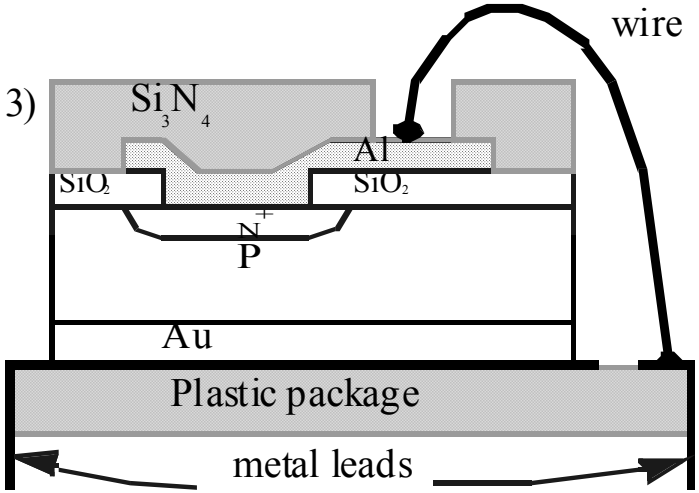
(11) Back Side milling



(12) Au deposition on the back side



(13)



Dicing, wire bonding, and packaging