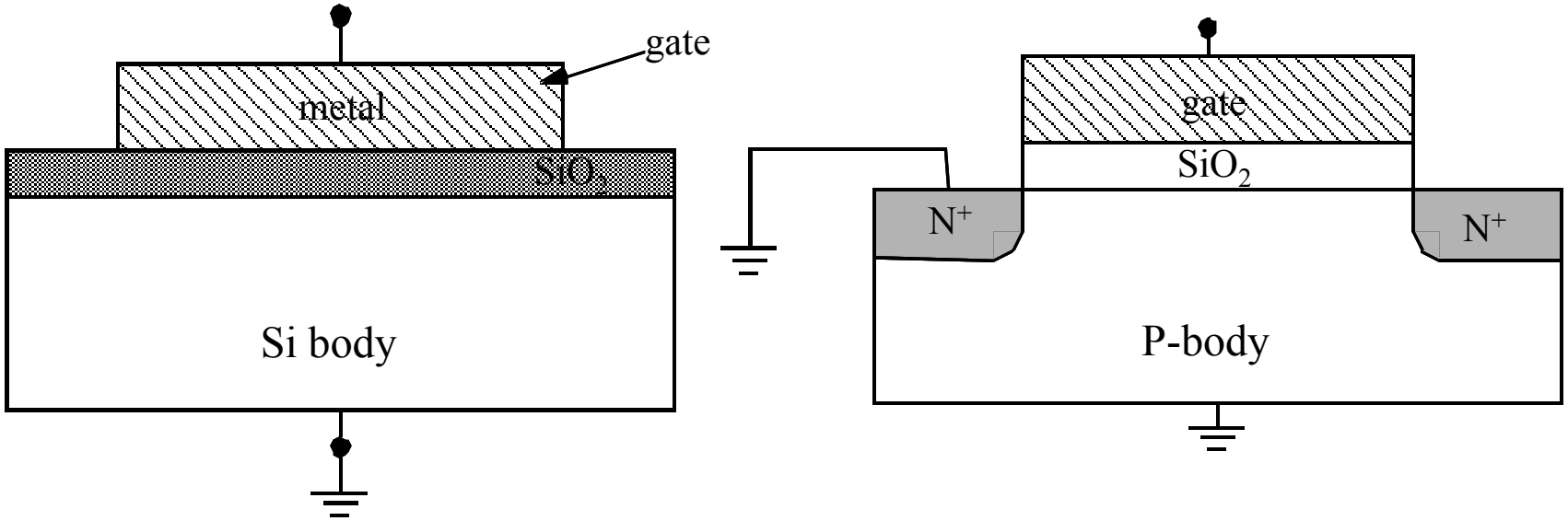
Chapter 5 MOS Capacitors

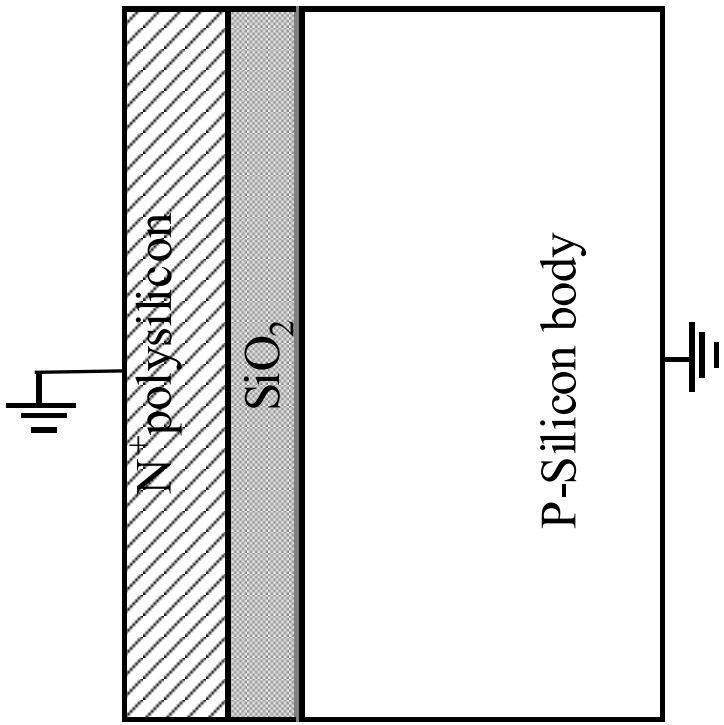
MOS: Metal-**O**xide-**S**emiconductor



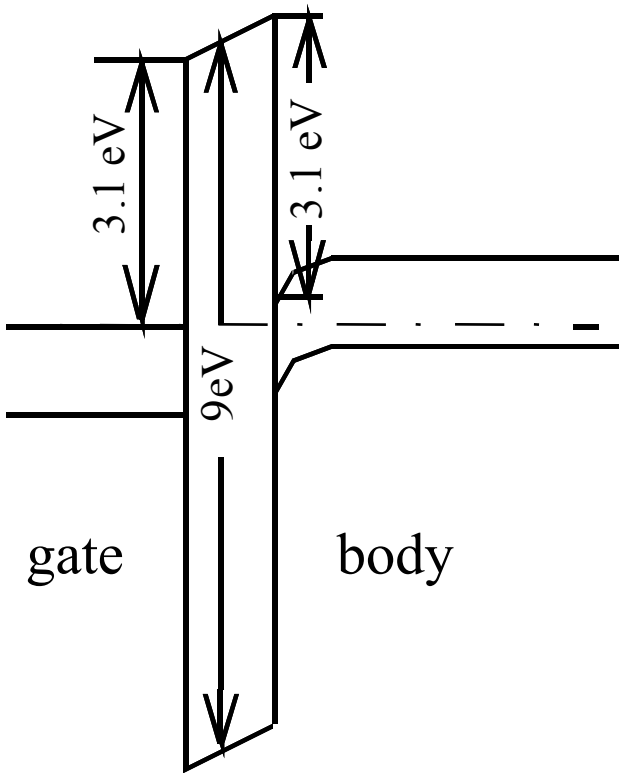
MOS capacitor

MOS transistor

Chapter 5 MOS Capacitors



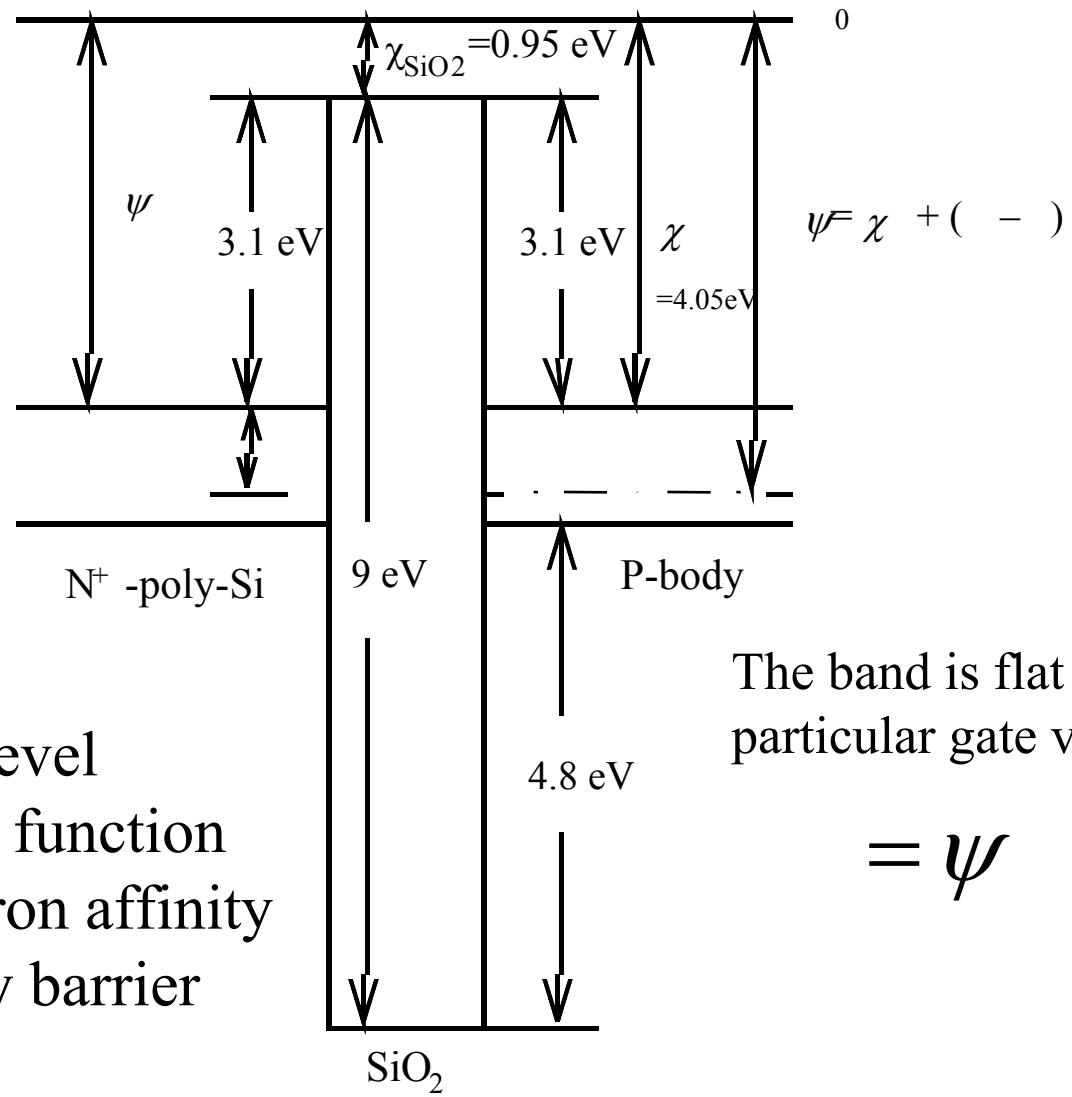
(a)



(b)

How does one arrive at this energy-band diagram for = 0?

5.1 Flat-band Condition and Flat-band Voltage



The band is flat at a particular gate voltage.

$$= \psi - \psi$$

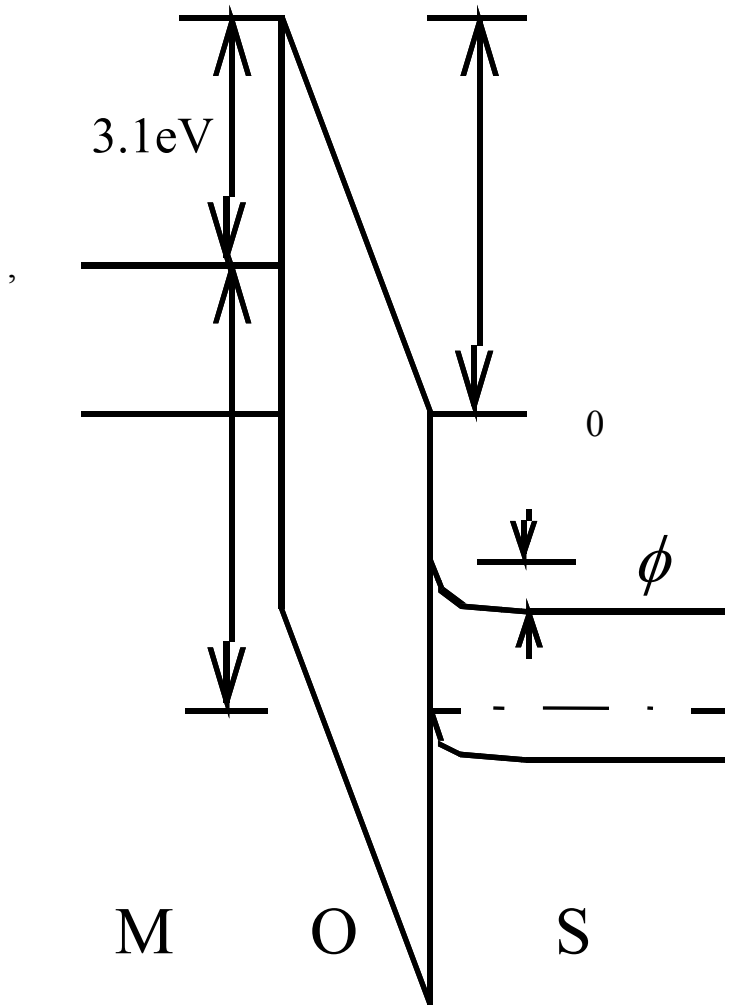
$_0$: Vacuum level

$_0 -$: Work function

$_0 -$: Electron affinity

Si/SiO_2 energy barrier

5.2 Surface Accumulation



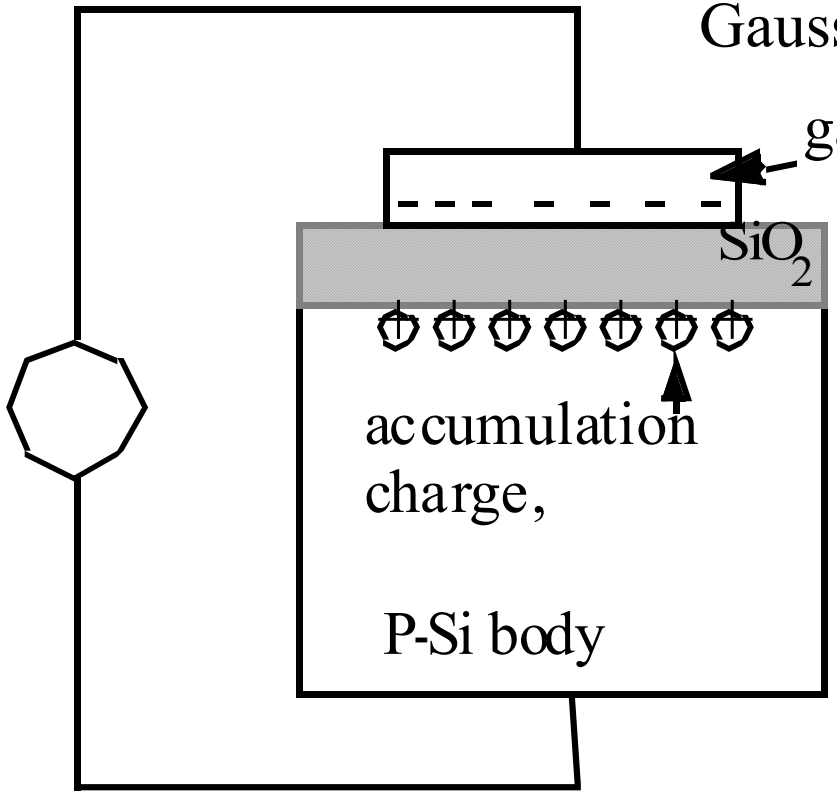
Make < .

$= \quad + \phi +$

ϕ : surface potential, band bending
: voltage across the oxide

ϕ is negligible when the surface is in accumulation because a little band-bending leads to a large accumulation charge.

5.2 Surface Accumulation



$$= \quad -$$

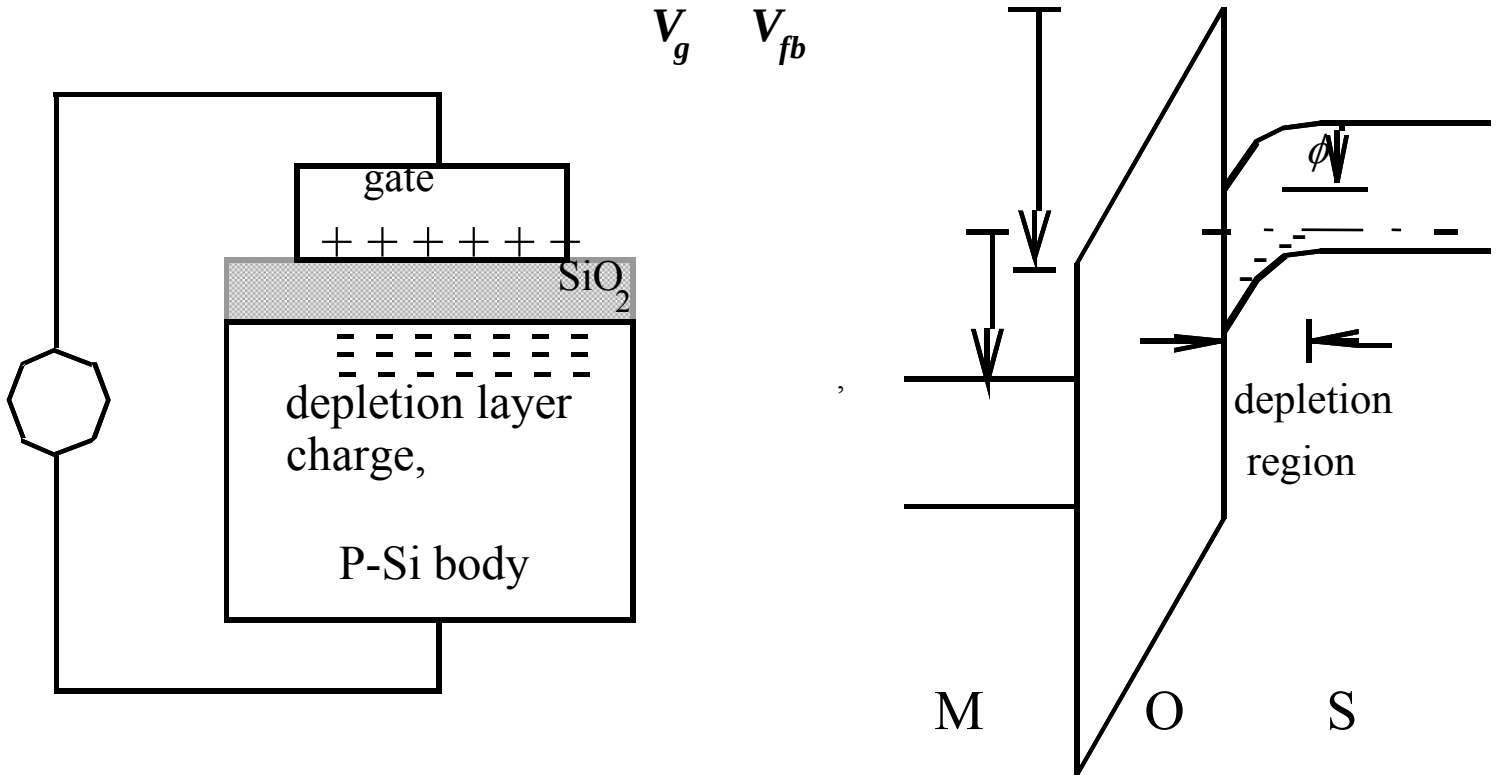
$$<$$

Gauss Law $\rightarrow$ $$= - \quad /$$

$$= - \quad (\quad - \quad)$$

$$= - \quad /$$

5.3 Surface Depletion



(a) (b)

$$= - \qquad = - \qquad = \qquad = \frac{\sqrt{2\varepsilon\phi}}{}$$

5.3 Surface Depletion

$$= \quad + \phi \; + \quad = \quad + \phi \; + \frac{\sqrt{\quad 2\varepsilon \; \phi}}{\quad}$$

Can this equation be solved to yield ϕ ?

5.4 Threshold Condition and Threshold Voltage

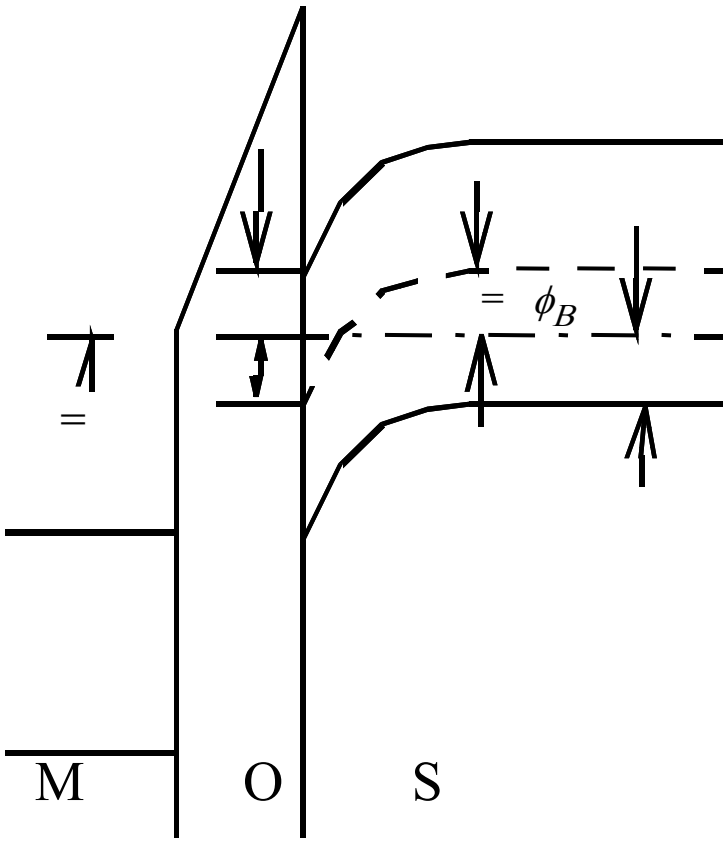
threshold (of inversion)

threshold **:** , or

( ) ( ) or

✧ and ,

$$\phi \quad = 2\phi \quad = 2 \frac{}{} \ln\left(\frac{}{}\right)$$



$$\phi \quad = \frac{}{2} - (\quad - \quad) \Big| \quad = \frac{}{} \ln\left(\frac{}{}\right) - \frac{}{} \ln\left(\frac{}{}\right) = \frac{}{} \ln\left(\frac{}{}\right)$$

Threshold Voltage

$$= \quad + \quad +$$

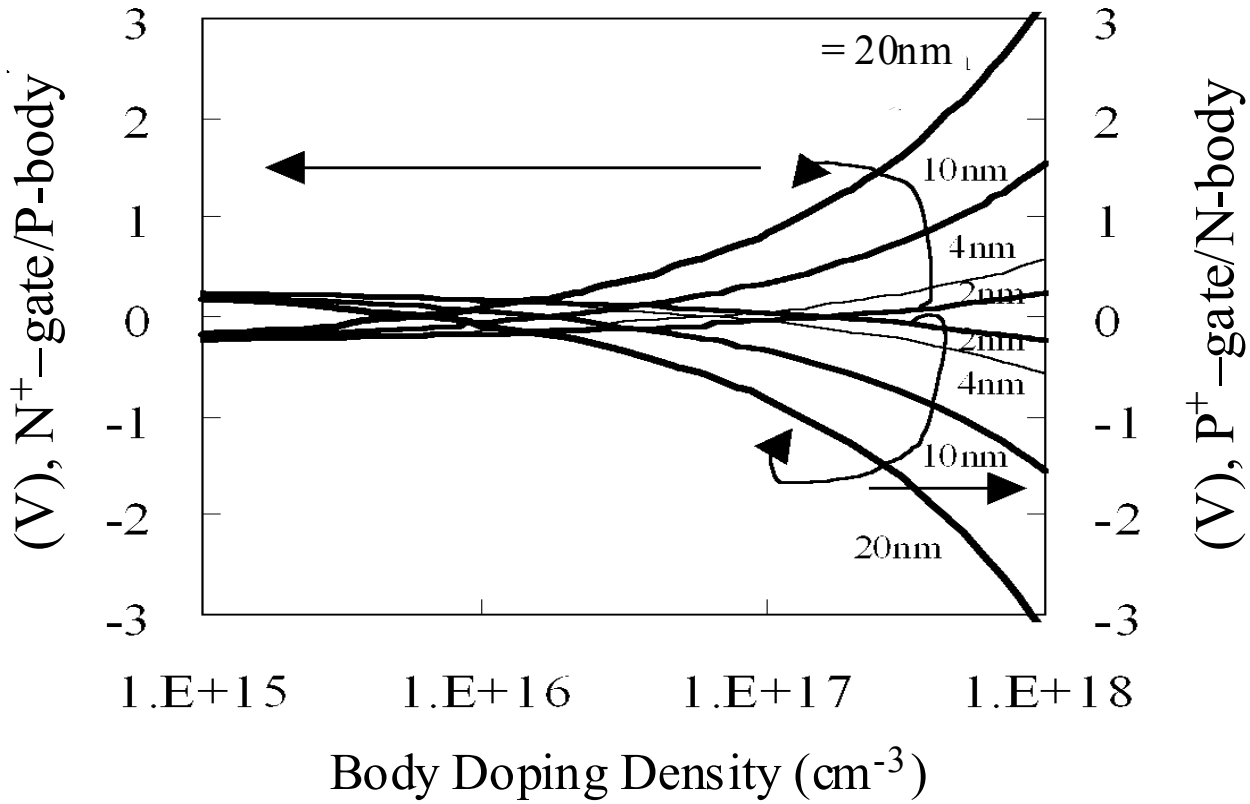
$$= \quad + 2\phi \quad + \frac{\sqrt{\quad 2\varepsilon \; 2\phi}}{}$$

Alternative definition of the threshold condition :

$$\phi \quad = \phi \quad + 0.45\,\mathrm{V} = \frac{}{} \ln \frac{}{} + 0.45\,\mathrm{V}$$

$$= \quad + \phi \quad + 0.45\,\mathrm{V} + \frac{\sqrt{2 \quad 2\varepsilon \; (\phi \quad + 0.45\,\mathrm{V})}}{}$$

Threshold Voltage



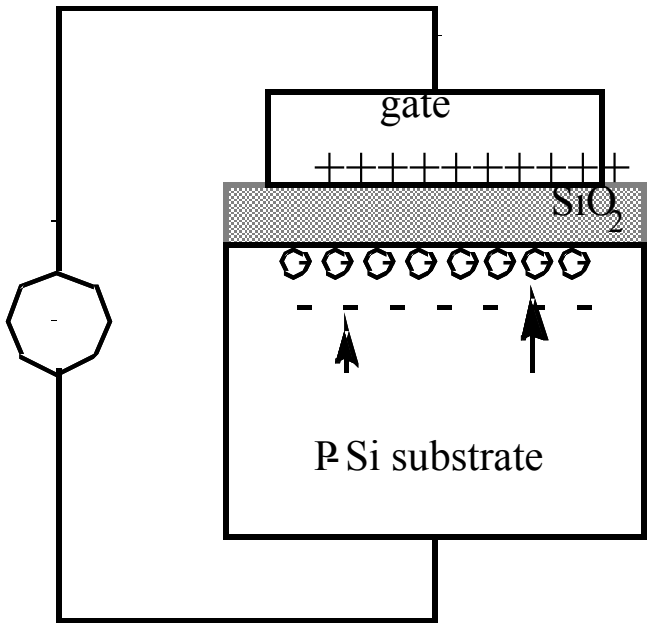
+ for P-body,
– for N-body:

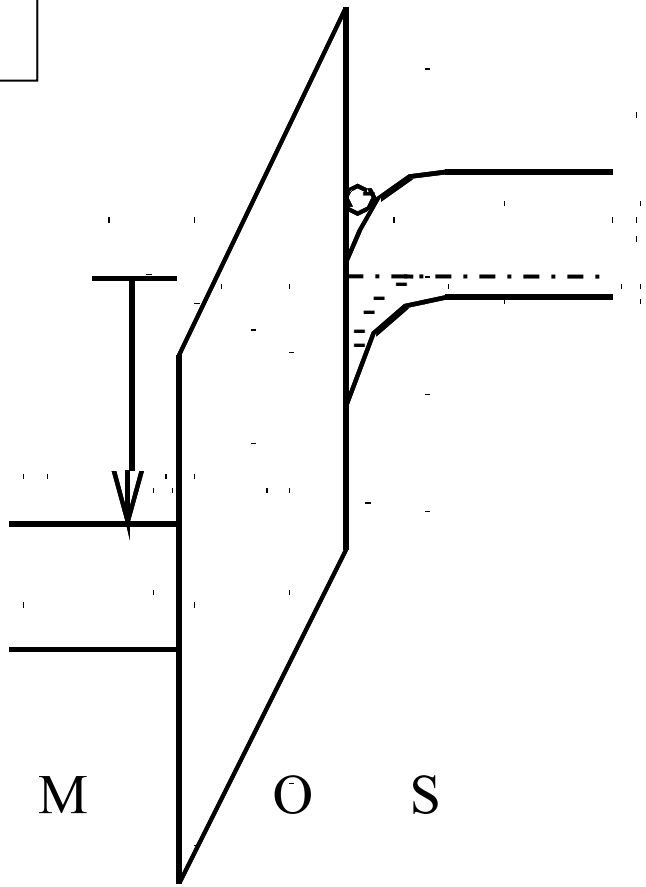
$$= \pm 2\phi \pm \frac{\sqrt{2\varepsilon\ 2\phi}}{}$$

5.5 Strong Inversion–Beyond Threshold

$$= \qquad = \sqrt{\frac{2\varepsilon\,\phi}{}}$$

$>$

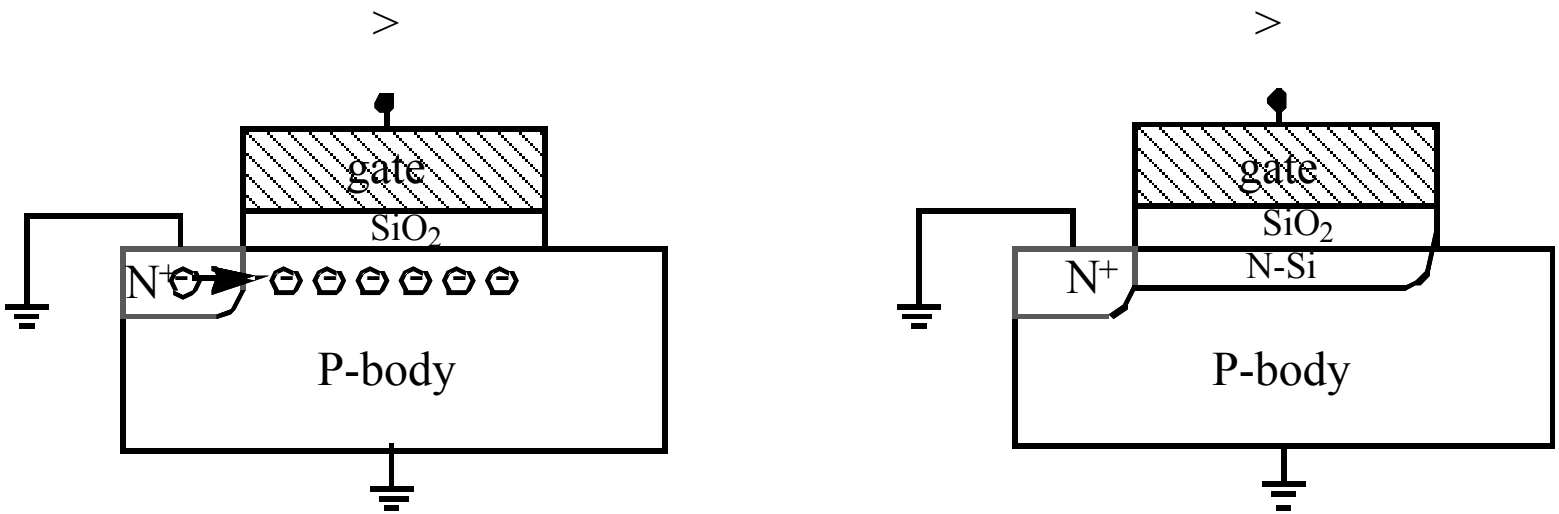




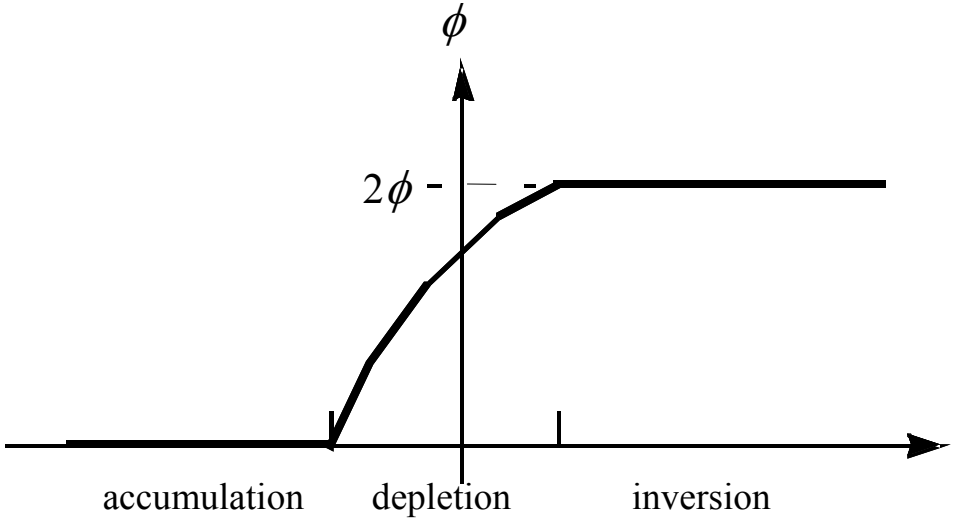
Inversion Layer Charge, Q_{inv} (C/cm^2)

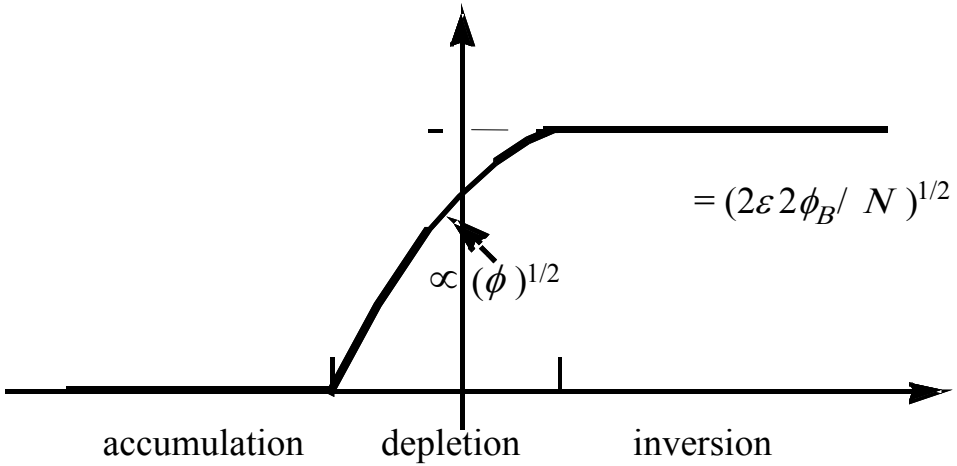
$$= \quad +\phi \quad - \text{——} - \text{——} = \quad +\phi \quad + \frac{\sqrt{\quad 2\varepsilon\ \phi}}{} - \text{——}$$

$$= \quad - \text{——} \qquad \therefore \quad \boxed{\quad = - \quad (\quad - \quad)}$$

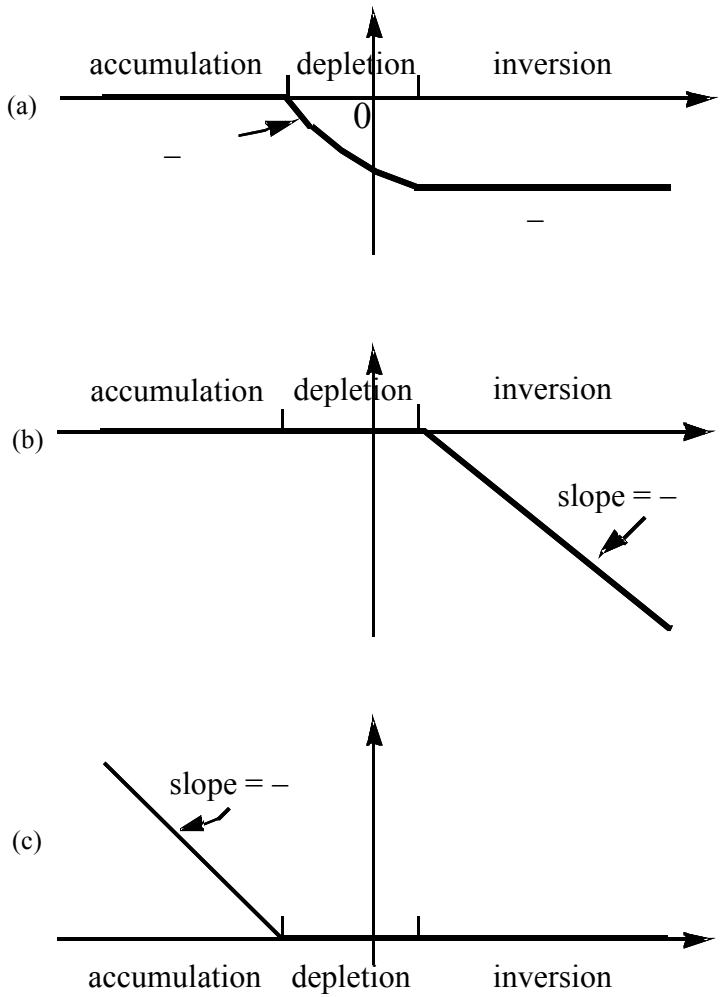


Review : Basic MOS Capacitor Theory



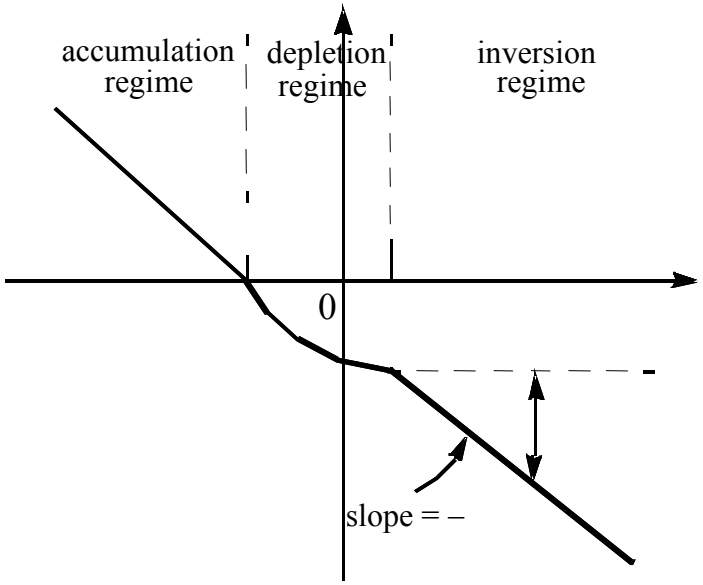


Review : Basic MOS Capacitor Theory

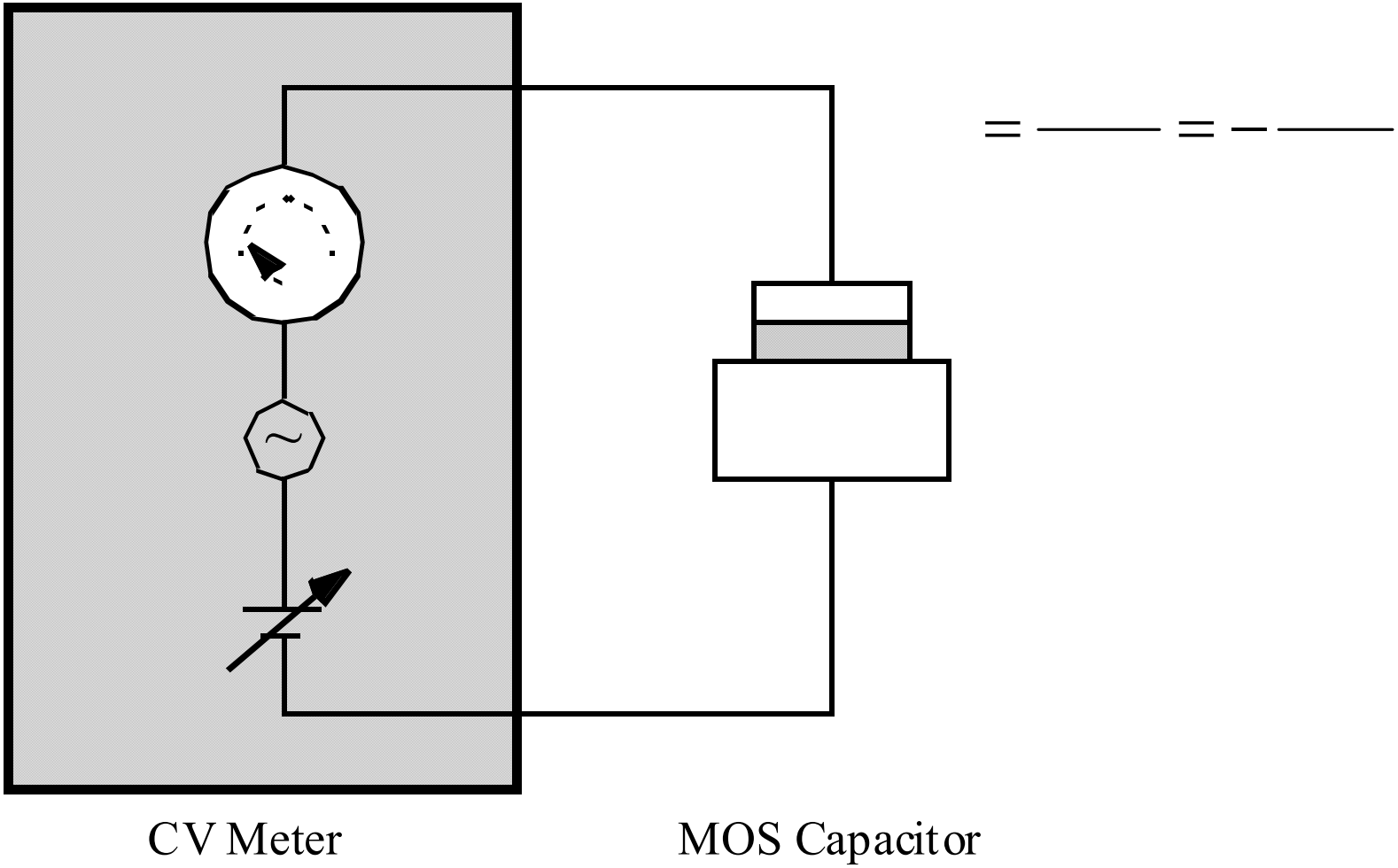


total substrate charge,

= + +

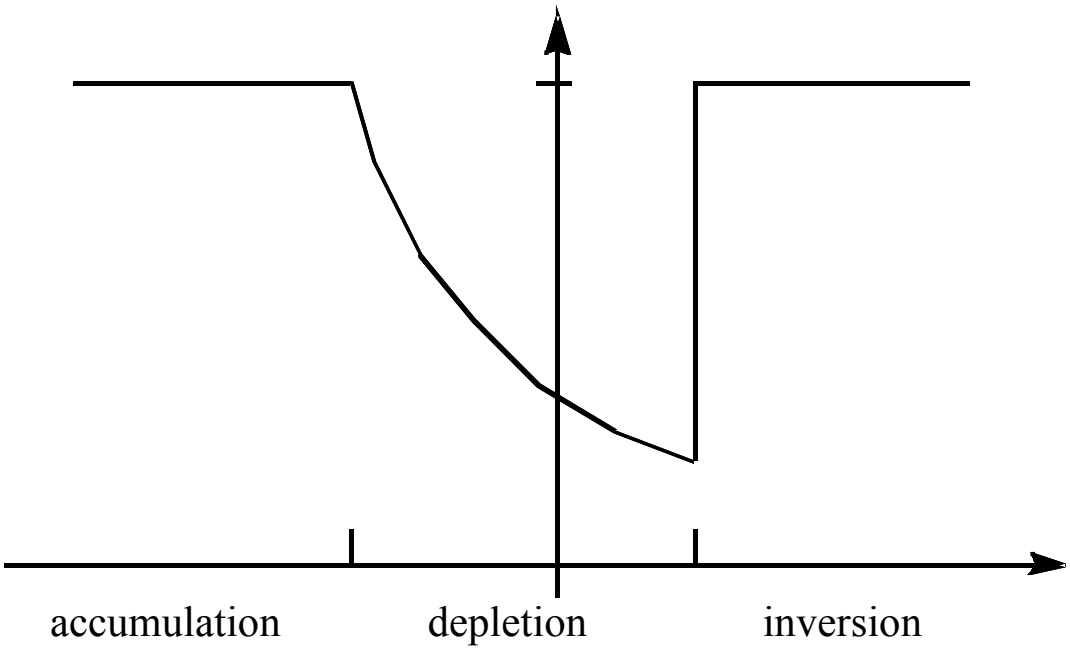


5.6 MOS CV Characteristics



5.6 MOS CV Characteristics

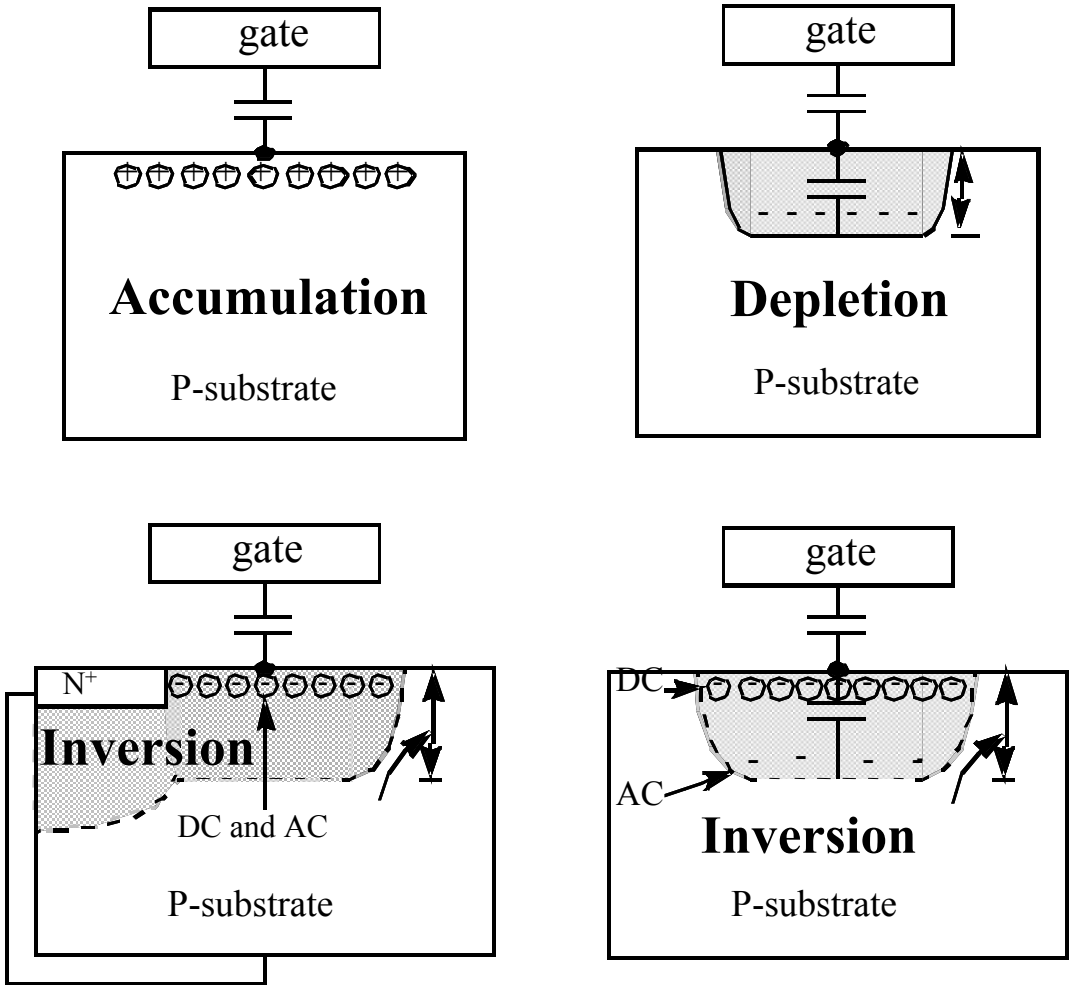
CV Characteristics



In the depletion regime: $\frac{1}{\ } = \frac{1}{\ } + \frac{1}{\ }$

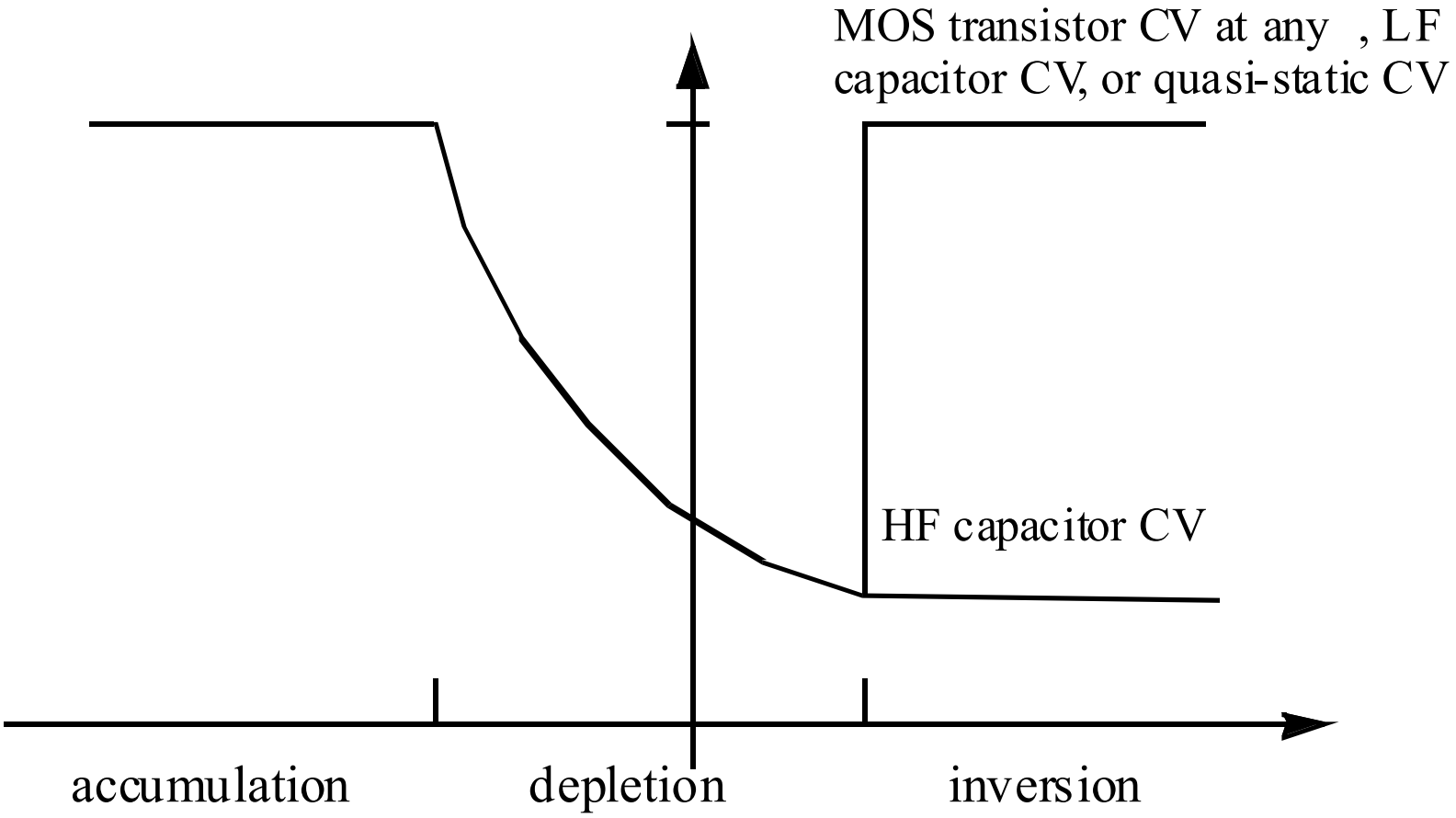
$$\frac{1}{\ } = \sqrt{\frac{1}{\ ^2} + \frac{2(\ \ - \ \ )}{\varepsilon}}$$

Supply of Inversion Charge May be Limited

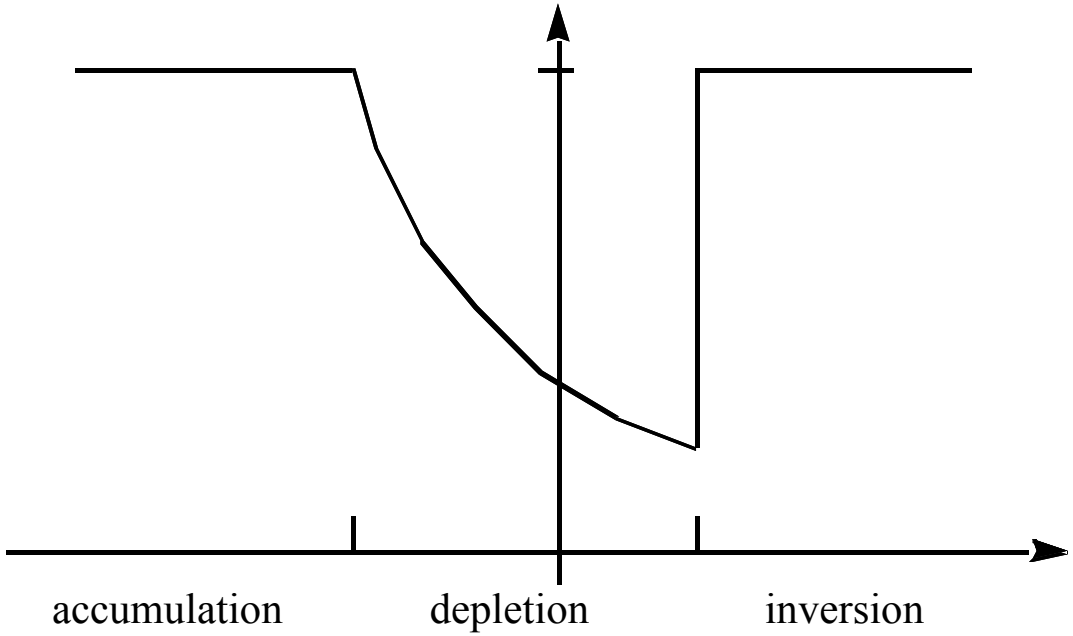


In each case, = ?

Capacitor and Transistor CV (or HF and LF CV)

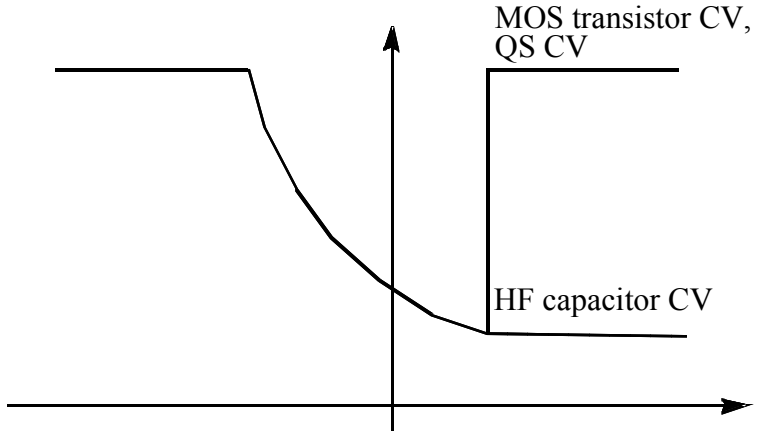


Quasi-Static CV of MOS Capacitor

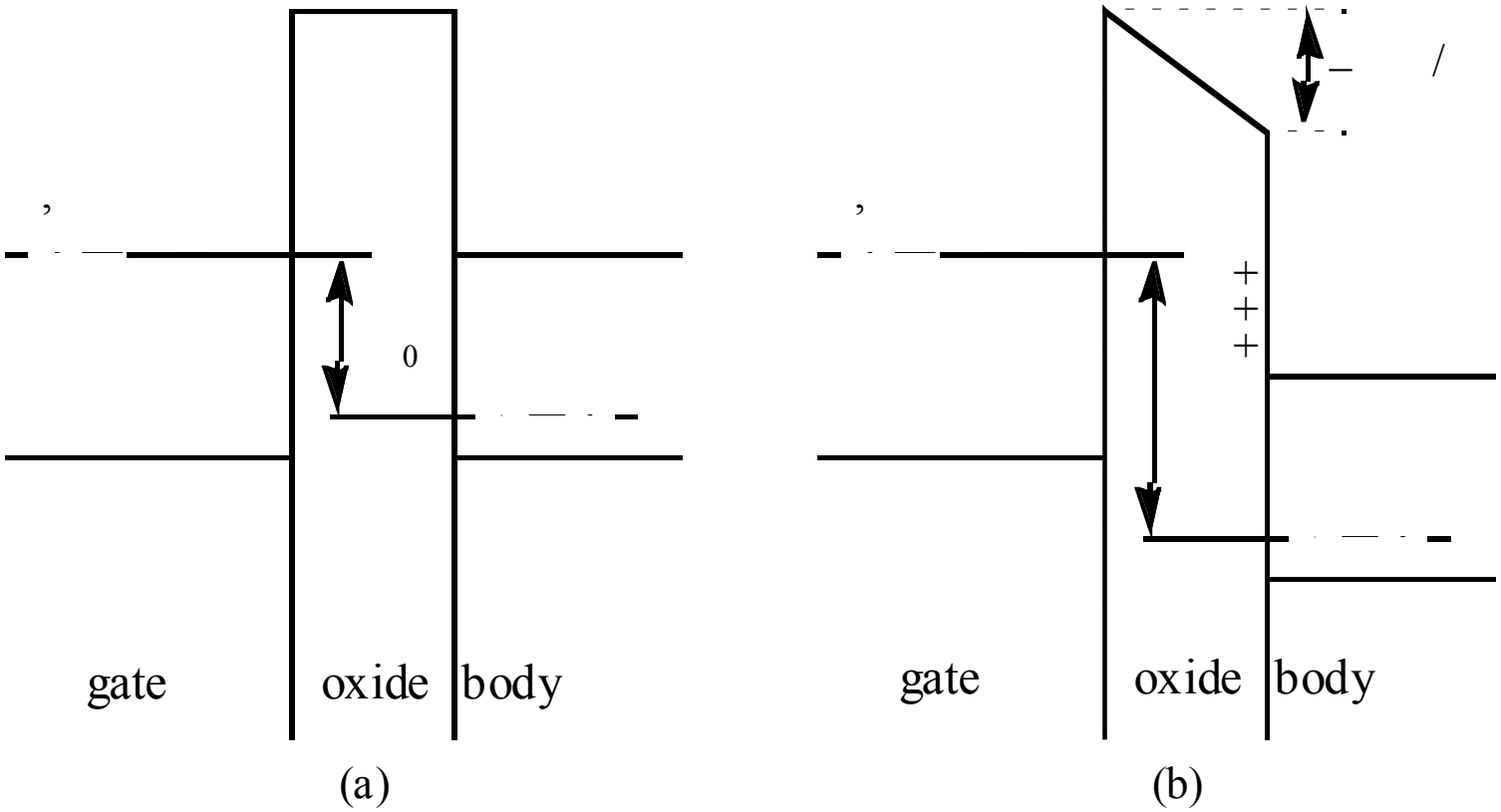


The quasi-static CV is obtained by the application of a slow linear-ramp voltage (< 0.1V/s) to the gate, while measuring with a very sensitive DC ammeter. is calculated from = · / . This allows sufficient time for to respond to the slow-changing .

EXAMPLE : CV of MOS Capacitor and Transistor



5.7 Oxide Charge–A Modification to V_{fb} and V_t



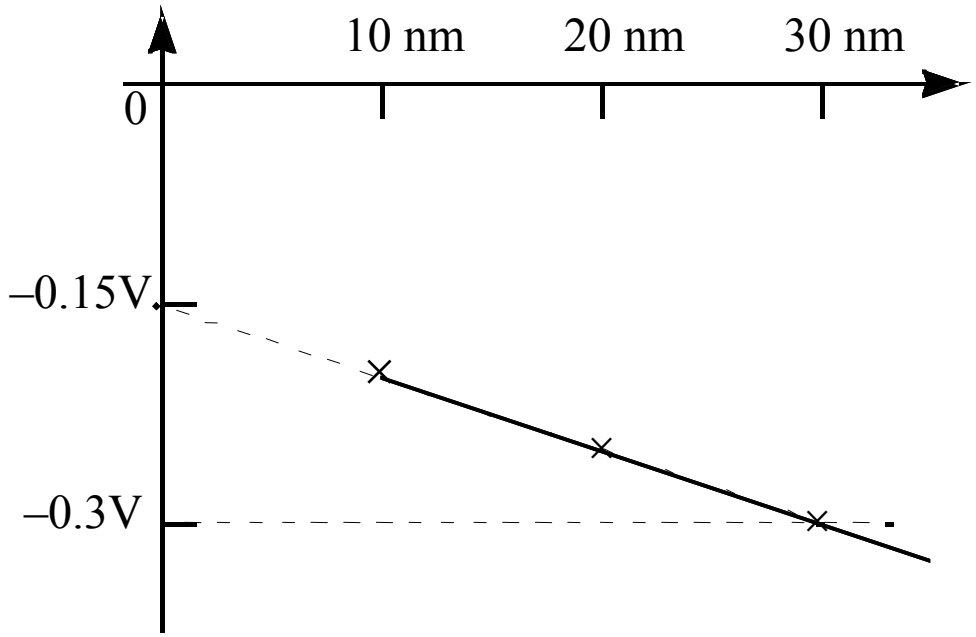
$$= \quad _0 - \quad / \qquad = \psi \quad - \psi \quad - \quad /$$

5.7 Oxide Charge–A Modification to V_{fb} and V_t

Three types of oxide charge:

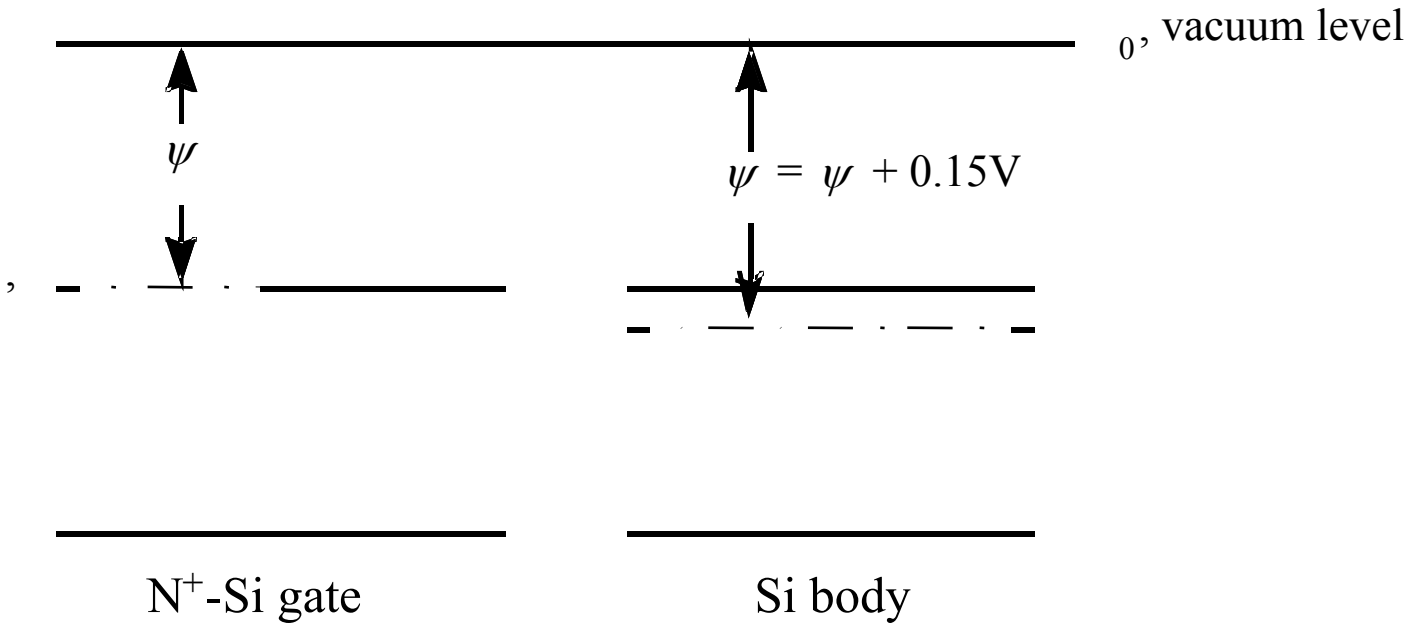
- Fixed oxide charge, Si^+
- Mobile oxide charge, Na^+
  (due to sodium contamination)
- Stress-induced charge-a reliability issue

EXAMPLE:



Solution: $= \psi \quad - \psi \quad - \qquad\qquad / \varepsilon$

$$\longrightarrow \psi \quad -\psi \quad = -0.15\ \mathrm{V}$$



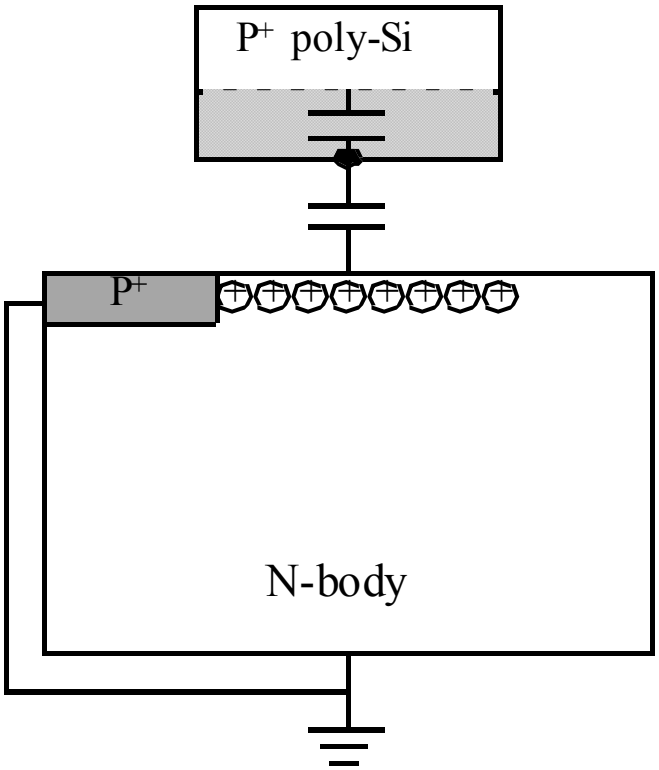
$$, \quad = \quad = \quad {}^{-0.15\ \mathrm{eV}/} \quad \approx 10^{17}\ \mathrm{cm}^{-3}$$

$$\longrightarrow \quad = 1.7 \times 10^{-8}\ \mathrm{C/cm}^{2}$$

5.8 Poly-Silicon Gate Depletion–Effective Increase in T_{ox}

Gauss's Law

$$= \varepsilon \quad \mathcal{E} \quad /$$



$$= \left(\frac{1}{\quad} + \frac{1}{\quad} \right)^{-1} = \left(\frac{\quad}{\varepsilon} + \frac{\quad}{\varepsilon} \right)^{-1}$$

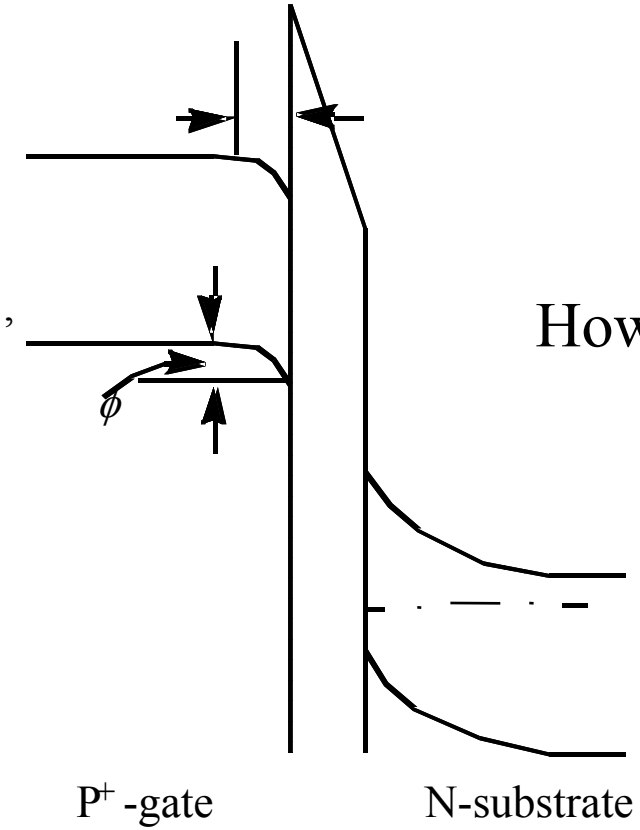
$$= \frac{\varepsilon}{\quad + \quad / 3}$$

If = 15 Å, what is the effective increase in ?

Why is a reduction in undesirable?

Effect of Poly-Gate Depletion on Q_{inv}

$$= \quad (\quad -\phi \quad - \quad)$$



How can poly-depletion by minimized?

EXAMPLE : Poly-Silicon Gate Depletion

+

$$= \quad \times$$

$$\phi$$

Solution:

$$= \varepsilon \quad \mathcal{E} \quad / \qquad = \varepsilon \qquad /$$

$$= \frac{3.9 \times 8.85 \times 10^{-14}\,(\mathrm{F/cm}) \cdot 1\,\mathrm{V}}{2 \times 10^{-7}\,\mathrm{cm} \cdot 1.6 \times 10^{-19}\,\mathrm{C} \cdot 8 \times 10^{19}\,\mathrm{cm}^{-3}}$$

$$= 1.3\,\mathrm{nm}$$

EXAMPLE : Poly-Silicon Gate Depletion

$$= \sqrt{\frac{2\varepsilon\,\phi}{}}$$

$$\phi \quad = \qquad {}^{2} \quad / 2\varepsilon \;\; = 0.11\,\mathrm{V}$$

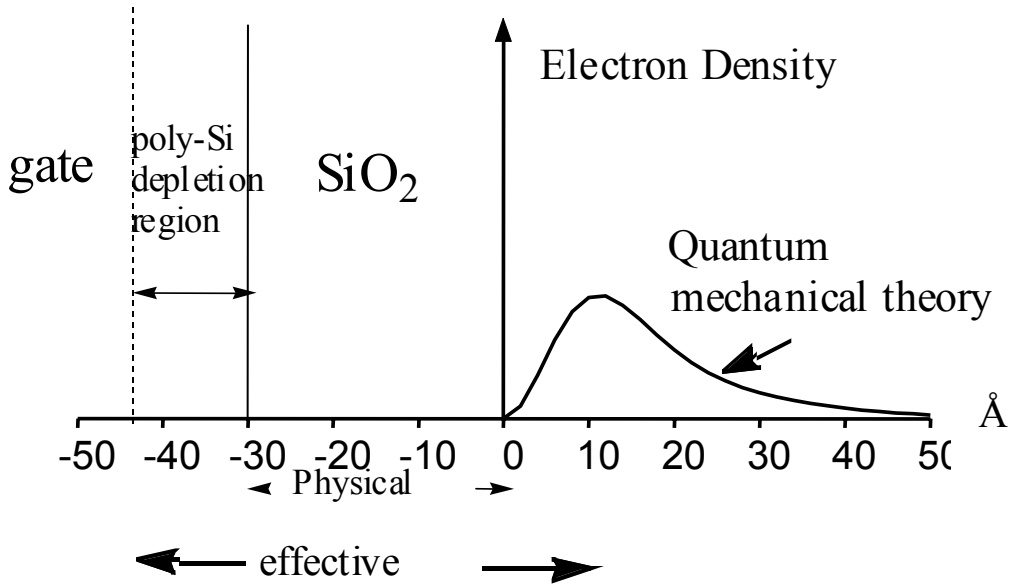
$$= \qquad + \phi \;\; + \qquad + \phi$$

$$= \frac{}{} - \frac{}{} \ln\left(\frac{}{}\right) = 1.1\,\mathrm{V} - 0.15\,\mathrm{V} = 0.95\,\mathrm{V}$$

$$= 0.95\,\mathrm{V} - 0.85\,\mathrm{V} - 1\,\mathrm{V} - 0.11\,\mathrm{V} = -1.01\,\mathrm{V}$$

5.9 *Inversion and Accumulation Charge-Layer Thickness–Quantum Mechanical Effect*

Average inversion-layer location below the Si/SiO_2 interface is called the ***inversion-layer thickness, T*** .

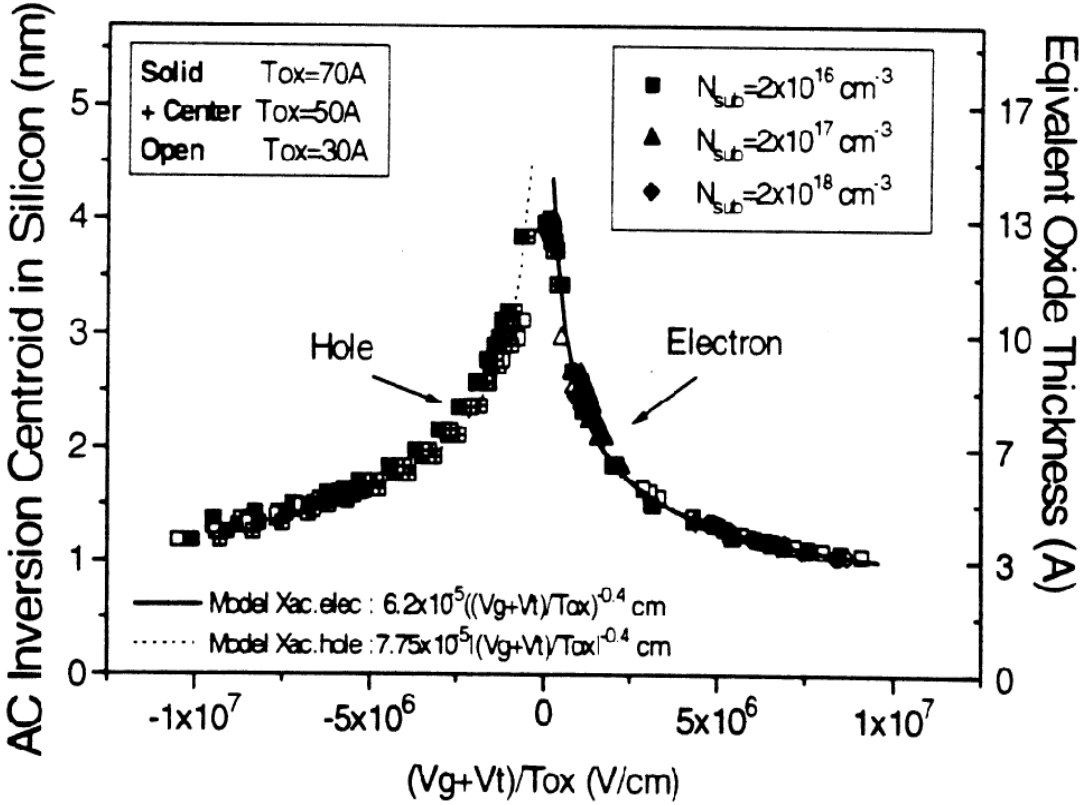


What equations need to be solved to find ( )?

Does change with varying ?

Electrical Oxide Thickness, T_{oxe}

= + /3 + /3 at

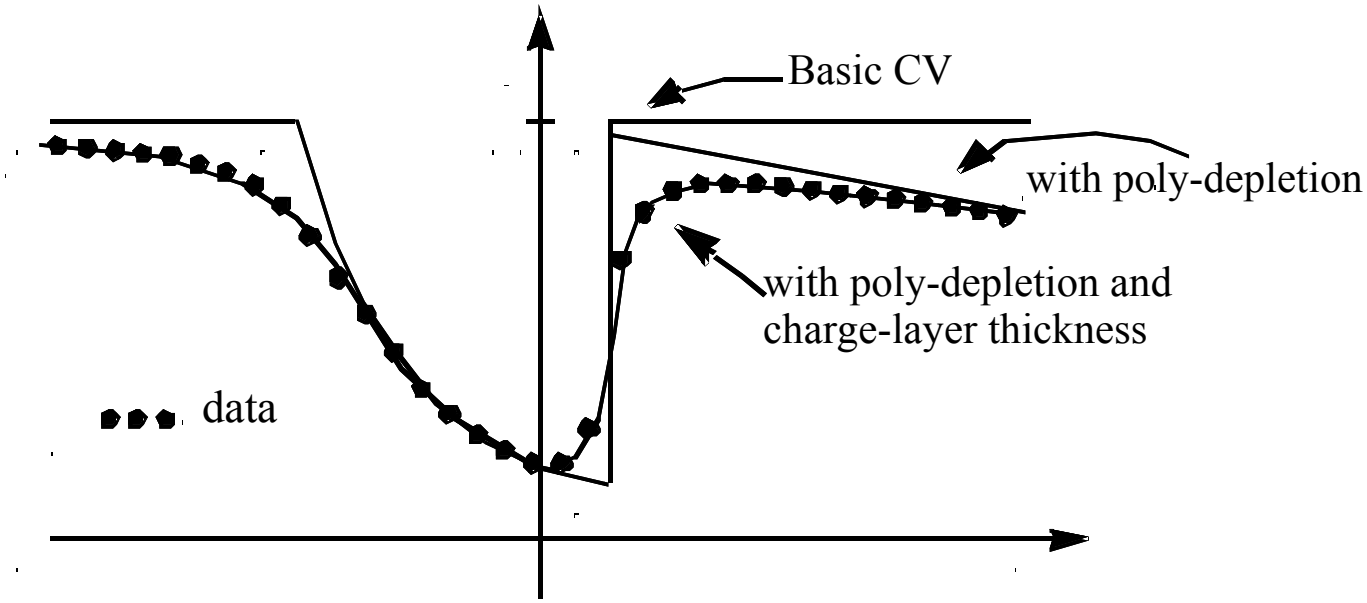


(+)/ can be shown to be the average electric field in the inversion layer. of holes is larger than that of electrons because of difference in effective mass.

Effective Oxide Thickness and Effective Oxide Capacitance

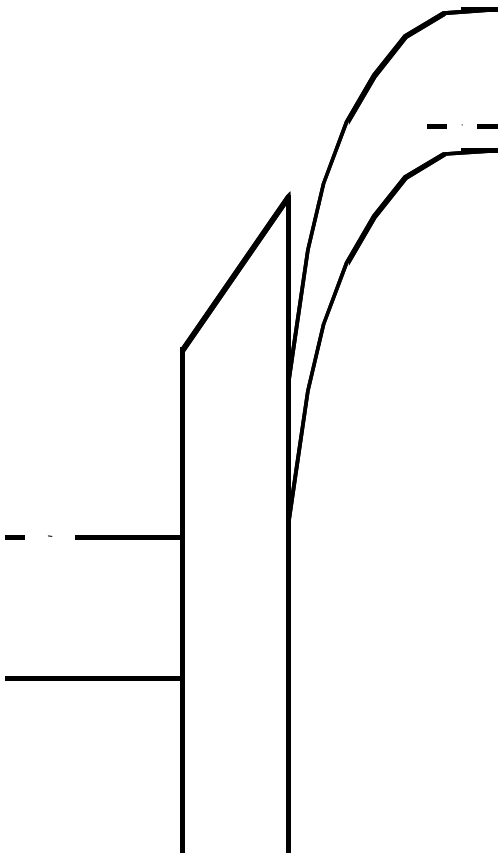
$$= \quad (\quad - \quad)$$

$$= \quad + \qquad /3 + \qquad /3$$

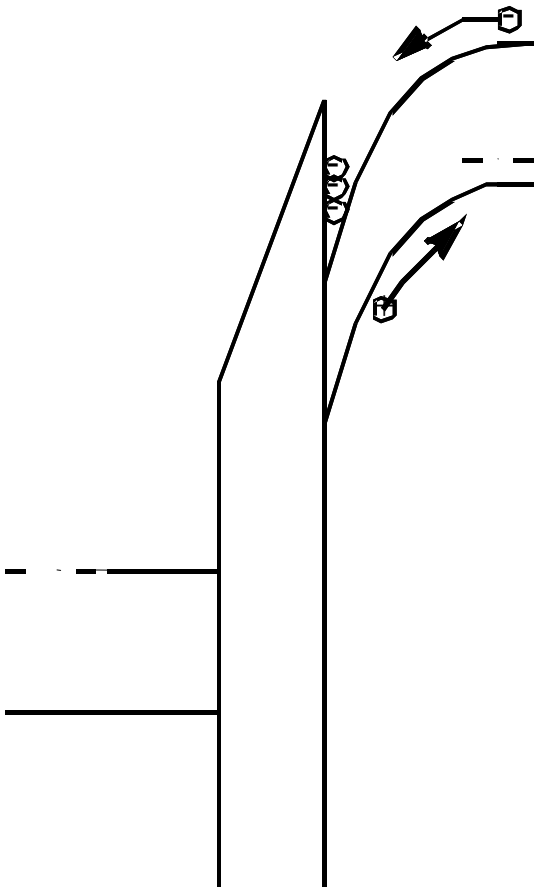


Which is worse in reduction : P^+-poly over N-body or N^+-poly over P-body?

5.10 CCD Imager



(a)

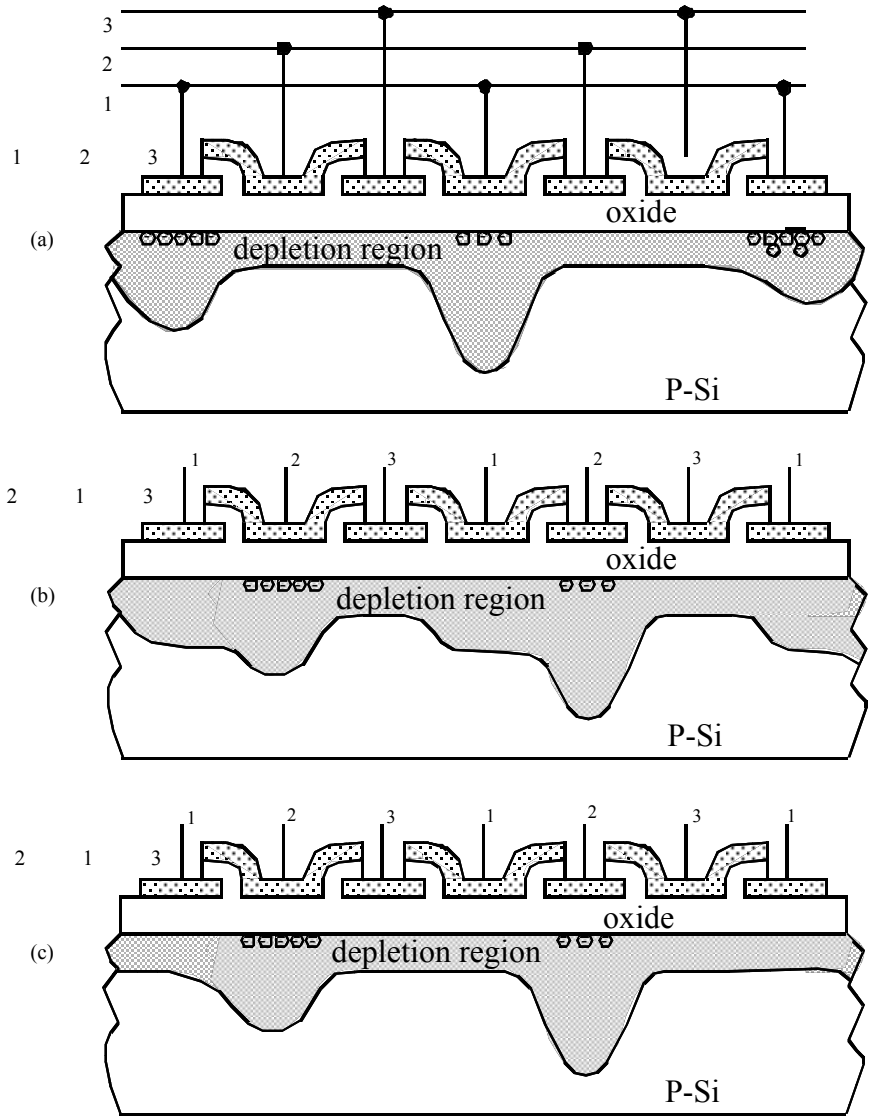


(b)

Deep depletion, = 0

Exposed to light

CCD Charge Transfer



5.11 Chapter Summary

N-type device: N^+-polysilicon gate over P-body

P-type device: P^+-polysilicon gate over N-body

$$= \psi \quad - \psi \ (- \qquad / \qquad)$$

$$= \qquad + \phi \ + \qquad (+ \phi \qquad)$$

$$= \qquad + \phi \ - \qquad / \qquad (+ \phi \qquad)$$

5.11 Chapter Summary

$$\phi = \pm 2\phi \quad \text{or} \quad \pm(\phi + 0.45\,\text{V})$$

$$\phi = \text{——} \ln \text{——}$$

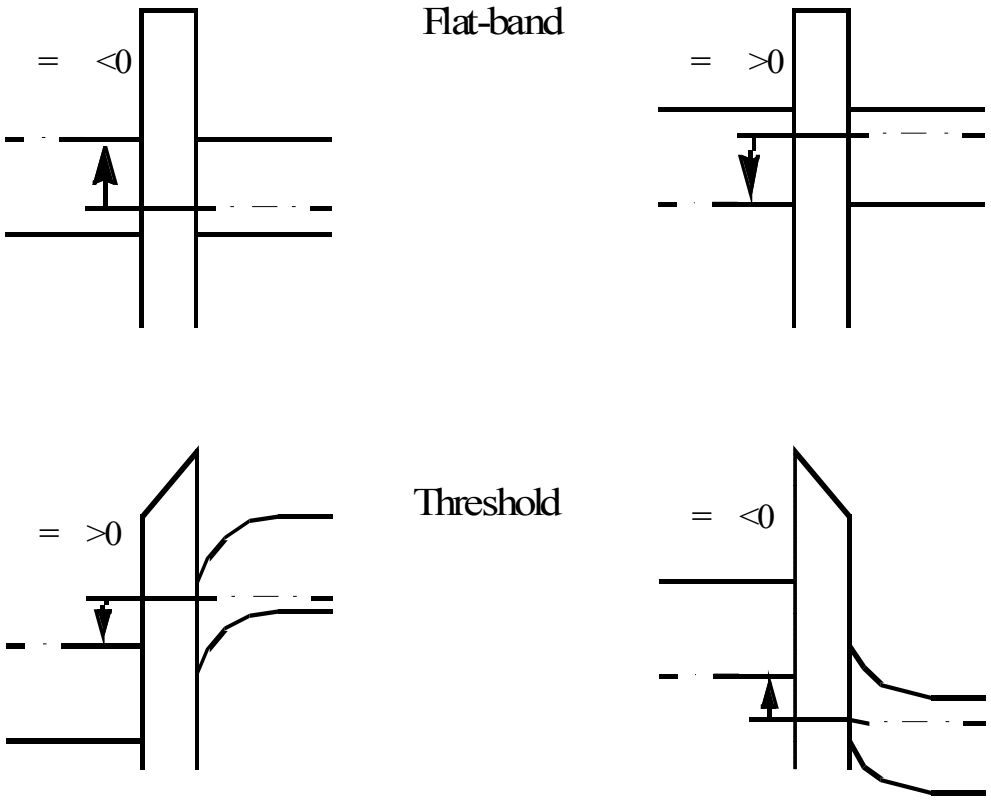
$$= \quad + \phi \pm \frac{\sqrt{2\varepsilon\,|\phi|}}{}$$

+ : N-type device, – : P-type device

5.11 Chapter Summary

N-type Device (N$^+$-gate over P-substrate)

P-type Device (P$^+$-gate over N-substrate)

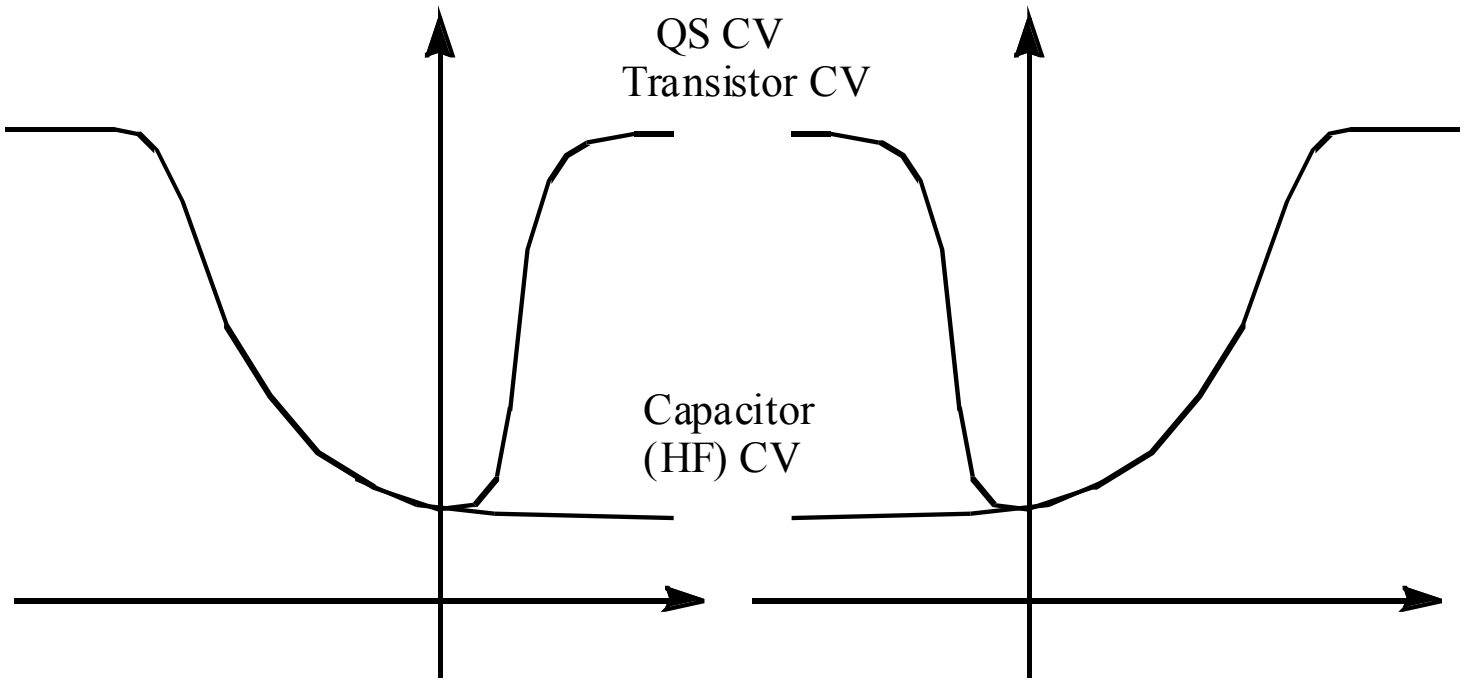


What's the diagram like at > ? at = 0?

5.11 Chapter Summary

N-type Device
(N^+-gate over P-substrate)

P-type Device
(P^+-gate over N-substrate)



What is the root cause of the low in the HF CV branch?