Chapter 6 MOSFET in the On-state

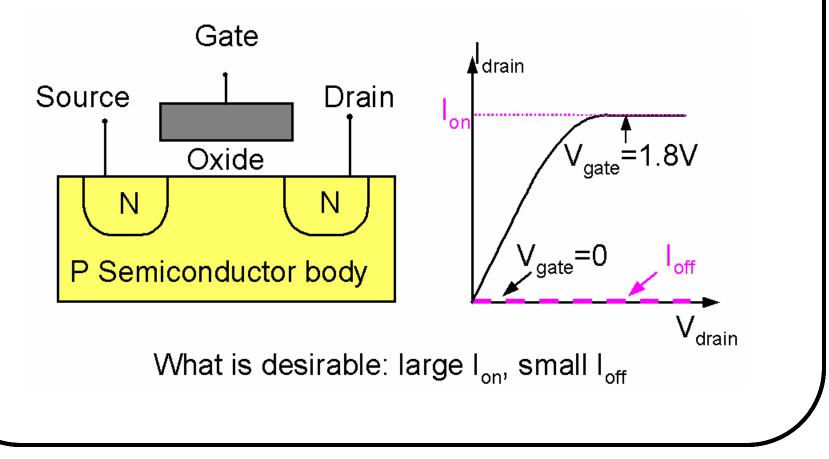
The MOSFET (MOS Field-Effect Transistor) is the building block of Gb memory chips, GHz microprocessors, analog, and RF circuits.

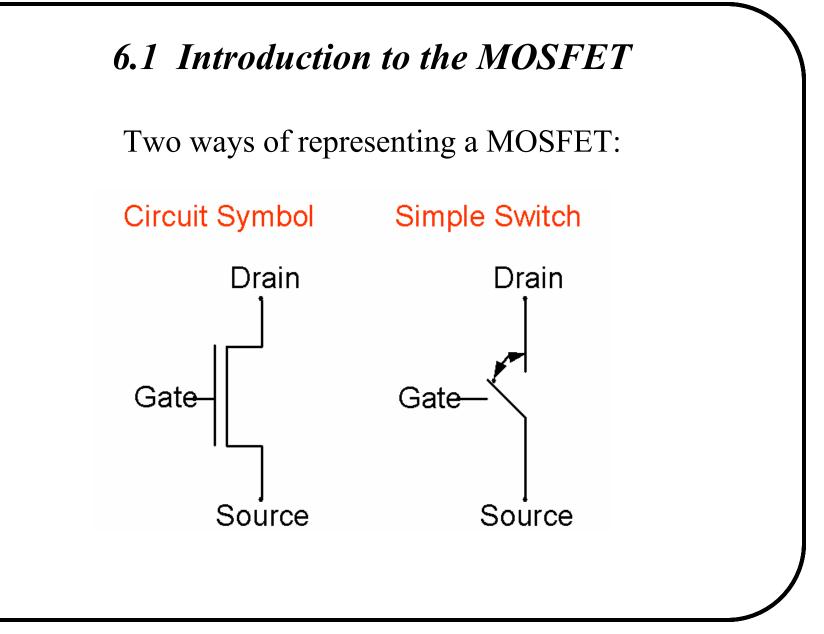
Match the following MOSFET characteristics with their applications:

- small size
- high speed
- low power
- high gain

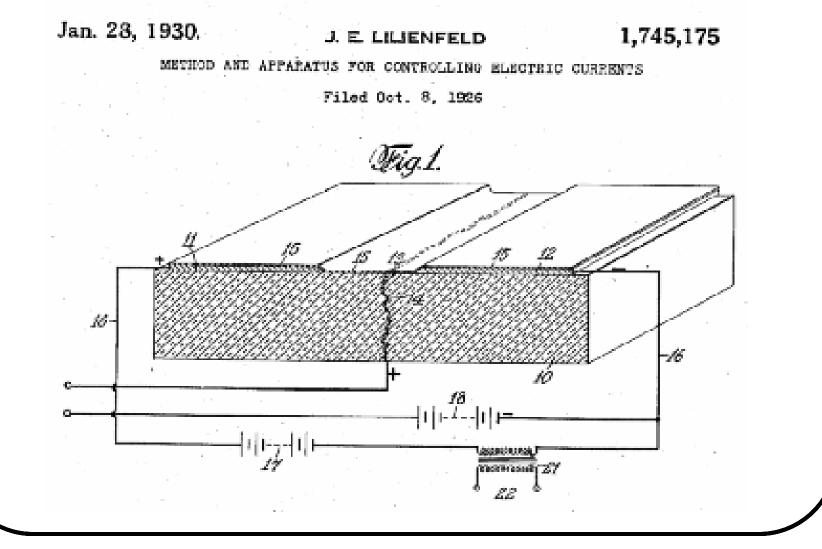
6.1 Introduction to the MOSFET

Basic MOSFET structure and IV characteristics

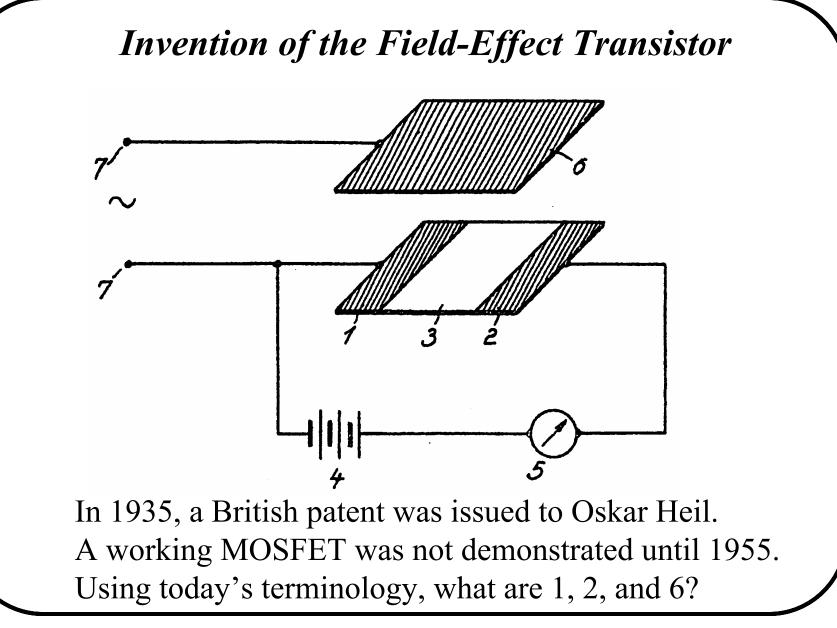




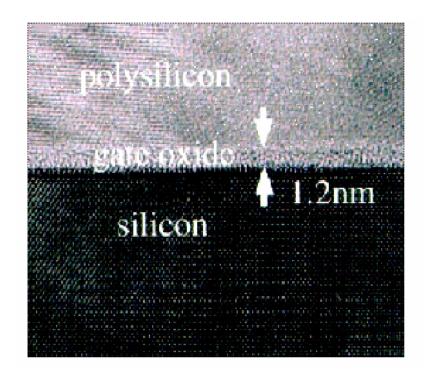
Invention of the Field-Effect Transistor



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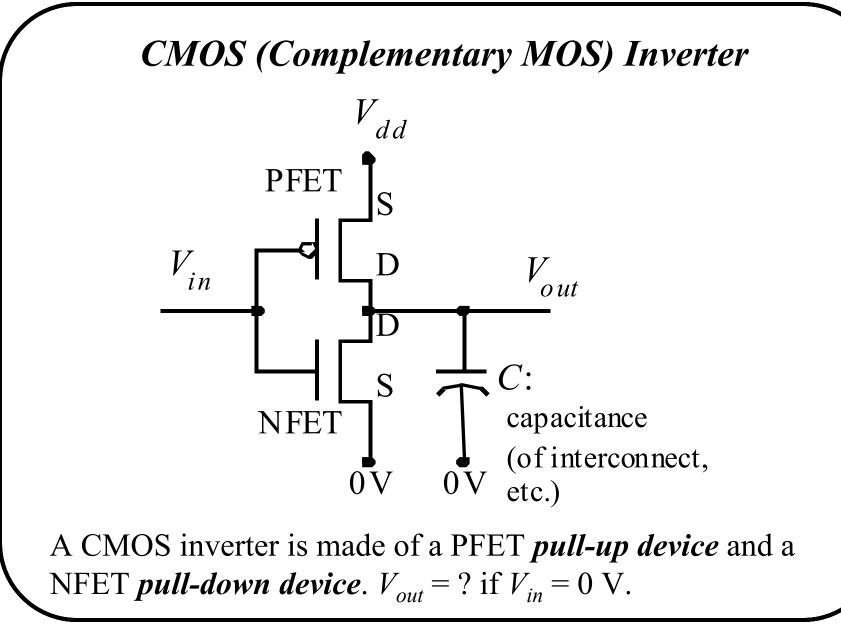
Today's MOSFET Technology

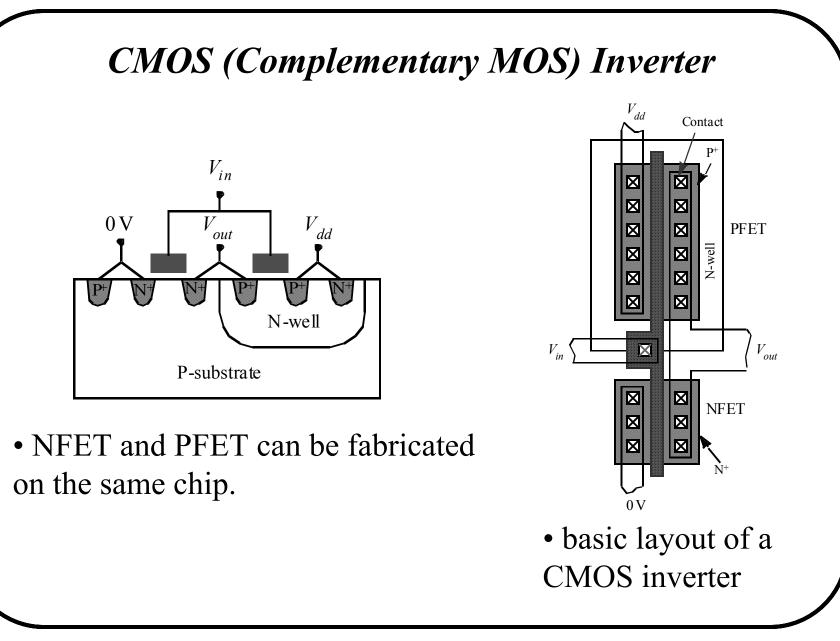


Gate oxides as thin as 1.2 nm can be manufactured reproducibly. Large tunneling current through the oxide limits oxide-thickness reduction.

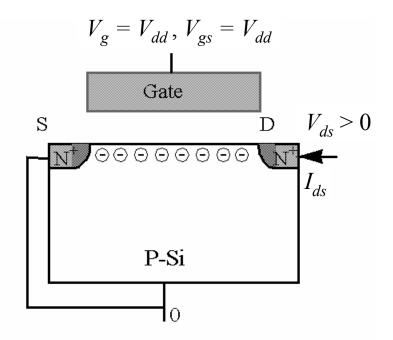
6.2 Complementary MOSFETs NFET PFET $V_g = 0$ $V_g = V_{dd}$ Gate Gate S $D - V_{ds} > 0$ S $D V_{ds} \leq V_{dd}$ $\Theta \Theta \Theta \Theta \Theta \Theta \Theta \Theta$ I_{ds} L_{ds} P-Si N-Si 0 V_{dd}

When $V_g = V_{dd}$, the NFET is on and the PFET is off. When $V_g = 0$, the PFET is on and the NFET is off.





6.3 Surface Mobilities of Electrons and Holes



How to measure the surface mobility:

$$I_{ds} = W \cdot Q_{inv} \cdot v = W Q_{inv} \mu_{ns} \mathcal{E} = W Q_{inv} \mu_{ns} V_{ds} / L$$
$$= W C_{oxe} (V_g - V_t) \mu_{ns} V_{ds} / L$$

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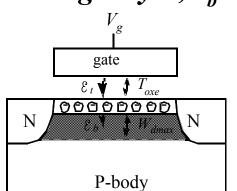
Surface mobility is a function of the average of the fields at the bottom and the top of the inversion charge layer, \mathcal{E}_b and \mathcal{E}_t .

From Gauss's Law,

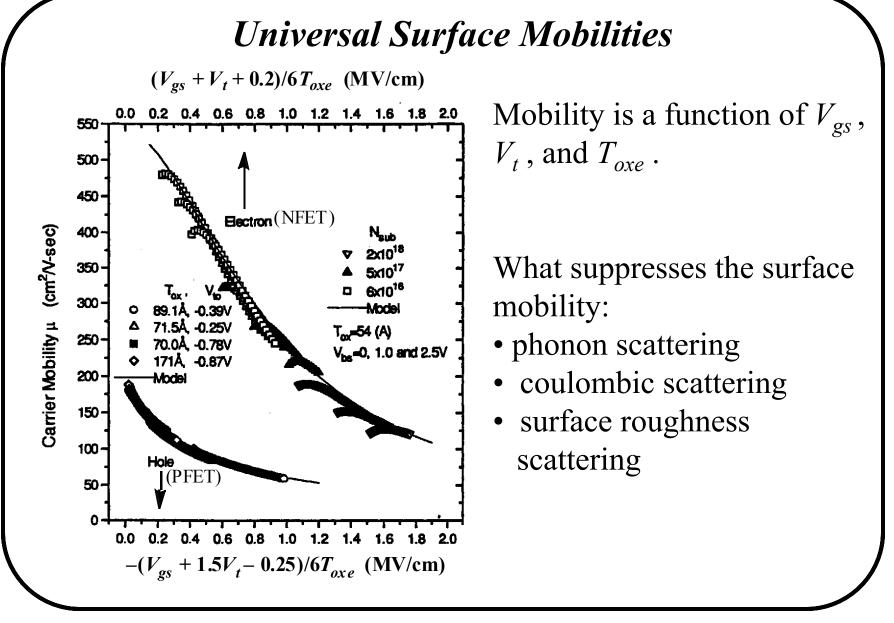
$$\mathcal{E}_b = -Q_{dep}/\mathcal{E}_s$$

$$V_t = V_{fb} + \phi_{st} - Q_{dep} / C_{oxe}$$

Therefore,



$$\begin{split} \mathcal{E}_{b} &= \frac{C_{oxe}}{\varepsilon_{s}} (V_{t} - V_{fb} + \phi_{st}) & \therefore \frac{1}{2} (\mathcal{E}_{b} + \mathcal{E}_{t}) = \frac{C_{oxe}}{2\varepsilon_{s}} (V_{gs} + V_{t} - 2V_{fb} - 2\phi_{st}) \\ \mathcal{E}_{t} &= -(Q_{dep} + Q_{inv})/\varepsilon_{s} \\ &= \mathcal{E}_{b} - Q_{inv}/\varepsilon_{s} = \mathcal{E}_{b} + \frac{C_{oxe}}{\varepsilon_{s}} (V_{gs} - V_{t}) \\ &= \frac{C_{oxe}}{\varepsilon_{s}} (V_{gs} - V_{fb} + \phi_{st}) \end{split} \qquad \approx \frac{2}{\varepsilon_{s}} (V_{gs} + V_{t} + 0.2 \text{ V}) \\ &= \frac{V_{gs} + V_{t} + 0.2 \text{ V}}{6T_{oxe}} \end{split}$$

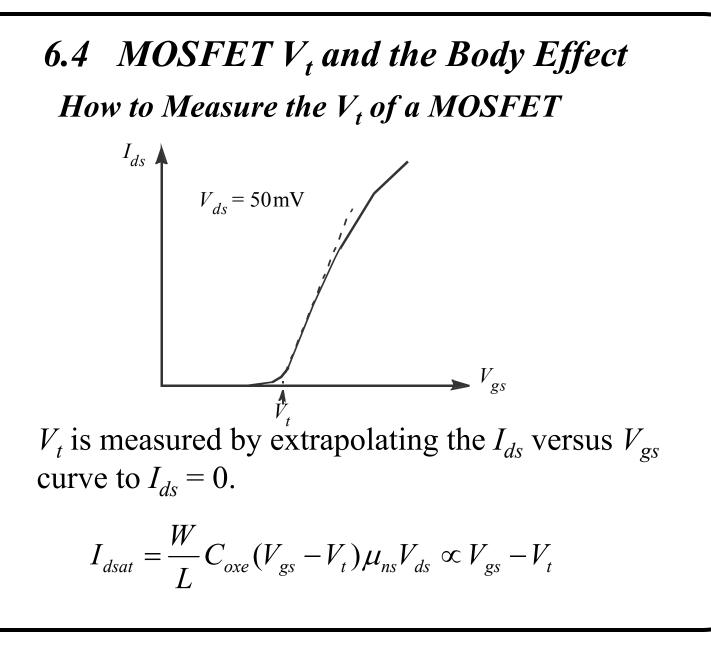


EXAMPLE: What is the surface mobility at $V_{gs}=1$ V in an N-channel MOSFET with $V_t=0.3$ V and $T_{oxe}=2$ nm?

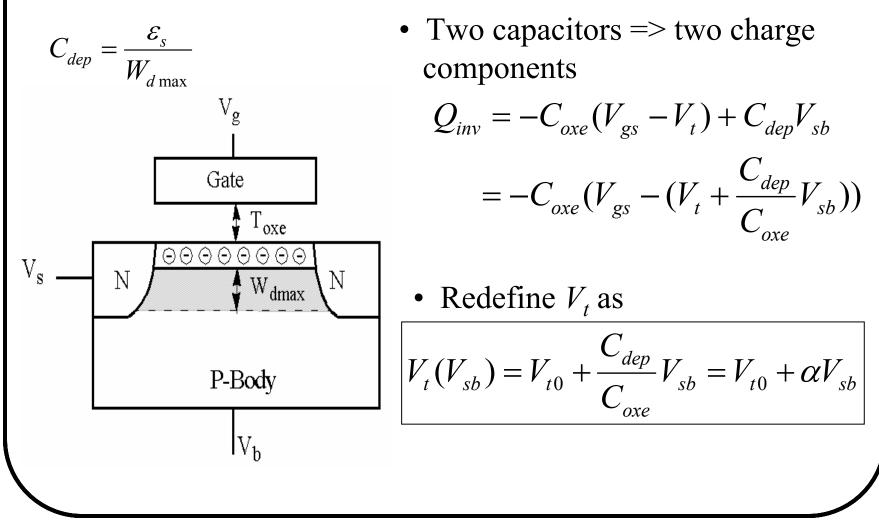
Solution:
$$(V_{gs} + V_t + 0.2) / 6T_{oxe}$$

= 1.5 V / 12×10⁻⁷ cm
= 1.25 MV/cm

1 MV is a megavolt (10⁶ V). From the mobility figure, μ_{ns} =190 cm2/Vs, which is several times smaller than the bulk mobility.



6.4 MOSFET V_t and the Body Effect

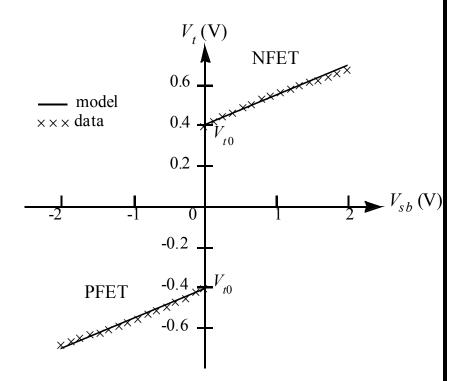


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6.4 MOSFET V_t and the Body Effect

• body effect: V_t is a function of V_{sb} • body effect coefficient: $\alpha = C_{dep}/C_{oxe}$ $= 3T_{oxe}/W_{dmax}$

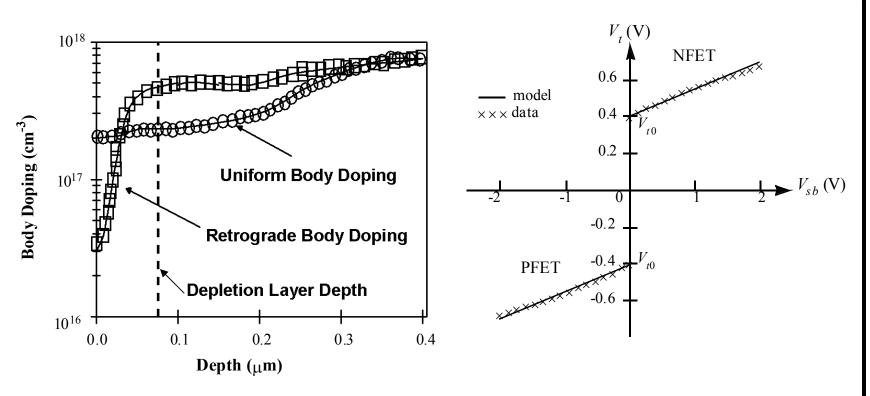
When the source-body junction is reverse-biased, the NFET V_t increases and the PFET V_t becomes more negative.



Is the body effect a good thing? How can it be reduced?

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Retrograde Body Doping Profiles



- W_{dep} does not vary with V_{sb} .
- Retrograde doping is popular because it reduces off-state leakage.

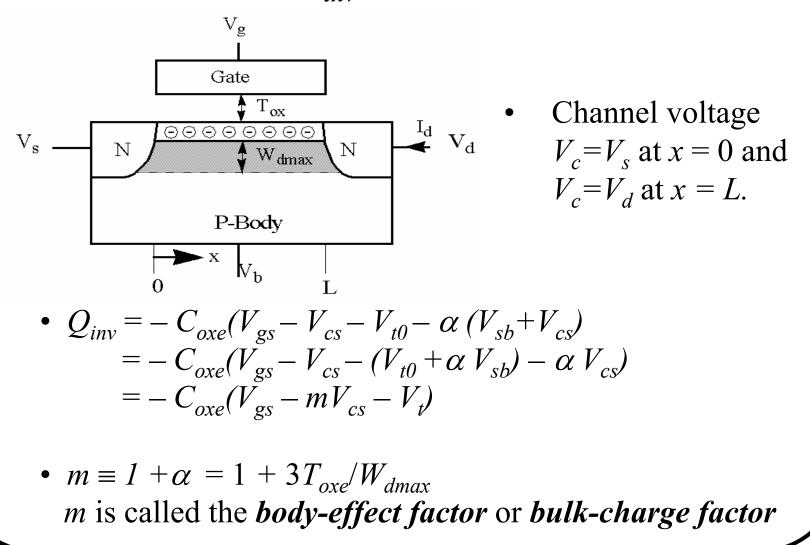
Uniform Body Doping

When the source/body junction is reverse-biased, there are two quasi-Fermi levels (E_{fn} and E_{fp}) which are separated by qV_{sb} . An NMOSFET reaches threshold of inversion when E_c is close to E_{fn} , not E_{fp} . This requires the band-bending to be $2\phi_B + V_{sb}$, not $2\phi_B$.

$$V_t = V_{t0} + \frac{\sqrt{qN_a 2\varepsilon_s}}{C_{oxe}} (\sqrt{2\phi_B + V_{sb}} - \sqrt{2\phi_B})$$
$$\equiv V_{t0} + \gamma (\sqrt{2\phi_B + V_{sb}} - \sqrt{2\phi_B})$$

 γ is the **body-effect parameter**.





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6.6 Basic MOSFET IV Model

$$I_{ds} = WQ_{inv}v = WQ_{inv}\mu_{ns}\mathcal{E}$$

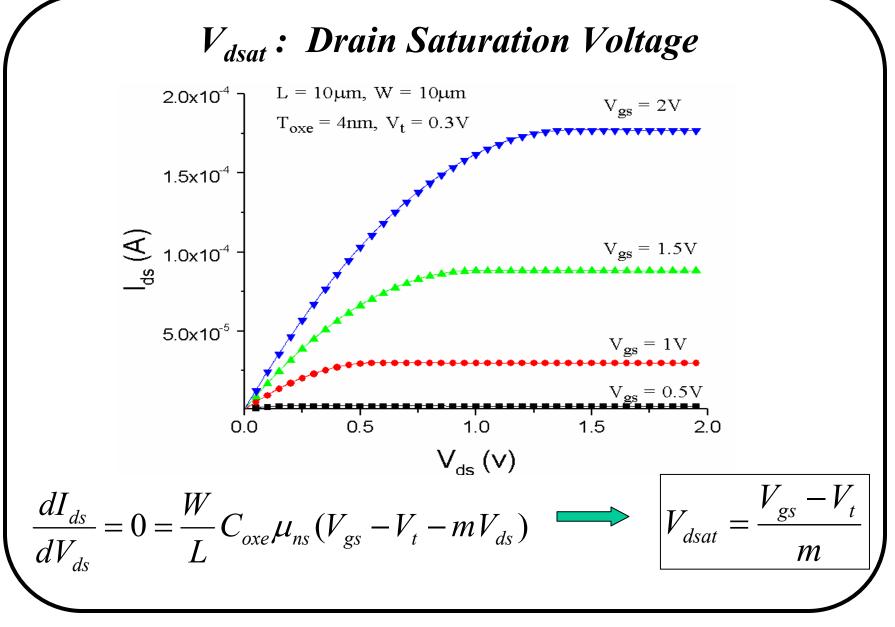
$$= WC_{oxe}(V_{gs} - mV_{cs} - V_{t})\mu_{ns}dV_{cs}/dx$$

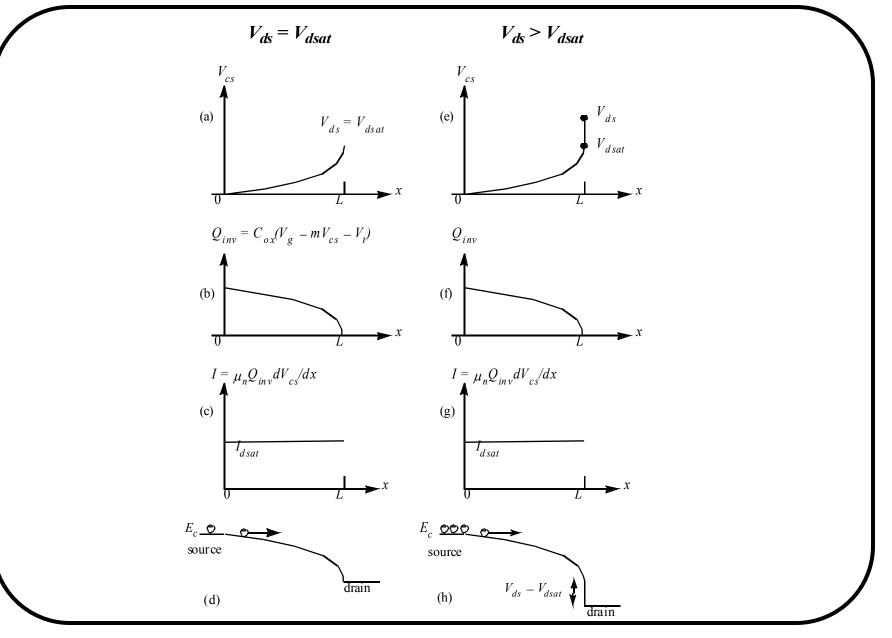
$$\int_{0}^{L} I_{ds}dx = WC_{oxe}\mu_{ns}\int_{0}^{V_{ds}} (V_{gs} - mV_{cs} - V_{t})dV_{cs}$$

$$I_{ds}L = WC_{oxe}\mu_{ns}(V_{gs} - V_{t} - mV_{ds}/2)V_{ds}$$

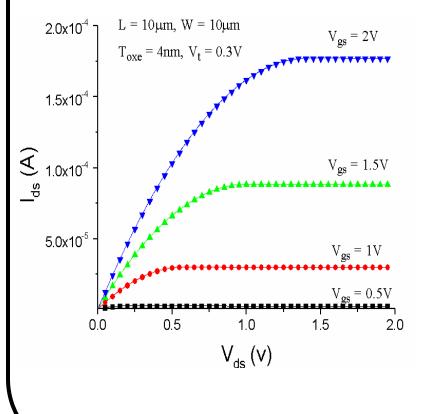
$$I_{ds} = \frac{W}{L}C_{oxe}\mu_{s}(V_{gs} - V_{t} - \frac{m}{2}V_{ds})V_{ds}$$

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Saturation Current and Transconductance



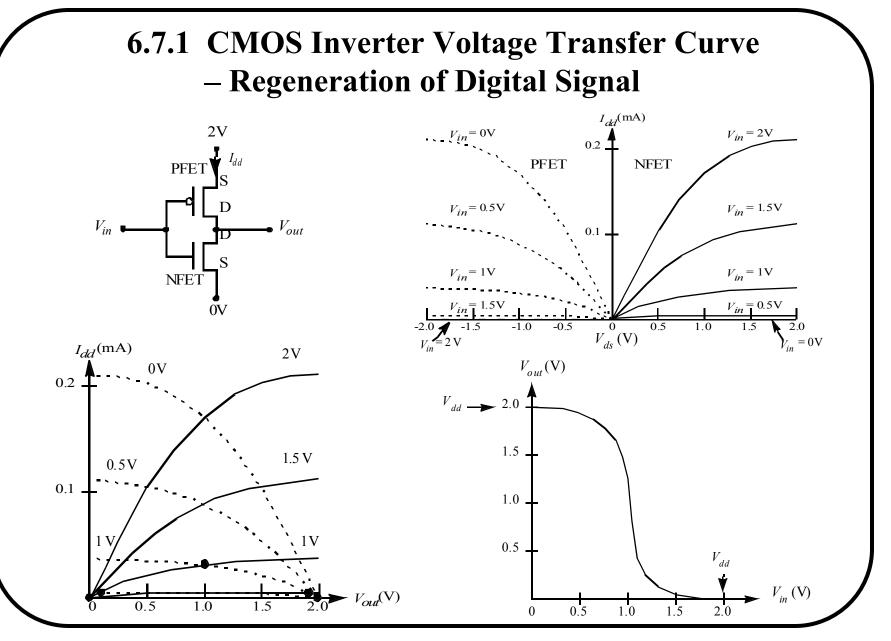
• linear region, saturation region

$$I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_{ns} (V_{gs} - V_t)^2$$

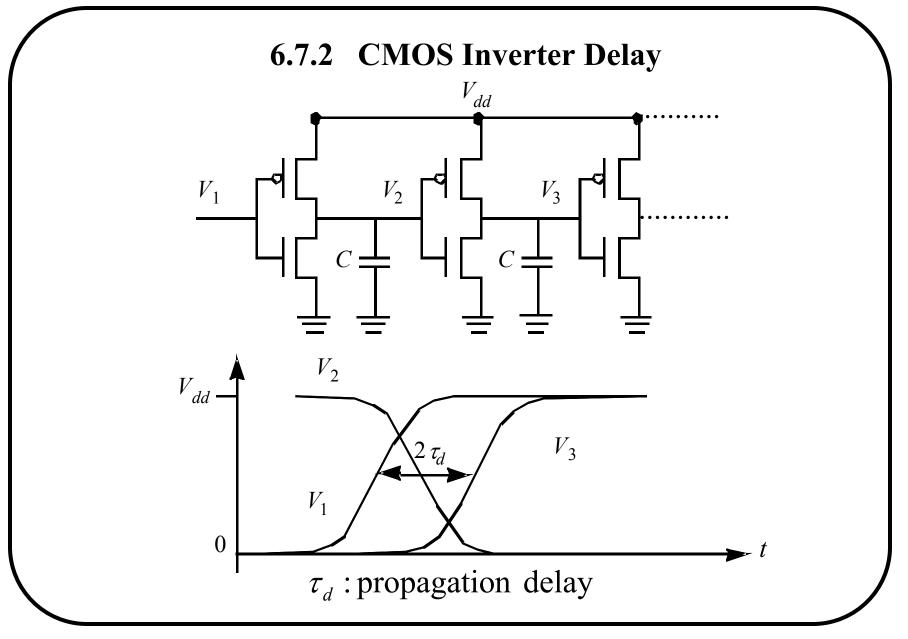
• transconductance: $g_m = dI_{ds}/dV_{gs}$

$$g_{msat} = \frac{W}{mL} C_{oxe} \mu_{ns} (V_{gs} - V_t)$$

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6.7.2 CMOS Inverter Delay

$$\tau_{d} = \frac{1}{2} (pull - down \ delay + pull - up \ delay)$$

$$pull - up \ delay \approx \frac{CV_{dd}}{2I_{dsatP}}$$

$$pull - down \ delay \approx \frac{CV_{dd}}{2I_{dsatN}}$$

$$\tau_{d} = \frac{CV_{dd}}{4} (\frac{1}{I_{dsatN}} + \frac{1}{I_{dsatP}})$$

$$R_{N} \text{ and } R_{P} = \frac{V_{dd}}{2I_{on}} = \frac{V_{dd}}{2I_{dsat}(|V_{g}| = V_{dd})}$$

How can the speed of an inverter circuit be improved?

6.7.3 CMOS Power Consumption

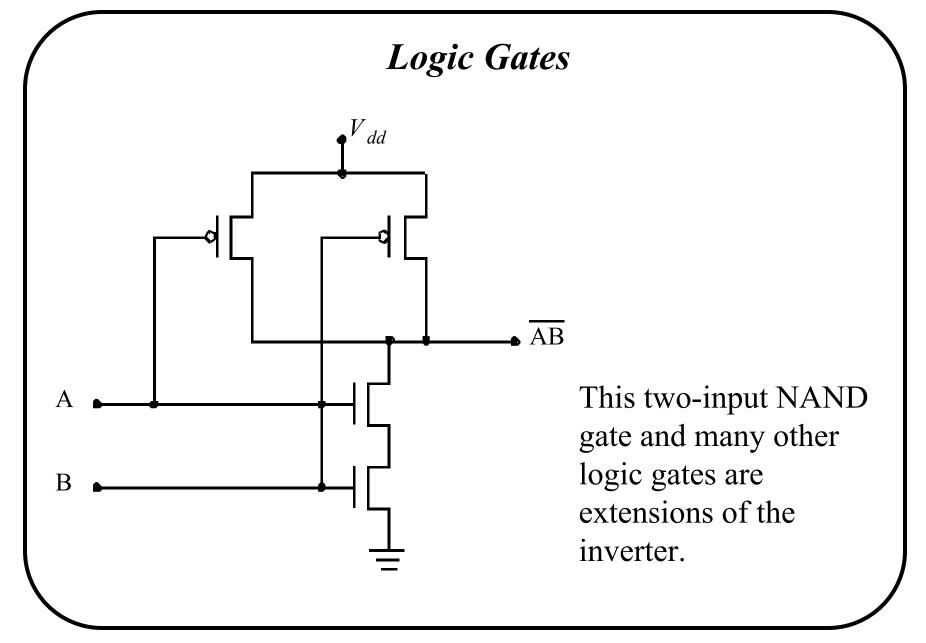
$$P_{dynamic} = V_{dd} \times average \ current = CV_{dd}^2 f$$

$$P_{\rm static} = V_{\rm dd} I_{\rm off}$$

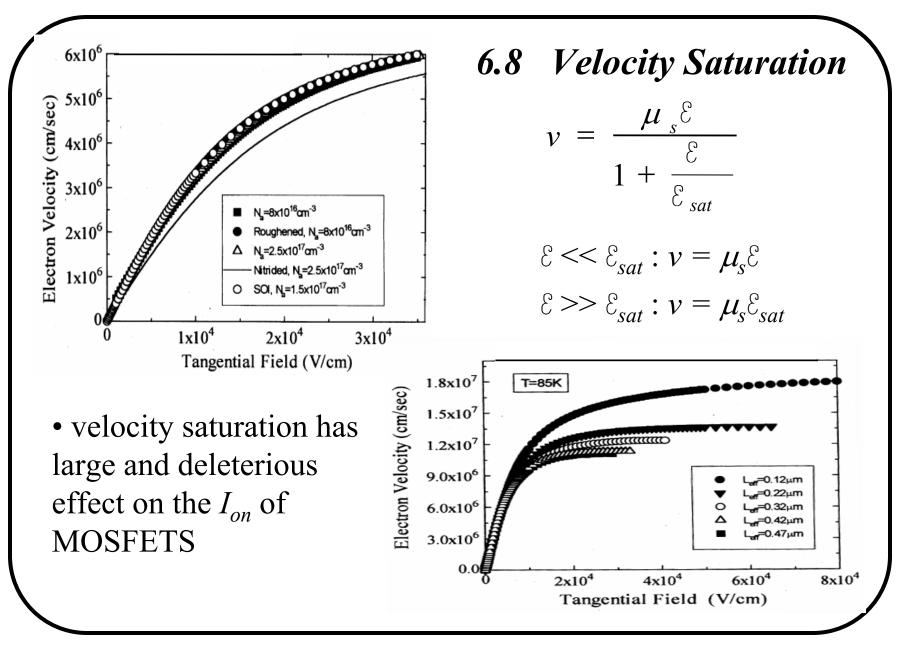
$$\begin{split} P_{direct-path} \approx V_{dd} \, \frac{I_{dsat}}{5} \frac{t_r + t_f}{2} \, f = 0.2 C V_{dd}^2 f \\ = 0.2 P_{dynamic} \end{split}$$

Total power consumption

$$P = 1.2CV_{dd}^2 f + V_{dd}I_{off}$$



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6.9 MOSFET IV Model with Velocity Saturation

$$I_{ds} = WQ_{inv}v$$

$$I_{ds} = WC_{oxe}(V_{gs} - mV_{cs} - V_t)\frac{\mu_{ns}dV_{cs}/dx}{1 + \frac{dV_{cs}}{dx}/\mathcal{E}_{sat}}$$

$$\int_0^L I_{ds}dx = \int_0^{V_{ds}} [WC_{oxe}\mu_{ns}(V_{gs} - mV_{cs} - V_t) - I_{ds}/\mathcal{E}_{sat}]dV_{cs}$$

$$I_{ds}L = WC_{oxe}\mu_{ns}(V_{gs} - V_t - \frac{m}{2}V_{ds})V_{ds} - I_{ds}V_{ds}/\mathcal{E}_{sat}$$

6.9 MOSFET IV Model with Velocity Saturation

$$I_{ds} = \frac{\frac{W}{L}C_{oxe}\mu_{ns}(V_{gs} - V_t - \frac{m}{2}V_{ds})V_{ds}}{1 + \frac{V_{ds}}{\mathcal{E}_{sat}L}}$$

$$I_{ds} = \frac{long - channel I_{ds}}{1 + V_{ds} / \mathcal{E}_{sat} L}$$

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6.9 MOSFET IV Model with Velocity Saturation

Solving
$$\frac{dI_{ds}}{dV_{ds}} = 0$$
,
 $V_{dsat} = \frac{2(V_{gs} - V_t)/m}{1 + \sqrt{1 + 2(V_{gs} - V_t)/m\mathcal{E}_{sat}L}}$

A simpler and more accurate V_{dsat} is:

$$\frac{1}{V_{dsat}} = \frac{m}{V_{gs} - V_t} + \frac{1}{\mathcal{E}_{sat}L}$$

$$\hat{\nabla}$$

$$\mathcal{E}_{sat} = \frac{2v_{sat}}{\mu_s}$$

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EXAMPLE: Drain Saturation Voltage

Question: At $V_{gs} = 1.8 V$, what is the V_{dsat} of an NFET with $T_{oxe} = 3 nm$, $V_t = 0.25 V$, and $W_{dmax} = 45 nm$ for (a) $L = 10 \mu m$, (b) L = 1 um, (c) $L = 0.1 \mu m$, and (d) $L = 0.05 \mu m$?

Solution: From V_{gs} , V_t , and T_{oxe} , μ_{ns} is 200 cm²V⁻¹s⁻¹.

$$\mathcal{E}_{sat} = 2v_{sat}/\mu_{es} = 8 \times 10^4 \text{ V/cm}$$
$$m = 1 + 3T_{oxe}/W_{dmax} = 1.2$$
$$V_{dsat} = \left(\frac{m}{V_{gs} - V_t} + \frac{1}{\mathcal{E}_{sat}L}\right)^{-1}$$

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EXAMPLE: Drain Saturation Voltage

$$V_{dsat} = \left(\frac{m}{V_{gs} - V_t} + \frac{1}{\mathcal{E}_{sat}L}\right)^{-1}$$

(a) $L = 10 \ \mu m$, $V_{dsat} = (1/1.3 \text{V} + 1/80 \text{V})^{-1} = 1.3 \text{ V}$

(b)
$$L = 1 \ \mu m$$
, $V_{dsat} = (1/1.3 \text{V} + 1/8 \text{V})^{-1} = 1.1 \text{ V}$

(c) $L = 0.1 \ \mu m$, $V_{dsat} = (1/1.3 \text{V} + 1/.8 \text{V})^{-1} = 0.5 \text{ V}$

(d)
$$L = 0.05 \ \mu m$$
, $V_{dsat} = (1/1.3 \text{V} + 1/.4 \text{V})^{-1} = 0.3 \text{ V}$

I_{dsat} with Velocity Saturation

Substituting V_{dsat} for V_{ds} in I_{ds} equation gives:

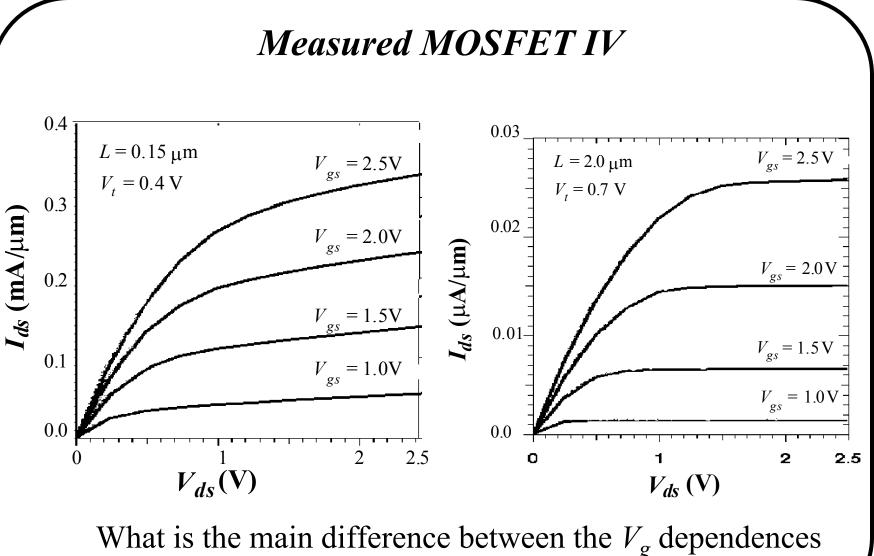
$$I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_s \frac{\left(V_{gs} - V_t\right)^2}{1 + \frac{V_{gs} - V_t}{m\mathcal{E}_{sat}L}} = \frac{long - channel I_{dsat}}{1 + \frac{V_{gs} - V_t}{m\mathcal{E}_{sat}L}}$$

Very short channel case: $\mathcal{E}_{sat}L \ll V_{gs} - V_t$

$$I_{dsat} = \frac{W}{2} C_{oxe} \mu_s \mathcal{E}_{sat} (V_{gs} - V_t)$$
$$= W_{v_{sat}} C_{oxe} (V_{gs} - V_t - \mathcal{E}_{sat} L)$$

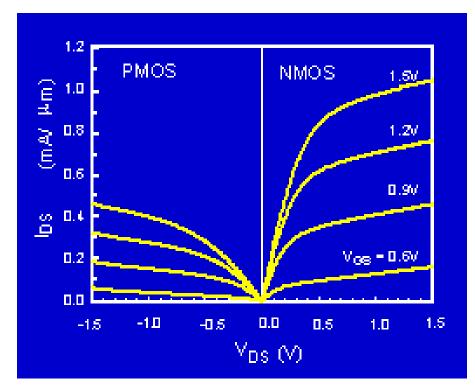
• I_{dsat} is proportional to $V_{gs} - V_t$ rather than $(V_{gs} - V_t)^2$, not as sensitive to L as 1/L.

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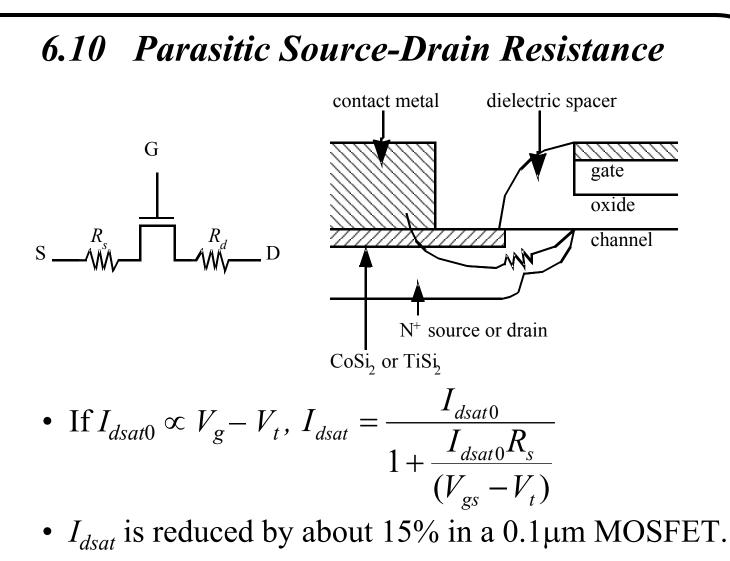


of the long- and short-channel length IV curves?

PMOS and NMOS IV Characteristics

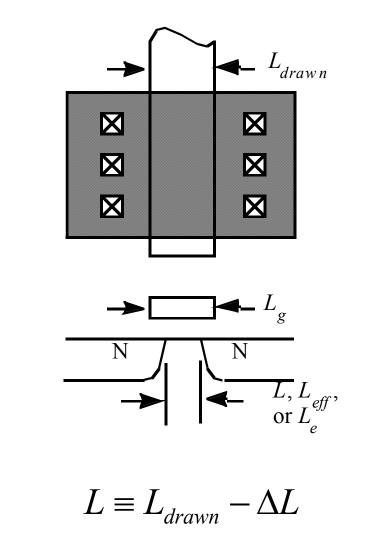


The PMOS IV is qualitatively similar to the NMOS IV, but the current is about half as large. How can we design a CMOS inverter so that its voltage transfer curve is symmetric?



•
$$V_{dsat} = V_{dsat0} + I_{dsat}(R_s + R_d)$$

Definitions of Channel Length



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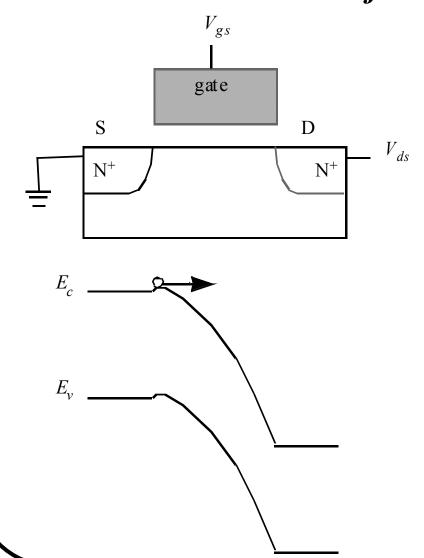
6.11 Extraction of the Series Resistance and the Effective Channel Length

$$I_{ds} = \frac{WC_{oxe}\mu_{s}V_{ds}}{L_{drawn} - \Delta L} (V_{gs} - V_{t})$$

$$V_{ds} = \frac{I_{ds}(L_{drawn} - \Delta L)}{WC_{oxe}(V_{gs} - V_{t})\mu_{s}}$$

$$\frac{V_{ds}}{I_{ds}} (\Omega)^{300} + (V_{gs} - V_{t}) + (V_{gs} - V_{t}$$

6.12 Source Injection Velocity Limit



• Carrier velocity is limited by the thermal velocity when they first enter the channel from the source.

•
$$I_{dsat} = WBv_{thx}Q_{inv}$$

= $WBv_{thx}C_{oxe}(V_{gs} - V_t)$

6.13 Chapter Summary

- body effect $V_t(V_{sb}) = V_{t0} + \alpha V_{sb}$ for steep retrograde body doping $\alpha = 3T_{oxe} / W_{dmax}$
 - basic I_{ds} model

$$I_{ds} = \frac{W}{L} C_{oxe} \mu_s (V_{gs} - V_t - \frac{m}{2} V_{ds}) V_{ds}$$

 $m = 1 + 3T_{oxe} / W_{dmax} \approx 1.2$

- Small α and *m* are desirable. Therefore, small T_{oxe} is good. Ch.7 shows that large W_{dmax} is not acceptable.
- CMOS circuit speed is determined by CV_{dd}/I_{dsat} , and its power by $CV_{dd}^2f + V_{dd}I_{off}$.

6.13 Chapter Summary

IV characteristics can be divided into a *linear region* and a *saturation region*.

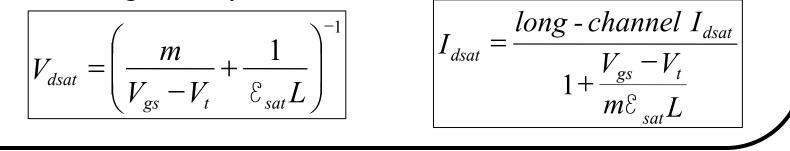
 I_{ds} saturates at:

$$V_{dsat} = \frac{V_{gs} - V_t}{m}$$
$$I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_s (V_{gs} - V_t)^2$$

transconductance:

$$g_{msat} = \frac{W}{mL} C_{oxe} \mu_s (V_{gs} - V_t)$$

Considering velocity saturation,



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