

1. OPA334

a. From the data sheet , we see that

$$V_{ss} - 0.1V < V_{cm} < V_{dd} - 1.5V$$

The input common mode voltage must remain at least 1.5V below vdd.

The input common mode voltage can be below Vss.

$$V_{ic, \max} = V_{dd} - 1.5$$

$$V_{ic, \min} = V_{ss} - 0.1 \quad (V_{ic, \min} < 0 \text{ if } V_{ss} = 0)$$

What kind of topology is it ?

For a simple differential amplifier,  $V_{ic, \min} = V_T + 2V_{dsat} + V_{ss} > 0$  (if  $V_{ss} = 0$ )

but our data sheet says  $V_{ic, \min} = V_{ss} - 0.1 = -0.1$  (if  $V_{ss} = 0$ )

Since these 2 facts contradict each other, the topology can not be a simple differential amp.

For a telescopic amplifier,  $V_{ic, \min} = V_T + 2V_{dsat} + V_{ss} > 0$  (if  $V_{ss} = 0$ ) .

The same analysis applies. So it's not a telescopic amplifier.

For a folded cascode amplifier with nmos transistors as the input pair,

$$V_{ic, \min} = V_T + 2V_{dsat} + V_{ss} > 0 \quad (\text{if } V_{ss} = 0) .$$

But our data sheet says  $V_{ic, \min} < 0$  . Contradiction!

**For a folded cascode amplifier with pmos transistors as the input pair,**

$$V_{ic, \min} = V_{dsat} - V_T + V_{ss} .$$

**We see that we can meet this spec if  $V_T > V_{dsat} + 0.1$**

**Since the output range is fairly large, this means the output is driven by an output stage.**

**It could be an inverter, or maybe a common source.**

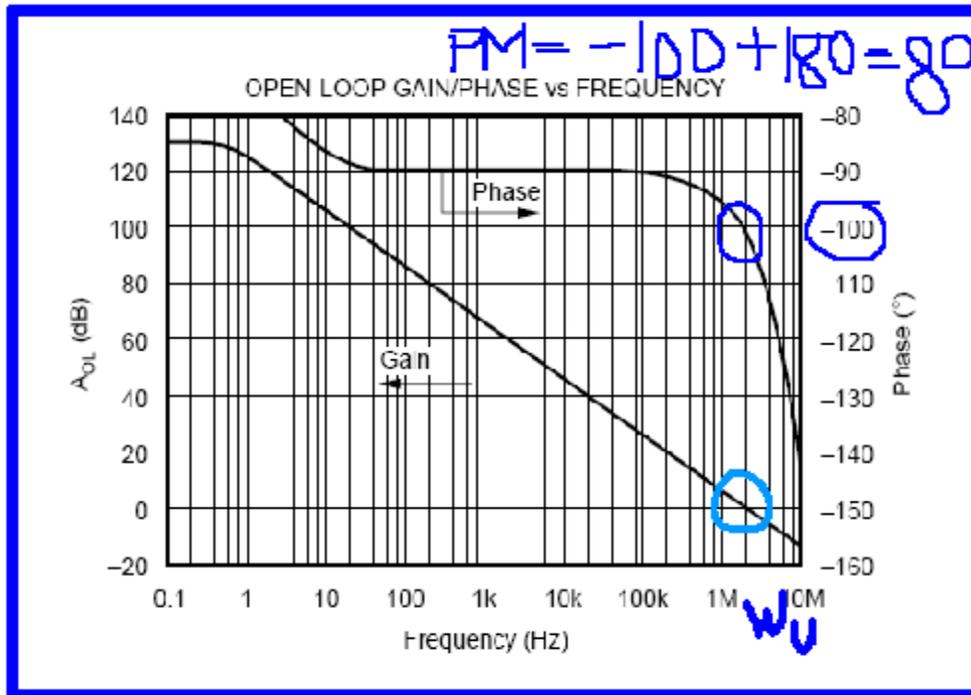
b. Typical value:

Low frequency gain = 130 dB

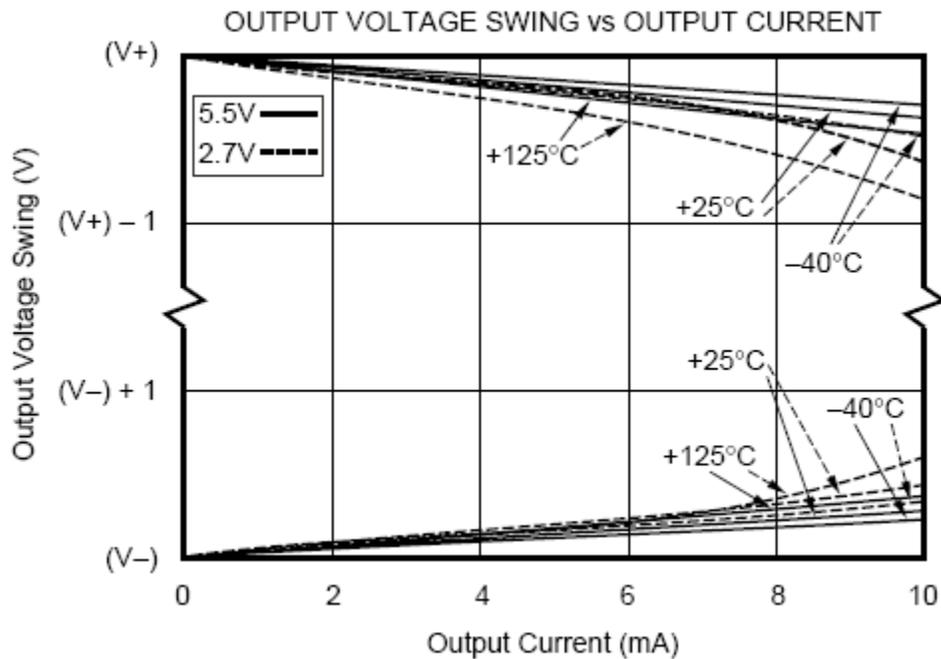
$$130 \text{ dB} = 20\text{dB} * \log ( A_v )$$

$$A_v \approx 3.16 \times 10^6 \text{ Volts/Volts}$$

c. As we can see on the following plot, phase margin is 80 degrees.



- d. Output voltage range when output current = 1mA is about from  $V_{SS}+0.1$  to  $V_{DD}-0.1$ . Very close to rail to rail swing.



Problem 2.

a.

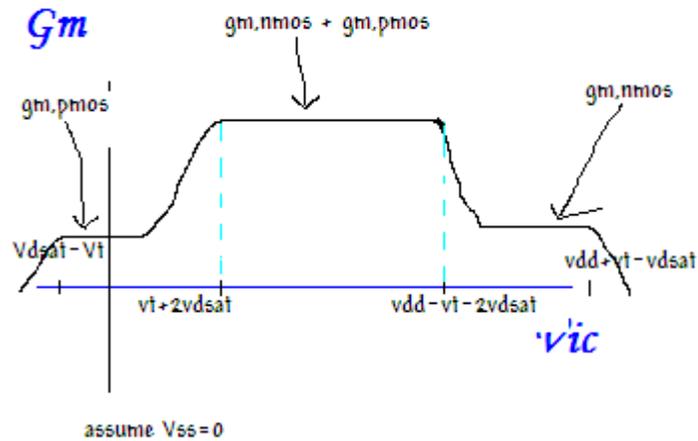
### RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA340 series extends 500mV beyond the supply rails. This is stated in the data sheet.

$$V_{ic,max} = v_{dd} + 0.5$$

$$V_{ic,min} = v_{dd} - 0.5$$

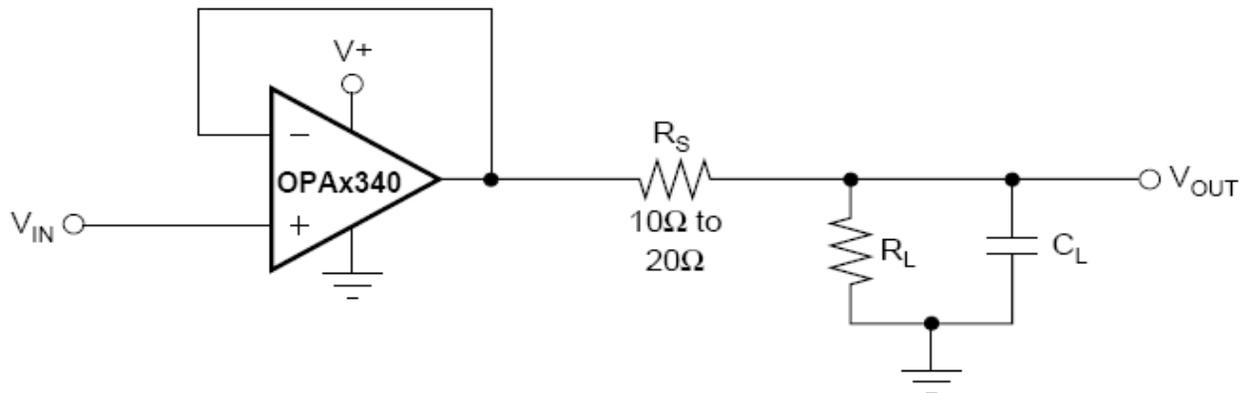
b.



c.

One method of improving capacitive load drive in the unity gain configuration is to insert a  $10\Omega$  to  $20\Omega$  resistor in series with the output, as shown in Figure 4. This significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, it creates a voltage divider introducing a dc error at the output and slightly reduces output swing. This error may be insignificant. For instance, with  $R_L = 10k\Omega$  and  $R_S = 20\Omega$ , there is only about a 0.2% error at the output.

Diagram for part c:



Problem 3.

0. Minimum allowable supply rail: (We look where there is the most transistors).

This could be the right side or the left side. But by observation, its possible to have all the transistors on the right side in saturation by leaving exactly  $V_{dsat}$  for each  $v_{ds}$ . This implies that  $V_{dd,min} = 4 V_{dsat} = 0.4$ . However, this will cause some of our transistors on the left side to go into triode.

Looking at the left side, the gate voltage of M4L is  $V_{gs4} = V_t + v_{dsat}$ .

This implies the drain voltage of M3L is  $V_t + V_{dsat}$  since a wire connects the gate of M4L to this node.

Looking up from the drain of M3L, we can bias our circuit such we leave exactly  $v_{dsat}$  across M2L and M5L. This implies the minimum  $V_{dd}$  required to bias all the transistors on the left side in saturation is equal to  $V_t + V_{dsat} + V_{dsat} + V_{dsat} = V_t + 3V_{dsat}$ .

Now we can double check that indeed we can bias all the other transistors in the circuit in saturation if we use  $V_{dd} = V_t + 3V_{dsat}$ .

How to design the supply independent biasing network:

If you are reading my solutions, you should look at the circuit diagram and try to follow along.

1. Pick currents for the folded cascode and decide on a  $v_{dsat}$ .

I pick  $200\mu A$ . For M5, and  $V_{bt5}$ ,  $100\mu A$  for transistors 1,2,3,4.

Reason:  $100\mu A$  seems like a good number to work with.

Pick  $V_{dsat} = 100mV$

Reason:  $g_m = \frac{2I_d}{V_{dsat}}$ , we want to use the smallest  $V_{dsat}$  to maximize  $g_m$ .

Also, since i will design my output range to swing within  $2V_{dsat}$  from each rail, if i make  $v_{dsat}$  small, it improves my swing at the output.

Since  $300mV$  within the rails is the spec, this implies  $2 V_{dsat} < 300mV$

or  $V_{dsat} < 150\text{mV}$  (for the transistors in the same branch as the output).

For my tail current source, M5T, i pick a  $v_{dsat}$  of  $200\text{mV}$ , it turns out it will be easier for me to bias it in this way.

2. Design the supply independent current source.

Sizing : MB1, MB2, MB3, MB4 , and RS

$$I_d = \frac{W}{2L} K_p (V_{dsat})^2 \quad , \text{ I neglect the } 1+\lambda \text{ because i plan to use large L values.}$$

To make calculations easier, i've decided to aim for  $200\mu\text{A}$  in the biasing network as well.

I plan to use the gate voltage of mb4 to bias the gate of m5. So i will set the  $v_{dsat}$  of MB4,  $MB3 = 100\text{mV}$ .

This implies  $(W/L)_4 = (W/L)_3 = 400$  ( $40000\mu\text{m}/100\mu\text{m}$ )

In order to make the current invariant from changes of  $v_{dd}$ . I pick  $L_3, L_4 = 100\mu\text{m}$ .

Formula given in Razavi :  $\frac{\delta I}{\delta V_{dd}} \propto \frac{1}{r_{o4}}$  , from Razavi (chapter 11)

bigger L --> bigger  $r_o$ . --> more stable current source.

For MB1, i pick a  $v_{dsat1} = 200\text{mV}$ , since its gate voltage will be used to bias VB5T.

$$I_d = \frac{W}{2L} K_n (V_{dsat})^2 \quad \text{---> } (W/L)_1 = 50. \text{ (} 500\mu\text{m}/10\mu\text{m)}$$

We also use a relatively large L value for  $(W/L)_1$  and  $(W/L)_2$  to reduce  $\lambda$  . This gives us a better current source.

Now, i choose  $(W/L)_2 = 4 (W/L)_1$  ( $2000\mu\text{m}/10\mu\text{m}$ )

=>  $V_{dsat2} = \frac{1}{2} V_{dsat1} = \frac{1}{2} * 200\text{mV} = 100\text{mV}$ .

To size Rs:

Do KCL, around the loop. I is picked to be  $200\mu\text{A}$ .

$$V_t + v_{dsat1} - (V_t + v_{dsat2}) - I R_s = 0$$

$$\Rightarrow 200\text{mV} - 100\text{mV} = I R_s$$

$$\Rightarrow R_s = 100\text{mV} / 200\mu\text{A} = 500 \text{ Ohms}$$

Spice results:

Supply independent current source:

volt      iref

2.00000    198.8411u

3.00000    200.8357u

4.00000    202.8120u

5.00000	204.7705u
6.00000	206.7114u
7.00000	208.6349u
8.00000	210.5412u
9.00000	212.4307u
10.00000	214.3036u
11.00000	216.1600u
12.00000	218.0004u
13.00000	219.8248u
14.00000	221.6335u
15.00000	223.4268u

3. Create the other biasing circuitry.  
Sizing MB5, MB6, MB7, MB8.

Once you have a stable reference voltage, there is some flexibility how you design the other parts of the biasing network.

First, lets use MB5 and MB6 to create V<sub>bcp</sub>.

We can size MB5 to be the same size as MB1. This gives us a steady 200uA reference current to work with.  $(W/L)_5 = (W/L)_1$  (500um / 10um)

Now the question is , how do we size MB6?

The purpose of sizing MB6 is to create a V<sub>bcp</sub> to bias our folded cascode in a high swing mode. If we bias it correct, V<sub>out</sub> will be able to go up within 2 V<sub>dsat</sub> of v<sub>dd</sub> while keeping all the transistors in saturation.

We also need to leave at least V<sub>dsat</sub> for the V<sub>ds</sub> of transistors M5l and M5r.

This means gate voltage of M2L and M2R needs to be set at V<sub>dd</sub>-V<sub>dsat</sub>-(V<sub>t</sub>+V<sub>dsat</sub>)

$$V_{bcp} = V_{dd} - V_t - 2V_{dsat}.$$

The V<sub>bcp</sub> is generated by MB6, and its equal to V<sub>dd</sub>- V<sub>t</sub>-V<sub>dsat6</sub>.

We see that we can get the appropriate voltage if we set V<sub>dsat6</sub> = 2 \* V<sub>dsat</sub> .

Where V<sub>dsat</sub> is the V<sub>dsat</sub> that i picked for transistors in the folded cascode. (100mV).

$$V_{dsat} = \sqrt{\left(\frac{2I}{K_p \frac{W}{L}}\right)}, \text{ Use this equation to calculate W/L ratios and Vdsats.}$$

By looking at this equation, we see that if we wanted to generate 2 V<sub>dsat</sub>, we should use  $(W/L)_6 = (1/4) * (W/L)_5_{\text{folded,cascode}}$ .

However there is a problem with the above scheme.

Problem: This biasing scheme biases the drain of M5L and M5R at almost exactly V<sub>dd</sub>-V<sub>dsat</sub>.

M5L and M5R are sitting on the edge between saturation and triode, and any disturbance could bring them into triode (such as raising the v<sub>dd</sub> to 15V) .

Solution: Bias the the gate of M2L and M2R at a slightly lower voltage.

Instead of using  $V_{dd} - V_t - 2\sqrt{2}V_{dsat}$  to bias  $V_{bcp}$ , we can set  $V_{bcp} = V_{dd} - V_t - 2\sqrt{2}V_{dsat}$ . I picked this value since if we set  $(W/L)_6 = 1/8 * (W/L)_5_{\text{folded,cascode}}$ , it sets  $V_{bcp}$  to the above expression. This sets the drain of M5 to  $V_{dd} - V_t - 2\sqrt{2}V_{dsat} + (V_t + V_{dsat}) \approx V_{dd} - 180\text{mV}$ . From the drain of M5, we have to get through another transistor to get to the output node, and since  $v_{dsat} \sim 100\text{mV}$ , it will allow our  $V_{out}$  to get up to  $V_{dd} - 300\text{mV}$  while all transistors are in saturation.

Sizing MB8 and MB7 is exactly the same method as sizing MB6 and MB5.

First, i sized MB8 by mirroring MB4, but using half of the current.

$$(W/L)_8 = \frac{1}{2} * (W/L)_4.$$

Reason: the transistors that i am trying to bias (nmos M3L, and M3R) are using 100uA.

Its slightly easier if currents are matched.

Now i sized MB7 to bias  $V_{bcn}$ .

$$V_{bcn} = V_t + 2\sqrt{2}V_{dsat}. \text{ The analysis is the same as above.}$$

This imple  $(W/L)_7 = 1/8 * (W/L)_3_{\text{folded,cascode}}$

This completes our biasing network.

#### 4. Size the transistors for the folded cascode :

I do not intend to post my transistor sizing for the folded cascode.

This is for your project =).

You maybe be able to figure out most of the W/L ratios just from the biasing structure I've used.

#### 5. Testing the Circuit.

Spice code :

\*HW7 Problem 3

.options nomod accurate=1 post

.op

.lib 'ee140\_model\_level1.lib' TT

.global vdd vss

vss vss 0 0

vdd vdd 0 2

.subckt my\_reference vbcp vbcn vb5 vb5t

xmb4 vb5t vb5 vdd vdd pmos w=40000u l=100u

xmb3 vb5 vb5 vdd vdd pmos w=40000u l=100u

xmb1 vb5t vb5t vss vss nmos w=500u l=10u

xmb2 vb5 vb5t s2 s2 nmos w=2000u l=10u

rs s2 vss 500

xmb5 vbcp vb5t vss vss nmos w=500u l=10u

xmb6 vbcp vbcp vdd vdd pmos w=50u l=1u

xmb8 vbcn vb5 vdd vdd pmos w=2000u l=10u

xmb7 vbcn vbcn vss vss nmos w=125u l=10u

```
.ends
```

```
.subckt start_up vb5t vb5  
xinvp gate vb5t vdd vdd pmos w=1u l=1000u  
xinvn gate vb5t vss vss nmos w=1000u l=1u  
xpulldown vb5 gate vss vss nmos w=1u l=1u  
.ends
```

```
.subckt folded_cascode vb5 vb5t vbcp vbcn vp vn out  
*sizing this amplifier will be your project =)  
xm1l dp vp middle middle nmos w=?? l=1u  
xm1r dn vn middle middle nmos w=?? l=1u  
xm5t middle vb5t vss vss nmos w=?? l=1u
```

```
xm5l dp vb5 vdd vdd pmos w=?? l=1u  
xm5r dn vb5 vdd vdd pmos w=?? l=1u  
xm2l d2 vbcp dp dp pmos w=?? l=1u  
xm2r out vbcp dn dn pmos w=?? l=1u  
xm3l d2 vbcn s3l s3l nmos w=?? l=1u  
xm3r out vbcn s3r s3r nmos w=?? l=1u  
xm4l s3l d2 vss vss nmos w=?? l=1u  
xm4r s3r d2 vss vss nmos w=?? l=1u  
.ends
```

```
xamp vb5 vb5t vbcp vbcn vp vn out folded_cascode  
xref vbcp vbcn vb5 vb5t my_reference  
xstart vb5t vb5 start_up
```

```
.param offset=offset_1_7 *use one of the values from below.
```

```
vic vn vss 1  
vid vp vn dc=offset ac=1
```

```
cl out 0 50pf
```

```
.param offset_1_7=0.0000786 * vdd =2 ,vout=1.7  
.param offset2_03= -0.000022 * vdd=2 vout=0.3  
.param offset15_03= -0.000008 * vdd=15 vout=0.3  
.param offset15_14_7=0.0003845 * vdd=15 vout=14.7
```

```
.tf v(out) vid
```

```
.ac dec 100 1 10g  
*.dc offset -0.000030 -0.000005 0.0000001  
*.print vout=par('v(out)')  
*.dc vdd 2 15 1
```

```
*.print id=par('id(xref.xmb1.m0)')
*.print vdsat2=par('vdsat(xref.xmb2.m0)')
*.print vdsat1=par('vdsat(xref.xmb1.m0)')
.end
```

Plots:

You should have 4 plots , one for each case:

Vdd=15V Vout=14.7

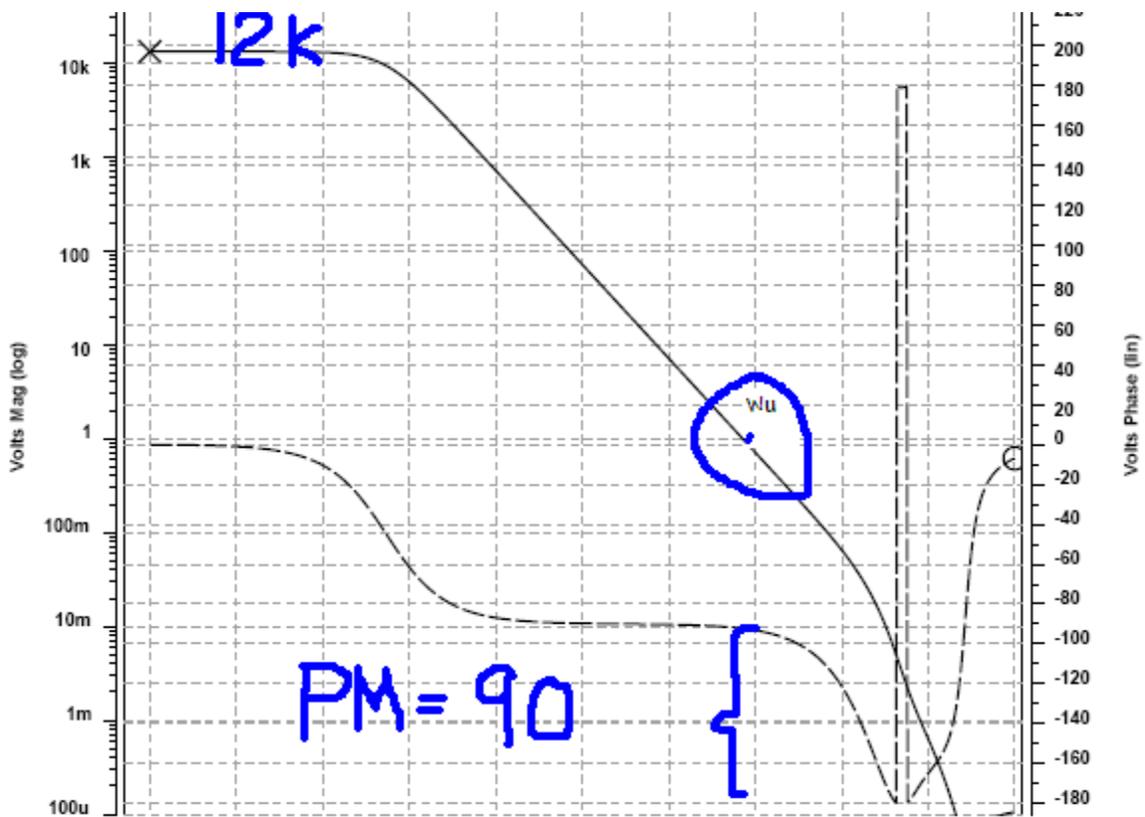
Vdd=15V Vout=0.3

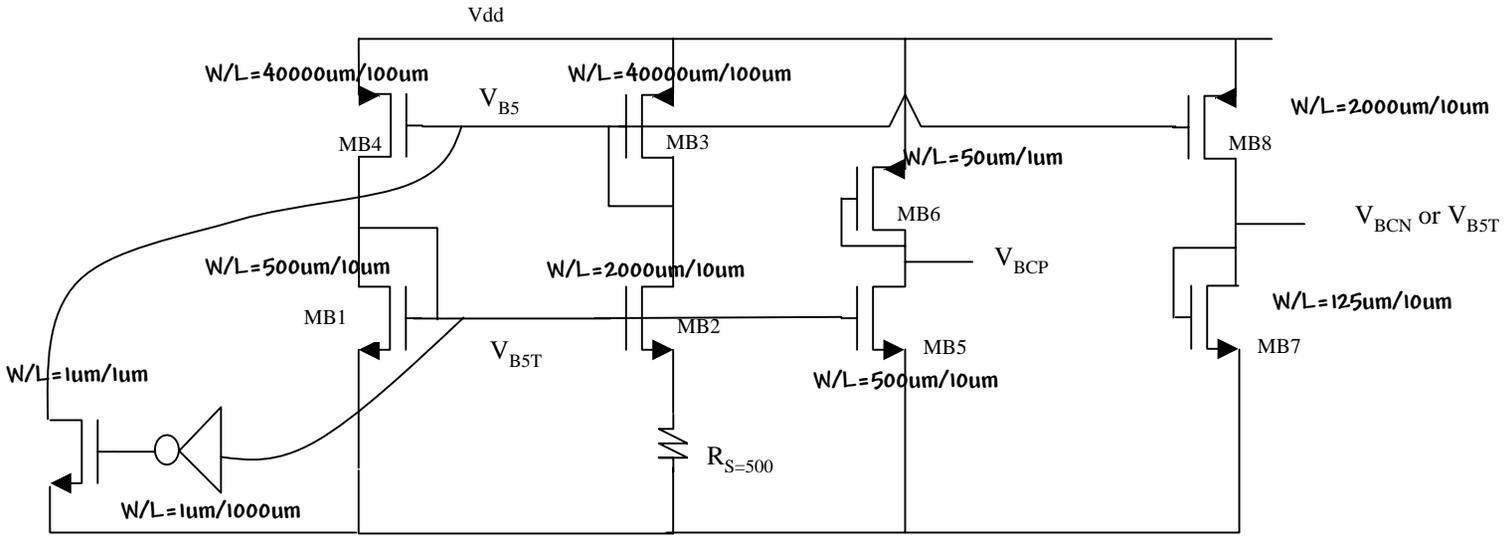
Vdd=2V Vout=1.7

Vdd=2V Vout=0.3

I will only provided this one since the other plots look similar.

Vdd=2V Vout=1.7





W/L=1000um/1um      W/L=1000um/1um  
**Startup circuit**  
 (avoid  $I_{b1}=I_{b2}=0$ )

**Supply independent**  
**Bias voltage generation**

**Folded cascode**

$$\begin{aligned}
 I_{d2L} &= I_{d5L} - I_{d1L} \\
 &= I_{d5L} - (I_{d5T}/2 + g_{m1} V_{id}/2) \\
 I_{d2R} &= I_{d5R} - I_{d1R} \\
 &= I_{d5R} - (I_{d5T}/2 - g_{m1} V_{id}/2)
 \end{aligned}$$

