

specs

$$\textcircled{1} a) I_{tail} = 200 \mu A \Rightarrow 200 \mu A = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{dsat3}^2$$
$$\left(\frac{W}{L}\right)_3 V_{dsat3}^2 = \frac{200 \mu A}{100 \frac{\mu m}{\mu m}} = 2 V^2$$

$$b) \text{Sink } 1 \text{ mA} \Rightarrow I_{d4} \geq 1 \text{ mA}$$

c) output swing to \pm in 200 mV of rails \Rightarrow

$$V_{dsat4} \leq 200 \text{ mV}$$

$$|V_{dsat5}| \leq 200 \text{ mV}$$

d) input CM to \pm in 200 mV of $V_{DD} \Rightarrow$

$$|V_{dsat2}| \leq 200 \text{ mV}$$

Step 1: current source design

pick all $L = 1 \mu m$ (L_6, L_3, L_4)

pick all $V_{dsats} \approx 140 \text{ mV}$ for $M3, M4, M6$

pick $I_{ref} = 100 \mu A$

(convenient factor of I_{tail}, I_{d4}
low impact on total current)

Calculate W_6

$$100 \mu A = \frac{200 \mu A}{2} \frac{W}{L}_6 (140 \text{ mV})^2$$

$$\frac{1}{2} V^2 = \left(\frac{W}{L}\right)_6 = 50$$

$$W_6 = 50 L_6 = 50 \mu m$$

calculate $W_3 = 2 W_6 = 100 \mu m$

calculate $W_4 \geq 10 W_6 \geq 500 \mu m$

pick $W_4 = \cancel{250} \mu m$ 600 μm

why? 1 mA sink min

play it safe. $I_{d4} = 1.2 \text{ mA}$

calculate $R = \frac{V_{DD} - (V_{in} + V_{dsat3})}{I_{ref}}$

pick $V_{DD} = 5V \Rightarrow R = \frac{4.36V}{100 \mu A} \approx 44K \Omega$

Step 2 Diff pair

M1a1 - pick $V_{dsat1} = 1V$, $L_1 = 0.5\mu m$
why? explore how small I can get from.

calculate $W_{1A} = W_{1B}$

$$\frac{I_{tail}}{2} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_{1A} V_{dsat1}^2$$

$$100\mu A = 100\frac{\mu A}{V^2} \left(\frac{W_{1A}}{0.5\mu m}\right) (1V)^2$$

$W_{1A} = 0.5\mu m$ violates process limits
($W_{min} = 1\mu m$)

try again: pick $V_{dsat1} = 0.5V$, $L_1 = 0.5\mu m$

calculate $W_{1A} = 2\mu m$

really low input capacitance

$$C_{gs1} = \left(\frac{5fF}{\mu m^2}\right) (1\mu m^2) \left(\frac{2}{3}\right) = 3.3fF$$
$$+ (0.5fF/\mu m) (2\mu m) + 1fF$$

$$= 4.3fF$$

$$C_{sd1} = 1fF$$

Step 3 Active load

pick $|V_{dsat2}| = 200mV$

$$L_2 = 2\mu m$$

why? L bigger, a little more gain

V_{dsat} as large as possible to ~~allow~~
minimize capacitive loading
(& maximize speed)

calculate

$$100\mu A = \frac{100\mu A/V^2}{2} \left(\frac{W}{L}\right)_2 V_{dsat2}^2$$

$$2V^2 = \left(\frac{W_2}{2\mu m}\right) (0.04V^2)$$

$$W_2 = 100\mu m$$

pick $W_2 = 120\mu m$

why? a little wider means

$|V_{dsat2}|$ will be a little less than
200mV, even w/ some process variation

top 4 calculate pick $V_{dsab5} = V_{dsab2}$

$$L_5 = L_2$$

why? make it easy to calculate size of M5, and make bias point less sensitive to process variation

calculate W_5 :

$$\left(\frac{W}{L}\right)_5 = \frac{I_{dc}}{I_{d2A}} = \frac{12}{1440} \Rightarrow W_5 = 12W_2 = 1440\mu\text{m}$$

layout only need 3 transistors:

$$\text{NMOS } \frac{W}{L} = \frac{50\mu\text{m}}{1\mu\text{m}}$$

M6: 1 copy

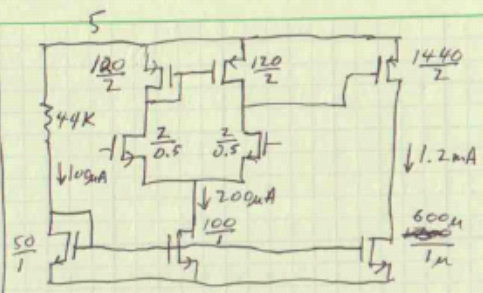
M3: 2 copies

M4: ~~2~~ copies

$$\text{NMOS } \frac{W}{L} = \frac{2\mu\text{m}}{0.5\mu\text{m}} \quad M1A, M1B$$

$$\text{PMOS } \frac{W}{L} = \frac{120\mu\text{m}}{2\mu\text{m}} \quad M2A, M2B \quad 1 \text{ copy each}$$

M5: 12 copies



$$\text{total gate area: } (WL)_5 = 2880\mu\text{m}^2$$

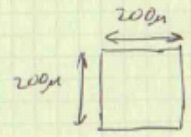
$$(WL)_6 = 600\mu\text{m}^2$$

$$2(WL)_2 = 480\mu\text{m}^2$$

$$\sim 4,000\mu\text{m}^2$$

$$\text{total layout area} \approx 10 \times \text{gate area}$$

$$\approx 40,000\mu\text{m}^2$$



total current 1.5mA

power 7.5mW

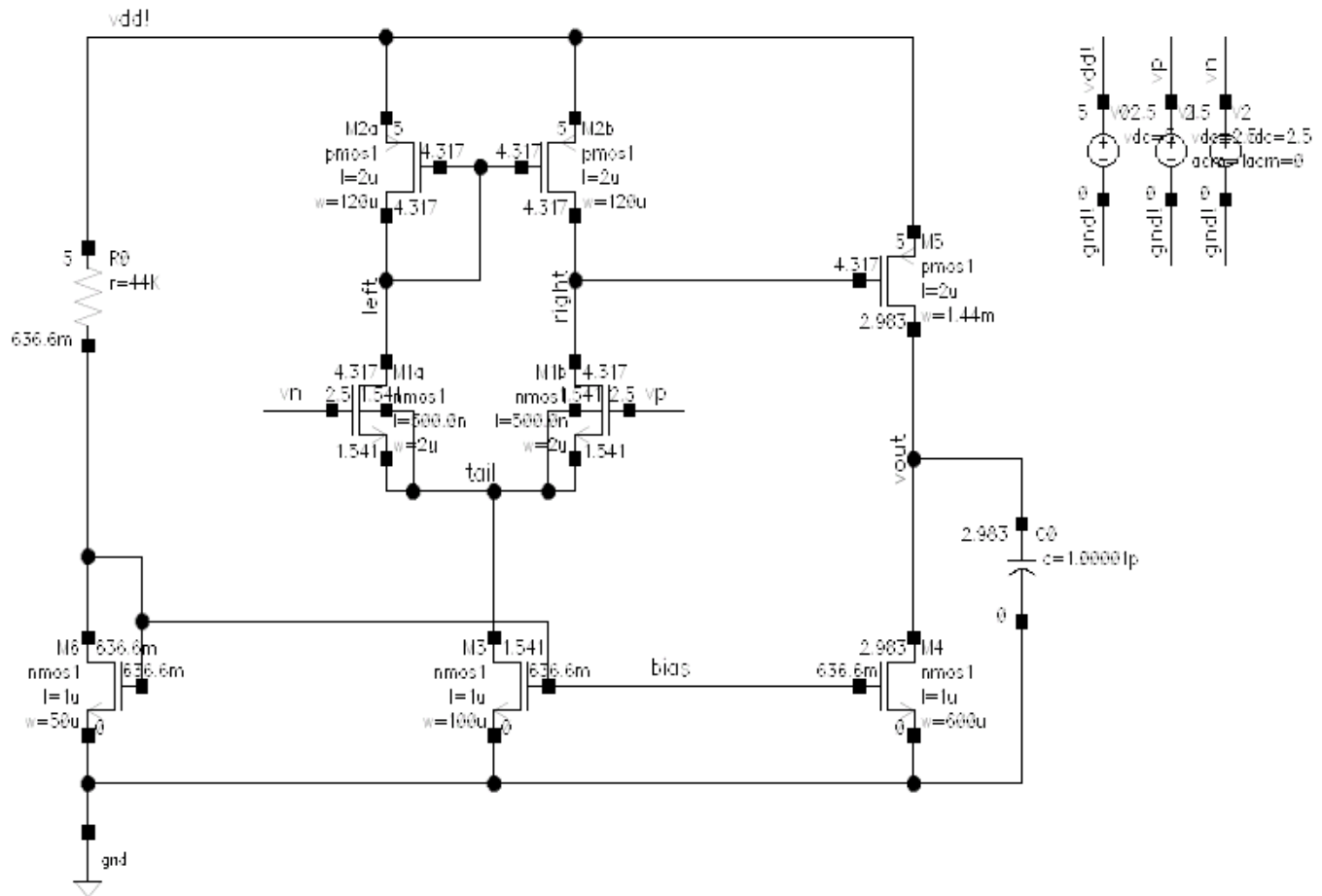


Fig.1. Schematic

[prob. 2]

(a) see Table 1

$$\begin{aligned}
 (b) \quad A_{v1} &= -g_{m1} \times (R_{o,1b} \parallel R_{o,2b}) \\
 &= -0.4 \text{ mS} \times (128 \text{ k}\Omega \parallel 107 \text{ k}\Omega) \\
 &= \underline{-23.31} \quad \text{vs. } 25.25 \text{ (SPICE)}
 \end{aligned}$$

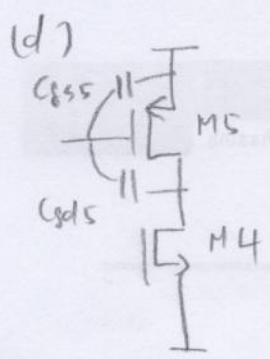
$$\begin{aligned}
 A_{v2} &= -g_{m5} \times (R_{o,4} \parallel R_{o,5}) \\
 &= -12 \text{ mS} \times (10.4 \text{ k}\Omega / 2) \\
 &= \underline{-62.4} \quad \text{vs. } 68.21 \text{ (SPICE)}
 \end{aligned}$$

$$A_{v,tot} = A_{v1} \times A_{v2} = \underline{1454.5} \quad \text{vs. } 1720.1 \text{ (SPICE)}$$

$$\begin{aligned}
 (c) \quad * \omega_{p1} &= [(R_{o,1b} \parallel R_{o,2b}) \times (C_{db1b} + C_{db2b} + (C_{gd,1b} + C_{gd,2b}) (1 - \frac{1}{A_{v1}})^0)]^{-1} \\
 &\approx [(128 \text{ k}\Omega \parallel 107 \text{ k}\Omega) \times (0.78 \text{ fF} + 78 \text{ fF} + 1 \text{ fF} + 60 \text{ fF})]^{-1} \\
 &= (58.28 \text{ k}\Omega \times 139.78 \text{ fF})^{-1} \\
 &= \underline{19.54 \text{ MHz}} \quad \text{vs. } 14.43 \text{ MHz (SPICE)}
 \end{aligned}$$

$$\begin{aligned}
 * \omega_{p2} &= [(R_{o,4} \parallel R_{o,5}) (C_{db4} + C_{db5} + (C_{gd4} + C_{gd5}) (1 - \frac{1}{A_{v2}})^0 + C_L)]^{-1} \\
 &\approx [5.2 \text{ k}\Omega \times (227.3 \text{ fF} + 642 \text{ fF} + 300 \text{ fF} + 720 \text{ fF} + 1000 \text{ fF})]^{-1} \\
 &= (5.2 \text{ k}\Omega \times 289 \text{ pF})^{-1} \\
 &= \underline{10.6 \text{ MHz}} \quad \text{vs. } 5.36 \text{ MHz (SPICE)}
 \end{aligned}$$

(The simulated ω_p 's are lower than the calculated values, because C_{gd} 's are millerized)



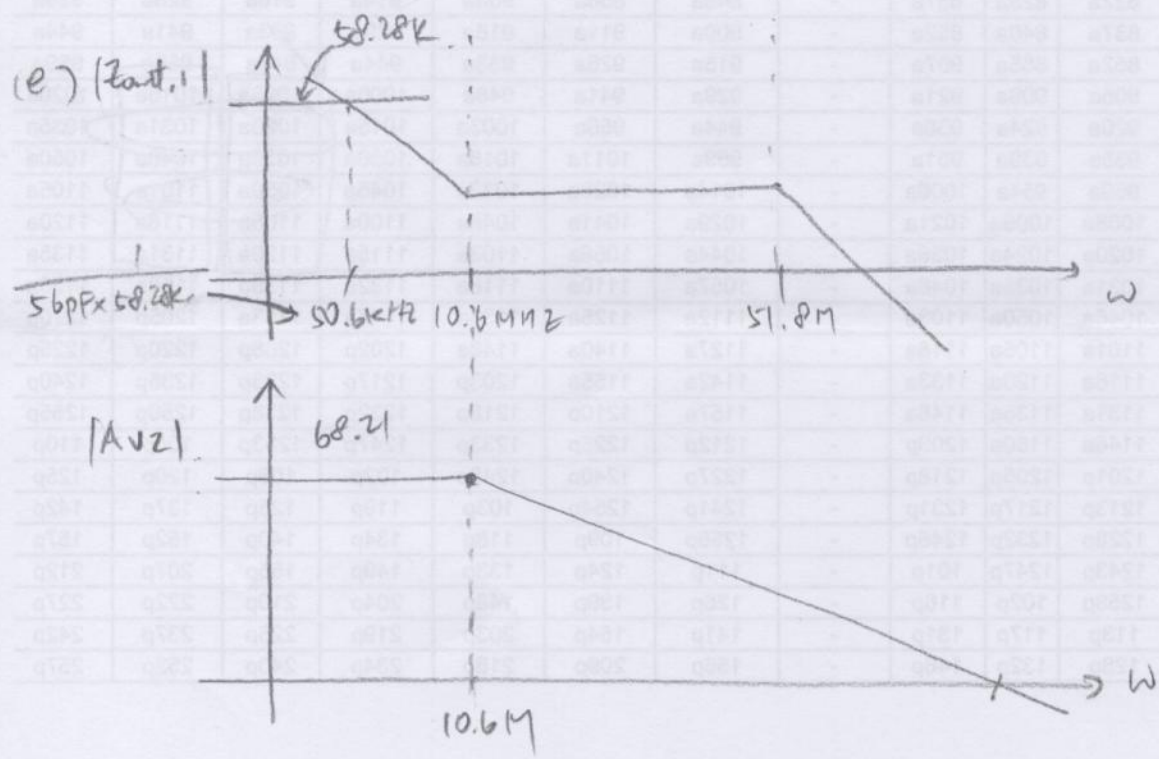
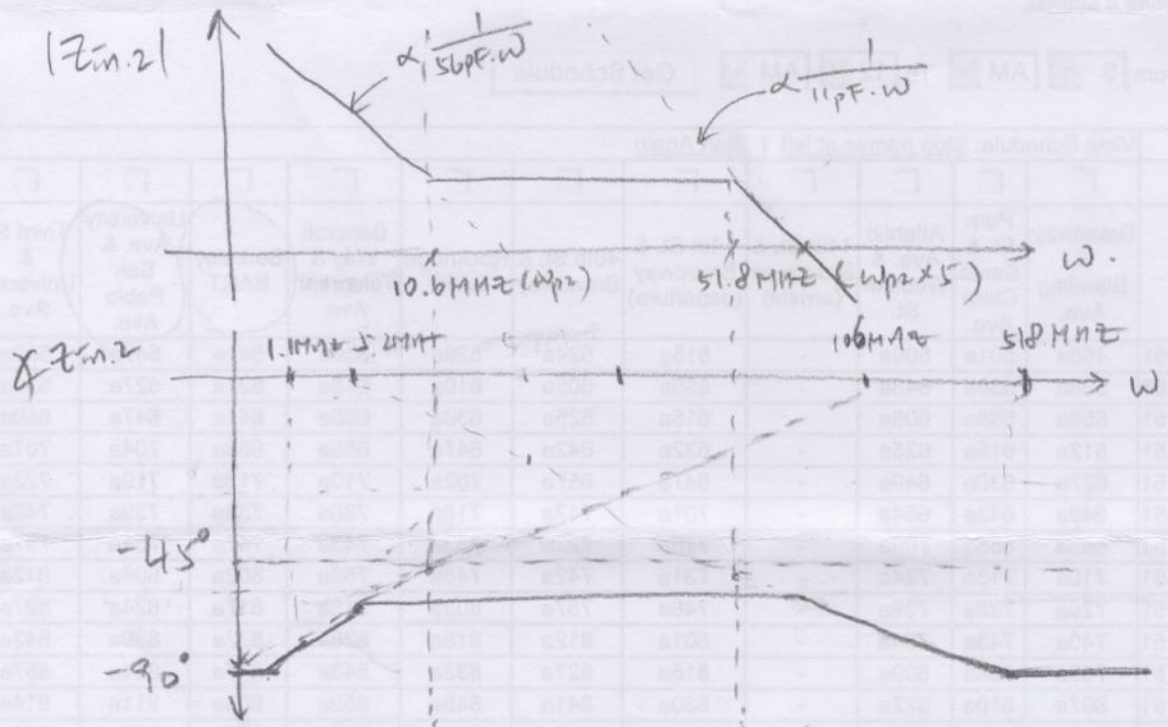
$$C_{in, \text{ low freq}} = C_{gs5} + (1 - A_{v_e}) \cdot C_{gd5}$$

$$= 10.32 \text{ pF} + (1 + 62.4) \cdot 720 \text{ fF}$$

$$\approx 56 \text{ pF}$$

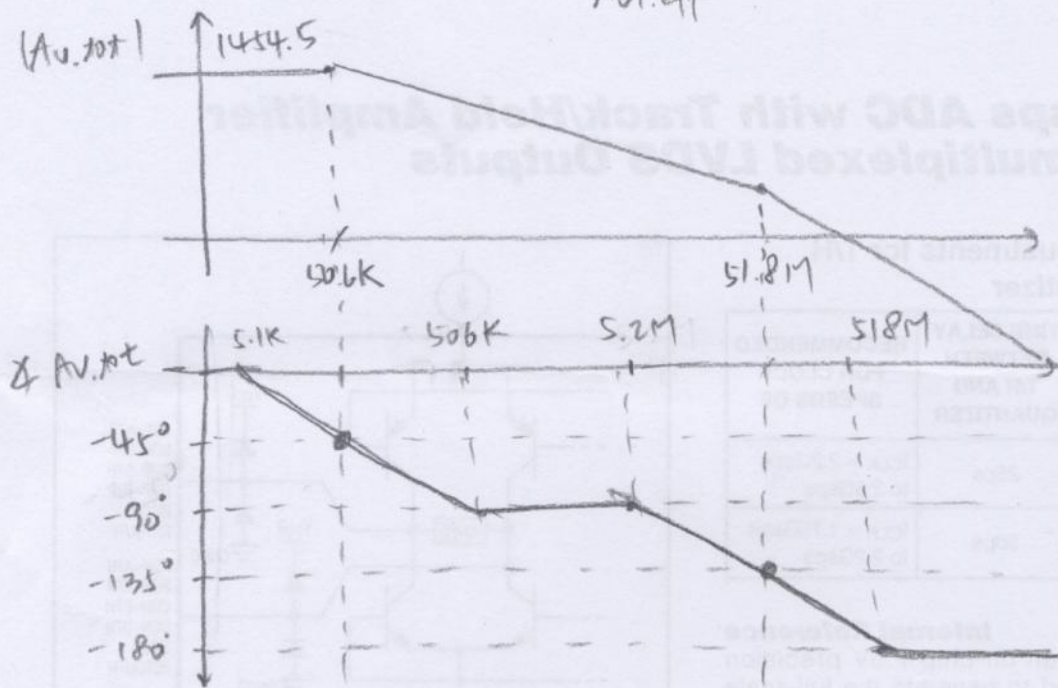
$$C_{in, \text{ high freq}} = C_{gs5} + C_{gd5}$$

$$\approx 11 \text{ pF} \quad (\times 5 \text{ difference})$$



The overall gain = $\frac{g_{m1} \times |Z_{out1}| \times A_{o2}}{A_{v1,eff}}$

#7



[prob. 3]

(a) The SPICE deck, DC analysis results, and comparisons are listed in list 1, 2, and table 1, respectively.

(b) The SPICE AC analysis results are shown in Fig 2. The second pole is slightly off. But overall, the hand calculation well predicts the simulation.

```

** design view name: schematic
.global vdd!

.ac dec 10 10.0 10e9
.op all 0

.param vtn=0.5
.param vtp=-0.5
.model nmos1 nmos vto='vtn'
+ tox=6.9nm kp=200u lambda=0.1 gamma=0.5 phi=0.6
+ capop=0 cgso=0.5n cgdo=0.5n pb=0.5 cj=1e-3
.model pmos1 pmos vto='vtp' tox=6.9nm kp=100u lambda=0.1 gamma=0.5 phi=0.6
+ capop=0 cgso=0.5n cgdo=0.5n pb=0.5 cj=1e-3

c0 vout 0 1.00001e-12
m1a left vn tail tail nmos1 l=500e-9 w=2e-6 ad=2e-12 as=2e-12
m1b right vp tail tail nmos1 l=500e-9 w=2e-6 ad=2e-12 as=2e-12
v2 vn 0 dc=2.5 ac 0
v0 vdd! 0 dc=5
v1 vp 0 dc=2.5 ac 1
r0 vdd! bias 44e3
m5 vout right vdd! vdd! pmos1 l=2e-6 w=1.44e-3 ad=1.44e-9 as=1.44e-9
m2b right left vdd! vdd! pmos1 l=2e-6 w=120e-6 ad=120e-12 as=120e-12
m2a left left vdd! vdd! pmos1 l=2e-6 w=120e-6 ad=120e-12 as=120e-12
m4 vout bias 0 0 nmos1 l=1e-6 w=600e-6 ad=600e-12 as=600e-12
m6 bias bias 0 0 nmos1 l=1e-6 w=50e-6 ad=50e-12 as=50e-12
m3 tail bias 0 0 nmos1 l=1e-6 w=100e-6 ad=100e-12 as=100e-12
.end

```

List. 1. Spice Deck

subckt	0:m1a	0:m1b	0:m2a	0:m2b	0:m3	0:m4	0:m5	0:m6
element	0:nmos1	0:nmos1	0:pmos1	0:pmos1	0:nmos1	0:nmos1	0:pmos1	0:nmos1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	1.076e-04	1.076e-04	-1.076e-04	-1.076e-04	2.152e-04	1.453e-03	-1.453e-03	9.917e-05
ibs	0.	0.	0.	0.	0.	0.	0.	0.
ibd	-2.776e-14	-2.776e-14	6.832e-15	6.832e-15	-1.541e-14	-2.983e-14	2.017e-14	-6.366e-15
vgs	9.589e-01	9.589e-01	-6.832e-01	-6.832e-01	6.366e-01	6.366e-01	-6.832e-01	6.366e-01
vds	2.775e+00	2.775e+00	-6.832e-01	-6.832e-01	1.541e+00	2.982e+00	-2.017e+00	6.366e-01
vbs	0.	0.	0.	0.	0.	0.	0.	0.
vth	5.000e-01	5.000e-01	-5.000e-01	-5.000e-01	5.000e-01	5.000e-01	-5.000e-01	5.000e-01
vdsat	4.589e-01	4.589e-01	-1.832e-01	-1.832e-01	1.366e-01	1.366e-01	-1.832e-01	1.366e-01
beta	1.022e-03	1.022e-03	6.410e-03	6.410e-03	2.308e-02	1.558e-01	8.653e-02	1.064e-02
gam eff	5.000e-01	5.000e-01	5.000e-01	5.000e-01	5.000e-01	5.000e-01	5.000e-01	5.000e-01
gm	4.690e-04	4.690e-04	1.175e-03	1.175e-03	3.152e-03	2.127e-02	1.585e-02	1.452e-03
gds	8.423e-06	8.423e-06	1.007e-05	1.007e-05	1.865e-05	1.119e-04	1.209e-04	9.323e-06
gmb	1.514e-04	1.514e-04	3.791e-04	3.791e-04	1.017e-03	6.866e-03	5.117e-03	4.688e-04
cdtot	1.781e-15	1.781e-15	1.380e-13	1.380e-13	9.949e-14	5.273e-13	1.362e-12	5.816e-14
cgtot	5.336e-15	5.336e-15	9.207e-13	9.207e-13	4.336e-13	2.602e-12	1.105e-11	2.168e-13
cstot	6.336e-15	6.336e-15	9.807e-13	9.807e-13	4.836e-13	2.902e-12	1.177e-11	2.418e-13
cbtot	2.781e-15	2.781e-15	1.980e-13	1.980e-13	1.495e-13	8.273e-13	2.082e-12	8.316e-14
cgs	4.336e-15	4.336e-15	8.607e-13	8.607e-13	3.836e-13	2.302e-12	1.033e-11	1.918e-13
cgd	1.000e-15	1.000e-15	6.000e-14	6.000e-14	5.000e-14	3.000e-13	7.200e-13	2.500e-14

List. 2. Spice DC Analysis Result

		Id (A)	Vdsat (V)	L (um)	lambda	Vds (V)	(1+lambda *Vds)(V)	gm (S)	W (um)	gds = 1/ro (S)	ro (ohms)	Vdb (V)	Cov (fF)	Cgd (fF)	Cdb (fF)	Cgs (fF)
M1a	Calc.	1.00E-04	0.5	0.5	0.1	2.8	1.28	4.00E-04	2	7.81E-06	1.28E+05	2.8	1.00	1.00	0.78	4.33
	SPICE	1.08E-04	0.46					4.69E-04		8.42E-06				1.00	0.78	4.34
	% error	-7.41	8.70					-14.71		-7.21				0.00	-0.15	-0.15
M1b	Calc.	1.00E-04	0.5	0.5	0.1	2.8	1.28	4.00E-04	2	7.81E-06	1.28E+05	2.8	1.00	1.00	0.78	4.33
	SPICE	1.08E-04	0.46					4.69E-04		8.42E-06				1.00	0.78	4.34
	% error	-7.41	8.70					-14.71		-7.21				0.00	-0.19	-0.15
M2a	Calc.	1.00E-04	0.2	2	0.1	0.7	1.07	1.00E-03	120	9.35E-06	1.07E+05	0.7	60.00	60.00	77.46	860.00
	SPICE	1.08E-04	0.18					1.18E-03		1.01E-05				60.00	78.00	861.00
	% error	-7.41	11.11					-15.25		-7.47				0.00	-0.69	-0.12
M2b	Calc.	1.00E-04	0.2	2	0.1	0.7	1.07	1.00E-03	120	9.35E-06	1.07E+05	0.7	60.00	60.00	77.46	860.00
	SPICE	1.08E-04	0.18					1.18E-03		1.01E-05				60.00	78.00	861.00
	% error	-7.41	11.11					-15.25		-7.47				0.00	-0.69	-0.12
M3	Calc.	2.00E-04	0.14	1	0.1	1.5	1.15	2.86E-03	100	1.74E-05	5.75E+04	1.5	50.00	50.00	50.00	383.33
	SPICE	2.15E-04	0.14					3.15E-03		1.87E-05				50.00	49.50	383.60
	% error	-6.98	0.00					-9.30		-7.00				0.00	1.01	-0.07
M4	Calc.	1.20E-03	0.14	1	0.1	2.5	1.25	1.71E-02	600	9.60E-05	1.04E+04	2.5	300.00	300.00	244.95	2300.00
	SPICE	1.45E-03	0.14					2.13E-02		1.12E-04				300.00	227.30	2302.00
	% error	-17.24	0.00					-19.52		-14.29				0.00	7.76	-0.09
M5	Calc.	1.20E-03	0.2	2	0.1	2.5	1.25	1.20E-02	1440	9.60E-05	1.04E+04	2.5	720.00	720.00	587.88	10320.00
	SPICE	1.45E-03	0.183					1.59E-02		1.21E-04				720.00	642.00	10330.00
	% error	-17.24	9.29					-24.53		-20.66				0.00	-8.43	-0.10
M6	Calc.	1.00E-04	0.14	1	0.1	0.6	1.064	1.43E-03	50	9.40E-06	1.06E+05	0.64	25.00	25.00	33.11	191.67
	SPICE	9.92E-05	0.137					1.45E-03		9.32E-06				25.00	33.14	191.80
	% error	0.81	2.19					-1.48		0.84				0.00	-0.08	-0.07

Table.1. Device Parameters

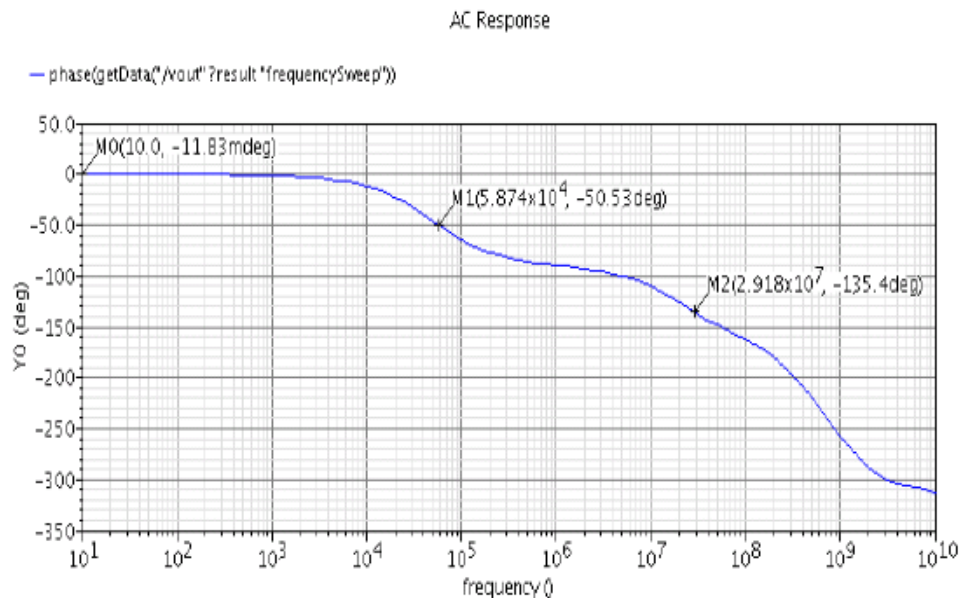
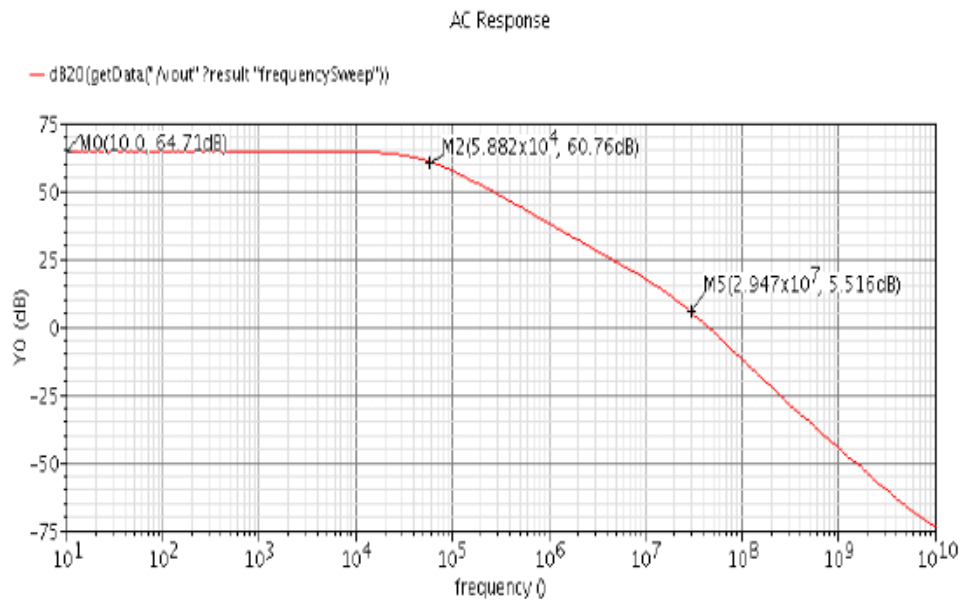
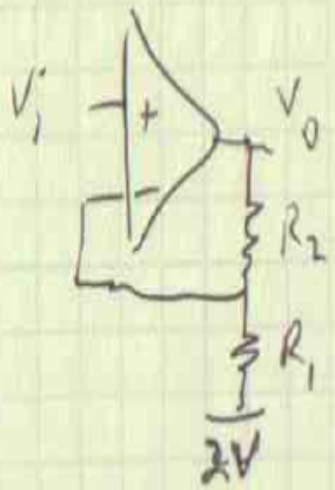
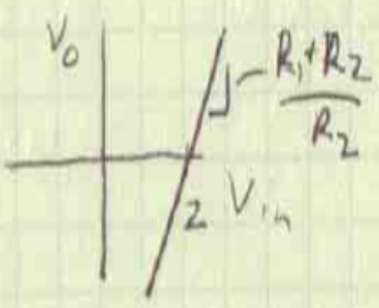


Fig.2. Spice AC Analysis Result



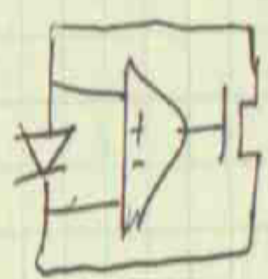
positive gain amplifier w/
input offset of 2V

$$V_o = \left(1 + \frac{R_1}{R_2}\right) (V_{in} - 2V)$$

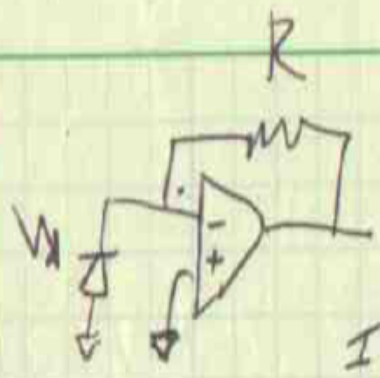


input range ~~is~~ smaller
than output swing

- need gain large compared to $\frac{R_2}{R_1+R_2}$
- need output resistance less than R_1+R_2

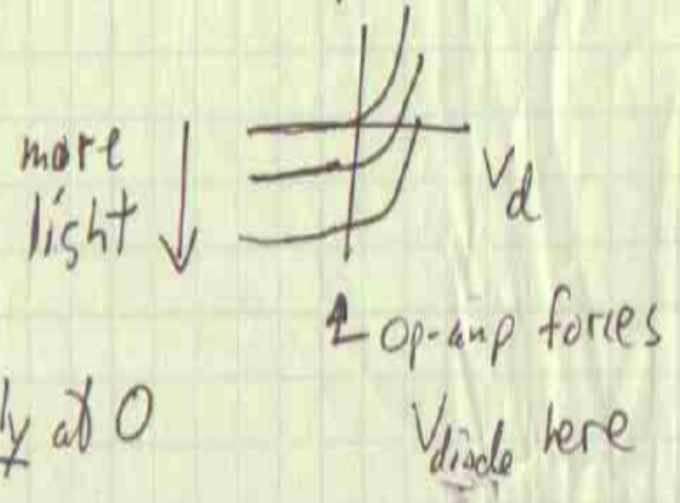


- super diode
- output can be very high impedance.
- output must be able to swing well above input CM, and probably a little below.

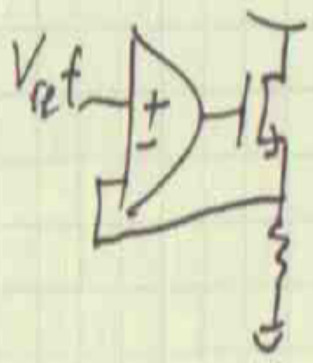


op-amp keeps $V_{diode} = 0$

IV curve for photodiode

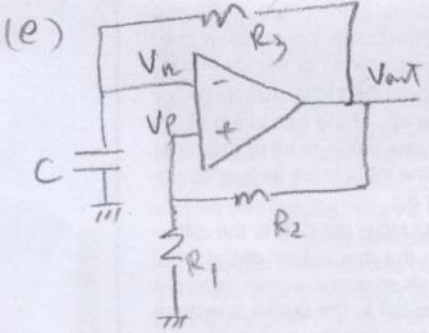


- input range only at 0
- output only positive
- need output resistance less than R



Voltage regulator

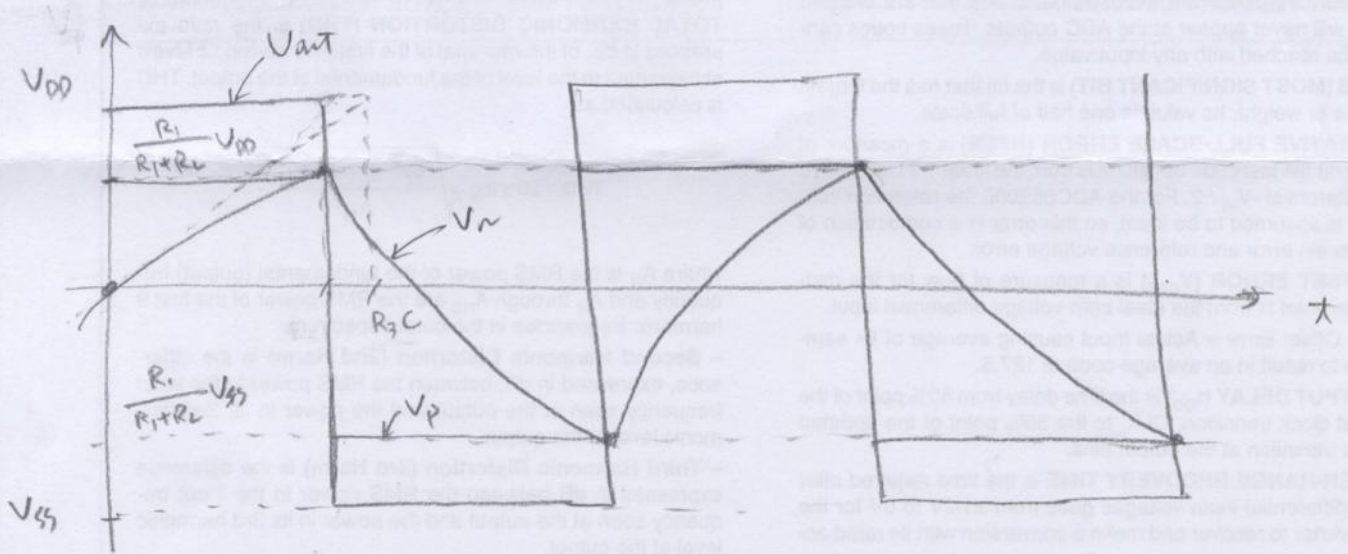
- input and output near top rail
- capacitive load - high Z OK



Assume that $V_{SS} \leq V_{out} \leq V_{DD}$,

$$V_n = 0 \text{ (} t=0 \text{)}, V_{out} = V_{DD} \text{ (} t=0 \text{)}$$

$$V_p = \frac{R_1}{R_1 + R_2} V_{out}$$



(Multi-vibrator)