EE140
Fall 2009
Project1
Due 10/26/09 8:00am

Here's the scenario: you're working as an analog design engineer at a high-tech startup. Your boss tells you that your first design project on the company's next-generation chip is a part of the sensor input path. The analog guru for the group has designed a system where all analog voltages are refered to Vref = 0.5V, with a single-sided 5V
supply. Your job is to design a digitally programmable variable-gain amplifier with resistive feedback.
The boss says don't try anything fancy: use a two-stage topology, or risk termination.
Here are the specs:
* 3 digital inputs (0 or 5V) to select gains of G=1, 2, and 4.
  Vo - Vref = G (Vi - Vref)
* valid input and output signals between 0.5 and 4V
* you are driving an 8-bit ADC which has a total input capacitance of 1pF
* at low frequency, your gain error must be less than one LSB equivalent for all gain settings
* at 10 Mrad/sec your gain error must be less than 10%
* phase margin must be at least 45 degrees for all gain settings

Someone else will be designing the reference current generator, so for now you can just use a resistor. Other than that resistor and your feedback resistor, all other circuit elements must be transistors or capacitors.

Both power and area are at a premium on this chip. Use your judgement on whether you optimize one or the other, or the product of the two.
For the area calculation, 10 * W*L + R * 0.1um2/Ohm + C * 0.2 um2/fF.

The analog team is doing a design review Monday morning, 8am, October 26. You need to email me your powerpoint before that meeting. The powerpoint needs to include a detailed description of your design process, as well as your circuit simulations to prove to everyone that you met every aspect the requirements.

Don't let the team down!

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