Golden Bear Circuits is working on its next exciting circuit product. This is a mixed-signal chip, with a microprocessor, flash and RAM memory, and a handful of analog inputs and outputs. You are a part of the three-person analog design team, and need to design all of the analog components for this chip. This includes:

- 8 bit successive-approximation analog to digital converter (ADC)
- programmable gain switched capacitor pre-amplifier (PGA)
- Bandgap voltage reference and Temperature sensor (BGT)
- Analog multiplexer (MUX)
- Analog and digital voltage regulators (REGs)
- The digital guys are handling the two Pulse Width Modulation (PWM) DACs.

All of the circuit blocks share a common ground. The microprocessor is the only block that runs off of $V_{DDD}$. All other blocks run off of either $V_{DDA}$ or $V_{BAT}$.

The product will be battery powered, so the circuits need to operate properly from as high as 3.7V (lithium thionyl chloride) down to 1.8V or less (two alkaline batteries at end of life). The product will be used in industrial environments, so all specs must be met over the range from -40 to +85 Centigrade.

**ADC**

The ADC must use an 8 bit successive approximation charge-redistribution topology. The digital output of the ADC taken as an integer between 0 and 255, times 1V/256, should be within 1 LSB of the analog input being sampled. In other words, each LSB should be just under 4mV. The digital SAR circuitry will be supplied to you by the digital team. We need to be able to take at least 100k samples/second.
PGA
The programmable gain amplifier must have a gain of all integers between 1 and 8 inclusive, implemented with switched capacitors. The gain error must be less than 0.4% for all gain settings. The gain setting is controlled by digital signals from the microprocessor.

Bandgap
The bandgap reference must be accurate to within 5mV after digital trim. Each LSB of a converted temperature measurement must correspond to 2 Kelvin, e.g. room temperature should give ADC readings of around 145 to 150.

MUX
The analog MUX must allow the microprocessor to select from one of 2 external analog inputs, as well as measure the battery voltage and the current temperature of the chip. The mux is controlled by digital signals from the microprocessor.

REGs
The regulators must take the battery voltage and deliver a clean supply to the analog and digital blocks. The digital block runs at 10MHz and pulls a peak current of 50mA, and its supply must stay within 10% of 1.5V. The digital circuits present a complex load which we model as a constant 1nF capacitance in parallel with a constant 10mA current and a periodic 40mA current. For example:
\[ \text{Jd}_{\text{d}} \text{d d} \text{d} 0 \text{ pulse (10m 50m 10n 10n 30n 100n) } \]
\[ \text{Cd}_{\text{igital} \text{d} d \text{d} 0 \text{ 1n} } \]
The analog blocks you design yourself, so you decide what they need. The DAC will pull up to 100uA from \( V_{BG} \), which should probably have a separate output buffer for the DAC.

Design restrictions
- Your circuit can contain as many MOSFETs and capacitors as you wish. MOSFET dimensions should be in multiples of 0.5um. The smallest MOSFET allowed is W/L=1u/0.5u. Capacitors used in any feedback network must have an integer ratio (e.g. C1=C2, or C1=16*C2). For example, C1=15.8*C2 is explicitly not allowed.
- Your circuit may contain resistors.
- The minimum sized capacitor that can be made reliably is 20fF.
- We’re using an NWELL CMOS process for this run, so all NMOS devices share a common bulk terminal. Device parameters are given in the process handout that you’ve used before.

This is a group project. Your team of three will all be evaluated together. I want to meet with the entire team at least twice before you’re done with the project. In the first meeting, I’d like you to present your planned schedule and division of labor: who will do what by when. You should have a block diagram of the project, with some detail on what kinds of amplifiers and other circuits will be needed in each block. You will also need to give me a list of how responsibility will be divided among each of you for each of the five components of the project. Everyone on the team must have at least 10% responsibility for every component. Your end-of-the-year bonus will depend on how
your parts of the project turn out (think of it like a grade!). If you would like to propose how your bonus should be calculated, in terms of how much credit you get for meeting performance and schedule milestones, this is the meeting in which to do so.

In the second meeting, I’d like to have a design review where you present your preliminary results. These should be fairly complete implementations of all of the blocks using semi-ideal amplifiers and switches.

I’m happy to have more meetings, but I’d like to have the entire team present for any meeting that we have.

You are encouraged to discuss your ideas with other project groups, and help each other with your designs, but there are limits. **Do** help each other debug SPICE problems, but **Don’t** share SPICE decks. **Do** brainstorm on topologies, calculations, and design ideas, but **Don’t** jointly agree on what all the saturation voltages, drain currents, and W/L values should be. Designers from Red Farm ICs are always lurking around trying to steal our designs!

Early turn-in bonus: 10% extra credit if turned in by Monday 12/7/05 at 8AM.

References
http://en.wikipedia.org/wiki/Switched_capacitor

Common Acronyms
ADC Analog to Digital Converter
DAC Digital to Analog Converter
LSB Least Significant Bit
PGA Programmable Gain Amplifier
PTAT Proportional to Absolute Temperature
PWM Pulse Width Modulation
SAR Successive Approximation Register