Homework 9

Due: Friday Nov. 21, 2014 at 1pm in the EE 140/240A Homework Box

1. Consider the class AB output stage depicted in Fig. PS9.1. Assume that the DC value of the input signal has been adjusted such that the output DC voltage is set at zero and the circuit is in the steady state with $v_{in}\,sin(2\pi f_0 t)$ *as* the input signal and $v_m\,sin(2\pi f_0 t)$ as the output signal.

(a) Find R_1 such that there is no dead zone in the transfer characteristics.

(b) Find the maximum value of v_m for $R_L = 100\Omega$, such that there is no clipping in the output waveform.

(c) Find the maximum output power delivered to 100Ω load and calculate the efficiency of the output stage (include all the elements).

(d) Find the maximum average power dissipated in transistors Q_1 and Q_2.

BJT parameters:

$V_{BE\,(on)} = 0.7\text{V}$, $\beta_{1,\,2} = 20$, $\beta_{3\text{-}8} = 100$, $V_A = 50\text{V}$, $V_{CE\,(sat)} = 0.2\text{V}$, $V_{CC} = 10\text{V}$,

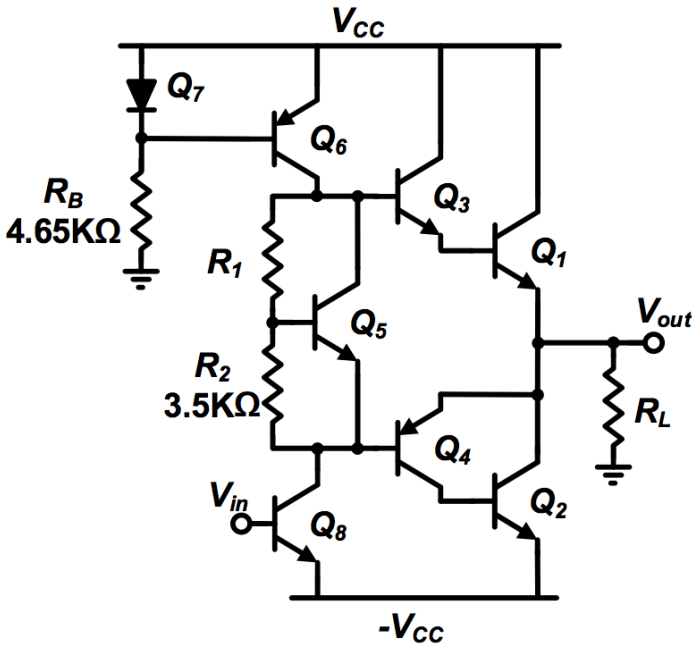

Fig. PS9.1

2. An amplifier has a low-frequency gain of 10,000, and its transfer function has three poles at 50kHz, 100MHz, and 900MHz

a. If this amplifier is connected in a feedback loop with a constant feedback factor β, resulting in a low-frequency gain $A_0 = 20$, estimate the phase margin and sketch the amplifier's frequency response in terms of both magnitude and phase.

b. Repeat (a) if $A_0 = 2$.

c. Find the maximum amplitude due to frequency peaking for both (a) and (b).

3. The op-amp in the circuit of Fig. PS9.2 has an open-loop gain of 10,000 and a single-pole roll-off with cut-off frequency $\omega_{3dB} = 10$ rad/s.

a. Sketch magnitude and phase Bode plots of the loop transmission.

b. Find the frequency at which the loop gain = 1, and find the corresponding phase margin.

c. Find the closed-loop transfer function and calculate its zeros and poles. Sketch a pole-zero plot. Sketch magnitude and phase Bode plots of the closed-loop circuit and label the important parameters on your sketch, e.g. low frequency gain, pole frequency, overshoot height.

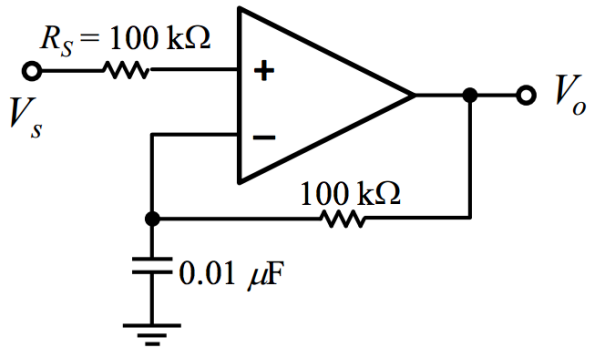

Fig. PS9.2

4. In the amplifier shown in Fig. PS9.3 transistors M_3-M_8 are biased with V_{ov}=200mV. Gates of M_3 and M_4 are biased to allow maximum undistorted sinusoidal signal at the output. Calculate all currents, channel widths and the value of capacitor C_c so that the amplifier has DC gain of 20, phase margin of 60 degrees for unity gain feedback, and the unity gain frequency of 50MHz. All transistors have the same channel length. Neglect all parasitic capacitances in this problem.

$V_{DD} = 3V,\ R_L = 10k\Omega,\ C_L = 5pF$

$V_{th0,n} = 0.5V,\ \mu_n C_{ox} = 250\dfrac{\mu A}{V^2},\ L = 0.5\mu m,\ \lambda = 0,\ \ \gamma = 0,\ L_d = 0$

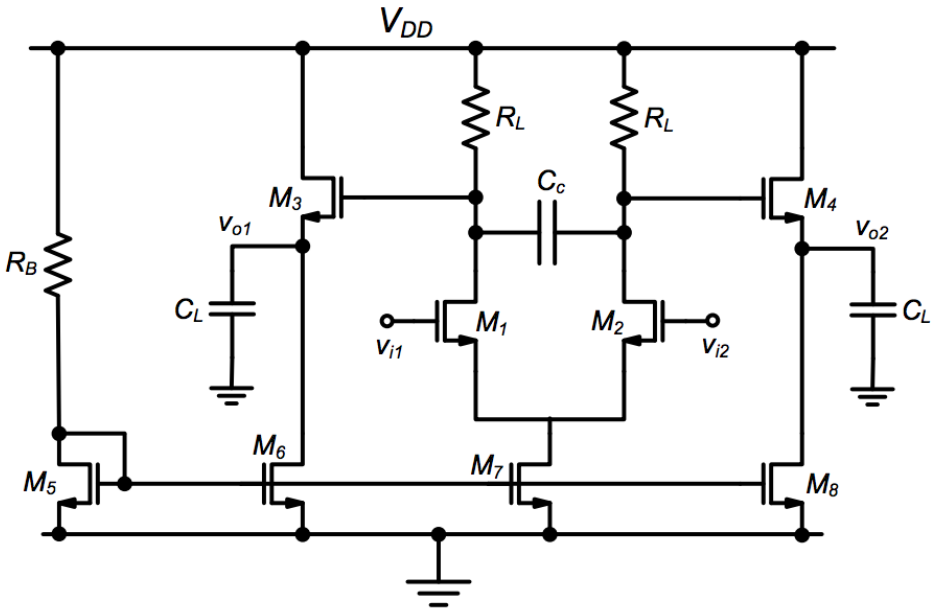

Fig. PS9.3