CMOS Operational Amplifier Design Problem

Issued: Monday, October 27, 2014
Report Due: Friday, Dec. 12, 2014

CMOS operational amplifiers have become an integral part of many integrated circuit chips fabricated today in a number of application areas. These amplifiers offer advantages in terms of power dissipation, die area, and compatibility with digital circuits when compared with their bipolar counterparts. Therefore, it is important that EE 140/240A students have an in-depth understanding of the tradeoffs and issues involved in their design. This understanding is best acquired by actually designing an op amp from beginning to end.

Thus, in this lab you are asked to design and simulate a CMOS operational amplifier that can satisfy the set of specifications given. You do not need to create a layout for the amplifier. However, you may have to perform some analysis in order to estimate the source/drain areas and perimeters of the transistors to calculate parasitic junction capacitances. Make sure to follow the guidelines listed below:

1- You are to work on this design project individually. Although you can discuss generalities with other students in the class, you are not to perform the design in teams or groups. The chances of any two people coming up with the same exact design are very slim. Therefore, we expect to see different designs from each one of you.

2- You are not required to do a layout for this amplifier. However, you do need to make sure that you take into account all the important layout effects and parameters. In particular, all the parasitic capacitances from pn junctions should be included. This means that you need to specify the areas and relevant perimeters of the drain and source for each transistor. Note that your *SPICE* device models automatically compute source/drain areas and perimeters, so you need not include them specifically in your *SPICE* netlist. However, you do need to compute source/drain areas and perimeters and account for them in your hand analysis.

3- You are not necessarily supposed to use any design tool other than *SPICE*. You can use any version of *SPICE* you like, so long as we have access to your *SPICE* code. Be aware, however, that *HSPICE* is preferred.

4- Assume that design is done in a 130 nm CMOS process technology. We'll mark this dimension as 2λ. This means that every dimension used must be a multiple of $\lambda = 65$ nm, and that the minimum feature size in this technology is $2\lambda = 130$ nm. In other words, the minimum drawn gate length is 130 nm. In addition, the lengths of the transistor drains and sources are $5\lambda = 325$ nm. Use this information to determine drain and source areas and perimeters for your calculations. Note that you do not need to perform a detailed layout; a realistic estimation of areas and relevant perimeters is sufficient. ***It is suggested that you use a minimum width of $3\lambda = 195$ nm for the transistors in your circuit. This will minimize circuit performance variations due to integrated circuit fabrication process variations.***

5- Although you can use a resistor in your V_{BIAS}-generator (but not an excessively large one), do not use physical resistors in your op amp. If you need a resistor, use an MOS device biased in the triode region as a resistor.

6- Your design approach should be outlined in your final report on this project. It is suggested that you use the following approach:
   a- Start with a circuit topology and perform hand calculations to come up with the estimates of the various parameters;
   b- Confirm the operation of the circuit using *SPICE*;
   c- Include all parasitics and important layout characteristics and redo simulations;
   d- Iterate design and re-simulate until all specs are met;
   e- Write your report.

Final report (due Dec. 12, 2014)

Your final report should be concise and complete. The report should be typewritten, and should be divided into the following sections (with page limits strictly observed using 12pt font sizes and reasonably-sized figures):

Overview (1-2 pages):
Complete schematic and basic description of circuit operation (including biasing). Your schematic should include device sizes next to each transistor. This section should not contain design discussion.

Design (1-3 pages):
A brief discussion of your design approach, specifically identifying important constraints. Note that you may have to provide some basic and important equations used in your design.

Transistor and Bias Summary (1 page):
A table listing for each transistor, the dimensions, drain bias current, the magnitude of the gate-to-source voltage, the transconductance, and the output conductance;

Performance (1 page):
A table comparing the simulated performance of your design with the design objectives. This table should be as complete as possible and should include all the op-amp performance specifications.

Discussion (<10 pages, plus figures):
A discussion of circuit performance with special attention paid to unique areas in your design which helped/hurt your attempts to meet the specifications. This is the most important section, in that it provides the validation for your design. Each of the performance specifications listed below should be validated in a subsection. You may want to include a diagram of the circuit you used, the justification for its use, and the simulation results or output data showing that it has met the needed specifications. Note that you should show simulation results for all the specifications. For each, select an appropriate circuit topology (i.e., input sources, current measuring sources, etc.) for measurement.

Conclusion (1 page):
A summary of your design experience. You should summarize the overall op amp characteristics, and should describe your overall experience and what you learned in doing this design. It would be good to get some feedback from you, both good and bad. Tell me if the design problem was worth the effort. (Your comments here will not adversely affect your grade.)

You should try your best to achieve the following design specifications. If after all attempts you fail to meet all the design specifications, describe your optimum and final design and describe in your report what you consider to have been the most restrictive and problematic spec to meet. Also discuss how that particular spec could be improved; i.e., discuss tradeoffs between various parameters, etc. Your report should indicate that you have tried many different techniques and have not been able to achieve any particular specification. Note that normally many students do a decent job in the design of the op-amp. Therefore, the quality of the report, both in terms of technical contents and presentation, will be very important in determining your final project grade. The grade sheet to be used for grading the reports is provided at the end of this document so you can see how the project grade is distributed.

If you are able to design the following op-amp, satisfying all specifications, then make sure that your report describes your overall design approach and procedure.

The design specifications for the CMOS operational amplifier are given below:

Parameter	*Specification*
Lmin	130 nm
Wmin	195 nm

DC Gain	≥1500 V/V
Common-Mode Input Range	0.5V (inside the output swing range)
Output Swing	Within 0.15 V of each supply **(Note: $\|V_{ov}\| > 0.10$ for ALL Devices)**
Power Dissipation (includes Biasing)	Minimize (less than 2 mW)
Unity Gain Frequency	≥100 MHz
Settling Time for Unity Gain Buffer (±0.4 V Input Step)	≤5 nsec to 0.1% for both rising and falling inputs
CMRR at DC	≥75 dB
PSRR	≥60 dB at DC ≥50 dB at 1 MHz
Load Capacitance	5 pF
Supply Voltage	$V_{DD} = 1.2$ V, $V_{SS} = 0$ V

The following device parameters are to be used in your circuit simulation:

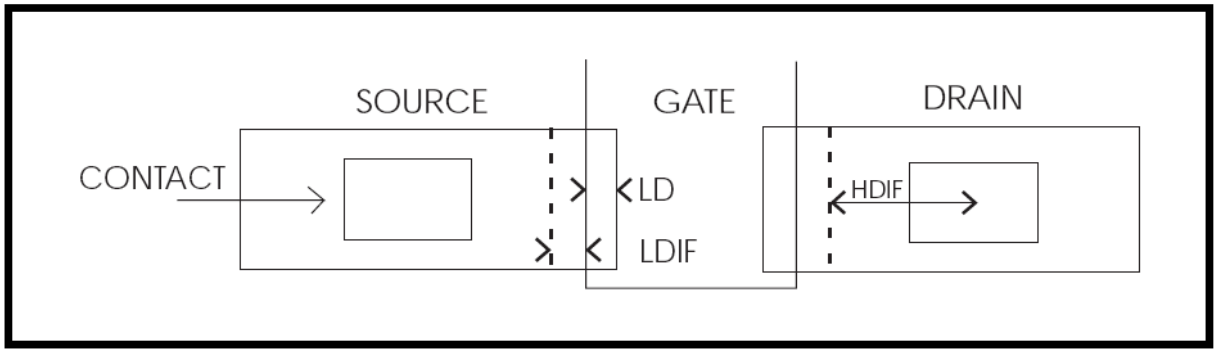
SPICE PARAMETERS FOR USE WITH OP-AMP DESIGN AND SIMULATION

Parameter	*NMOS*	*PMOS*
Level	2	2
VTO	0.3 V	-0.3 V
U0	250 cm^2/Vs	100 cm^2/Vs
GAMMA	0.2 $\sqrt{V}$	0.2 $\sqrt{V}$
LAMBDA (@ L=130nm)	0.2 V^{-1}	0.15 V^{-1}
TOX	2.6 nm	2.6 nm
LD	0.025 μm	0.025 μm
LDIFF	65 nm	65 nm
HDIFF	130 nm	130 nm
PHI (=2ϕ)	0.6 V	0.6 V
CJ	800 $\mu F/m^2$	800 $\mu F/m^2$
MJ	0.5	0.5
CJSW	8 pF/m	8 pF/m
MJSW	0.5	0.5
CJGATE	80 pF/m	80 pF/m

You will be provided with the model file. The device models are encapsulated in a sub-circuit in order to automatically account for the channel length modulation effect. You must use the prefix 'x' instead of 'm' when instantiating a device. For example:

```
x1 d g s b nmos w=1u l=130n
x2 d g s b pmos w=1u l=130n
```

The meanings of the parameters HDIFF and LDIFF are illustrated in the figure below. CJGATE is the zero-bias gate-edge sidewall bulk junction capacitance.



The following grading scheme will be used to grade the design project reports. Note that you should make sure that all the components that were mentioned above are included in your report even though they are not specifically mentioned in the table below. Write the best report you can because the distribution is typically very tight on the project reports and a few points can make all the difference.

Evaluation of
Reports On CMOS Op-Amp Design Project

	Maximum	Your Grade
Report Preparation and Presentation		
Overview	5	
Design Summary	5	
Discussion	15	
Conclusions	5	
Overall Presentation	10	
Design Techniques and Results		
Hand Design	10	
Simulation Results and Techniques	20	
Design Issues and Tradeoffs	10	
Achievement of Specs	15	
Minimization of Power Consumption	10	
Overall Effort	5	
TOTAL	***110***	

Note from the table that power consumption should be less than 2 mW, but should also be minimized. In other words, the lower the power consumption, the higher the grade for this part. For team projects, only the specifications of the best of the two designs will be used in determining competitive performance metrics.