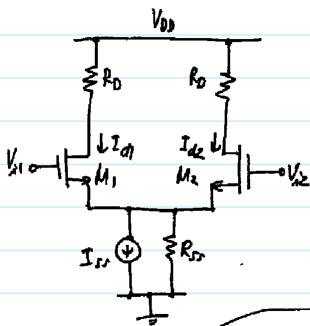
EE 140 | MOS Source-Coupled Pair | CTN | 10

MOSFET Source-Coupled Pair



Assume: M_1 & M_2 are identical.

Find $\Delta I_d = I_{d1} - I_{d2} = f(V_{id})$.

$\Rightarrow$ approach: get $V_{id} = f(\Delta I_d)$ $\rightarrow$ then invert to get $\Delta I_d = f(V_{id})$

$$I_{d1} = \underbrace{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1}_{k}(V_{gs1} - V_t)^2 \Rightarrow V_{gs1} = V_t + \sqrt{\frac{2I_{d1}}{k}}$$

$$\therefore V_{id} = V_{gs1} - V_{gs2} = \sqrt{\frac{2I_{d1}}{k}} - \sqrt{\frac{2I_{d2}}{k}}$$

Define. $\left.\begin{array}{l}\Delta I_d = I_{d1} - I_{d2} \\ I_d = \dfrac{I_{d1} + I_{d2}}{2}\end{array}\right\}$ $\begin{array}{l} I_{d1} = I_d + \dfrac{\Delta I_d}{2} \\ I_{d2} = I_d - \dfrac{\Delta I_d}{2}\end{array}$

$$V_{id} = \sqrt{\frac{2\left(I_d + \frac{\Delta I_d}{2}\right)}{k}} - \sqrt{\frac{2\left(I_d - \frac{\Delta I_d}{2}\right)}{k}} \Rightarrow \frac{k}{2}V_{id}^2 = I_d + \frac{\Delta I_d}{2} - 2\sqrt{I_d^2 - \left(\frac{\Delta I_d}{2}\right)^2} + I_d - \frac{\Delta I_d}{2}$$

$$\frac{k}{2}V_{id}^2 = 2I_d - 2\sqrt{I_d^2 - \left(\frac{\Delta I_d}{2}\right)^2}$$

$\Rightarrow$ now rearrange to get ΔI_d (algebra)

Solve for ΔI_d:

$$\Delta I_d = \frac{k}{2}V_{id}\left(\frac{2I_{SS}}{k/2} - V_{id}^2\right)^{1/2} = \boxed{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{id}\sqrt{\left(\frac{2I_{SS}}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}\right) - V_{id}^2} = \Delta I_d}$$

Large Signal Equation for Differential Output Current

Valid so long as the devices stay saturated:

$$|V_{id}| \le \sqrt{\frac{2I_{SS}}{k}} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} = \sqrt{2}\,(V_{GS} - V_t)$$

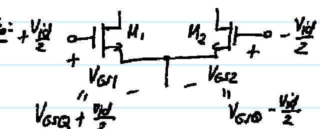
(V_{GS} for $I_D = \frac{I_{SS}}{2}$)

if true then input devices are both saturated

Thus, to extend the linear input range:

1. $I_{SS}\uparrow \rightarrow (V_{GS} - V_t)\uparrow$
2. $W\downarrow$
3. $L\uparrow$

To derive this:



When $\frac{V_{id}}{2} \ge V_{GSQ} - V_t = \Delta V$ then M_2 will cut-off

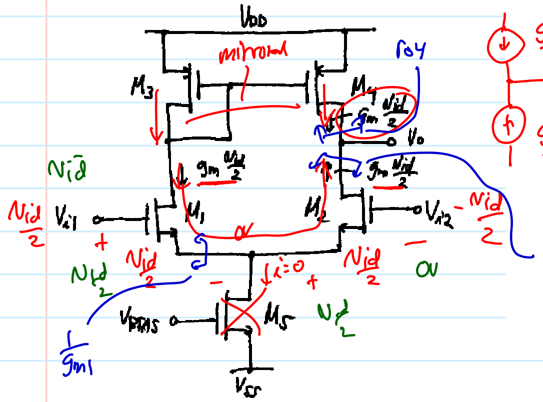
$\therefore V_{id} \le 2(V_{GSQ} - V_t) \rightarrow$ to maintain saturation

$$V_{GSQ} - V_t = \sqrt{\frac{2I_{d2}}{\mu_n C_{ox}\frac{W}{L}}} = \sqrt{\frac{2\left(I_d - \frac{\Delta I_d}{2}\right)}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} = \frac{V_{id}}{2}$$

then plug in ΔI_d & solve for V_{id}

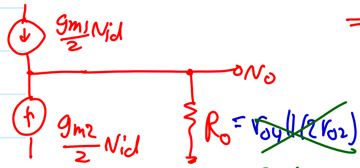
EE 140 | **Diff. Pair w/ Current Mirror Load** | CTN | 11

MOS Differential Stage w/ Current Mirror Load



$v_o = \left(\frac{g_m}{2}v_{id} + \frac{g_m}{2}v_{id}\right)R_o = g_m R_o v_{id}$

$\Rightarrow \frac{v_o}{v_{id}} = g_m R_o$ ← what is R_o?



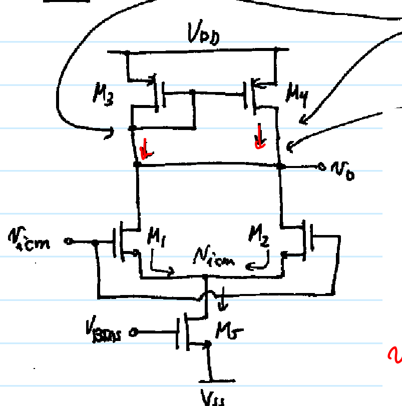
$R_o = r_{o4} \| (2r_{o2})$ → $r_{o2} \| r_{o4}$ ← From the "writing notes"

$r_{o2}\left(1 + g_{m2}\left(\frac{1}{g_{m1}}\right)\right) = 2r_{o2}$

$g_m = g_{m1} = g_{m2}$

$$\frac{v_o}{v_{id}} = g_m (r_{o2} \| r_{o4})$$

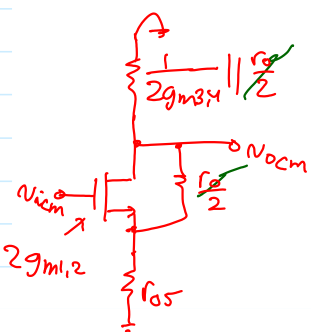
CMRR –



$V_{D3} = V_{D4}$ (they track each other) → provided the ckt. is completely symmetrical.

⇒ Thus, can short the drains of M_3 & M_4

↳ truly symmetric → we can draw a half ckt.
↳ or just combine the two half-ckts. together



$$A_{cm} \doteq -\frac{2g_{m1,2}\left(\frac{1}{2g_{m3,4}}\right)}{1 + 2g_{m1,2}r_{o5}}$$

Thus:

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = g_{m1,2}(r_{o1,2} \| r_{o3,4})(1 + 2g_{m1,2}r_{o5})\left(\frac{g_{m3,4}}{g_{m1,2}}\right) \rightarrow CMRR = (1 + 2g_{m1,2}r_{o5})\,g_{m3,4}(r_{o1,2} \| r_{o3,4})$$

BIG! → Good!

Common-Mode Input Range – Range of input voltages for which all devices remain in saturation.

Low End – must keep M_5 saturated

$V_{icm(min)} = CMR- = V_{SS} + V_{ov5} + V_{GS1,2}$

$$CMR- = V_{SS} + \sqrt{\frac{2I_{D5}}{\mu_n C_{ox}(W/L)_5}} + V_{t1,2} + \sqrt{\frac{I_{SS}}{\mu_n C_{ox}(W/L)_{1,2}}}$$

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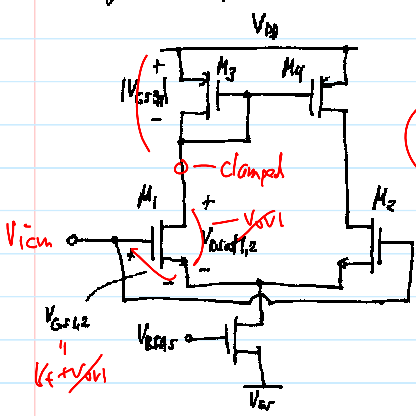
High End - keep M_1, M_2 saturated



$$V_{icm(max)} = CMR+ = V_{DD} - |V_{GS3,4}| - V_{ov1,2} + V_{GS1,2}$$

$$V_{icm(max)} = CMR+ = V_{DD} - \sqrt{\frac{I_{SS}}{\mu_p C_{ox} (W/L)_{3,4}}} - |V_{t3,4}| + V_{t1,2}$$

