Lecture 24: Slew Rate (revisited), Settling Time, and Power Supply Rejection Ratio

- **Announcements**:
- HW#10 due Wednesday at 8 a.m.
- Lab#3 (Design Project) due Friday, Dec. 11, at 11:59 p.m.
- I'm on travel, so this is a videotape lecture
- **Lecture Topics**:
  - Slew Rate (revisited)
  - Settling Time
  - Power Supply Rejection Ratio (PSRR)
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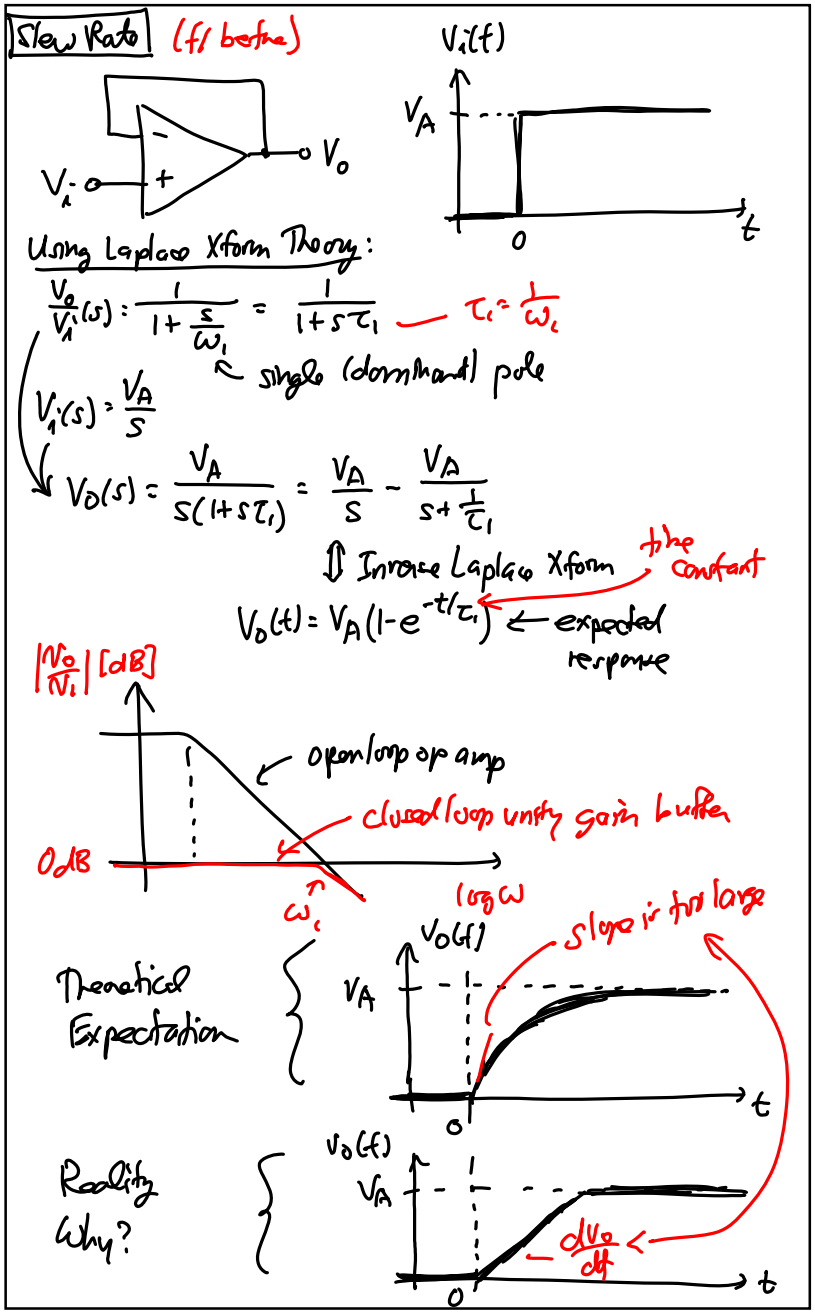
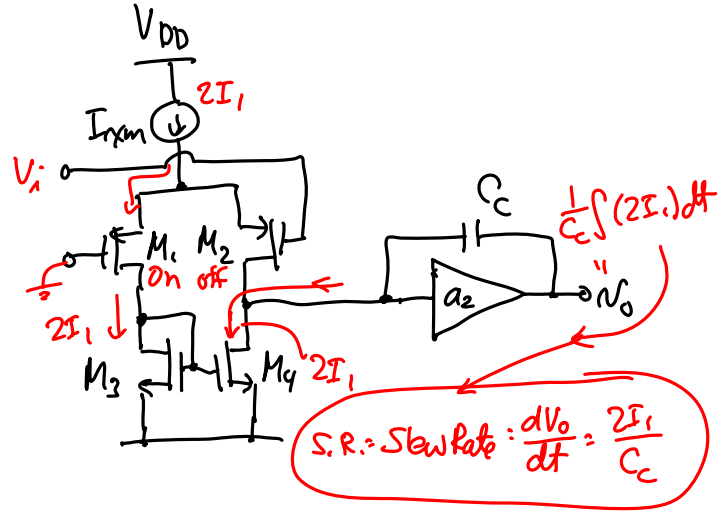
- **Last Time**:
- Started 2nd pass at Slew Rate
- Continue this now

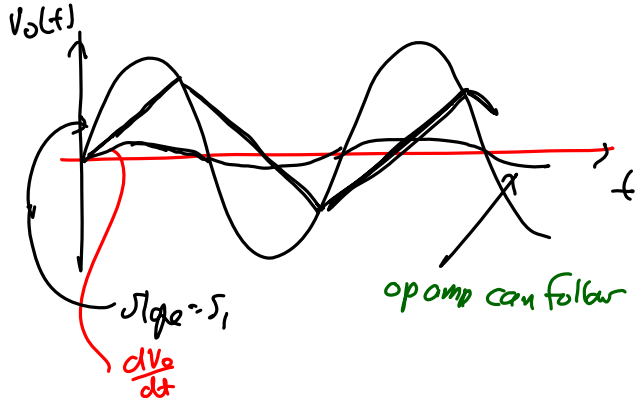
over



Reason: 1st & 2nd stage of op amp cannot source enough current to mimic the shape (or speed) of a fast rising input signal



Ex. If apply a very fast (i.e., high freq., large amplitude) sinusoid:



In terms of design variables:

$$S.R. = \frac{dV_o}{dt} = \frac{I_{xm}}{C_C} = \boxed{\frac{I_{xm}}{G_{m1}} \omega_{ult} A_o = S.R.}$$

$$C_C = \frac{G_{m1}}{\omega_{ult} A_o}$$ ← closed-loop gain

↑ ω_{ult} = ω @ $|a(j\omega)f| = 1$

To Increase S.R.:

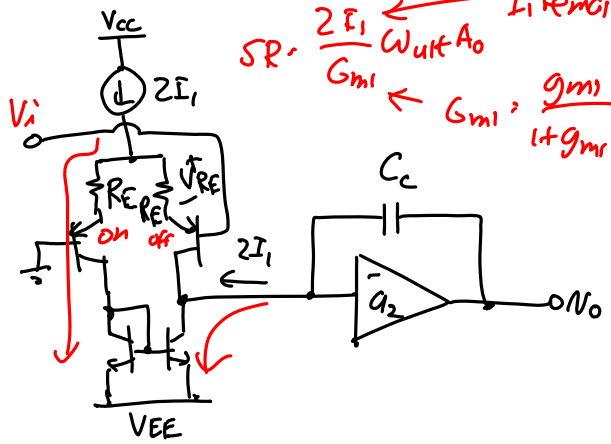
① Decrease G_{m1} ← transconductance of 1st stage

② Increase ω_{ult} → increase ω_2
↘ limited by the system freq. range

③ Use a larger A_o, if possible.
↑ closed loop gain ↓ (only if permitted by the application)

Increasing S.R. via G_m-Reduction

① Emitter or Source Degeneration of the Input Stage –



I_1 remains the same

$SR = \frac{2I_1}{C_{mi}} \omega_{ugf} A_0$

$G_{m1} = \frac{g_{m1}}{1+g_{m1} R_E}$ ↓ → SR↑

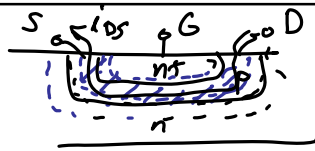
Limitations:

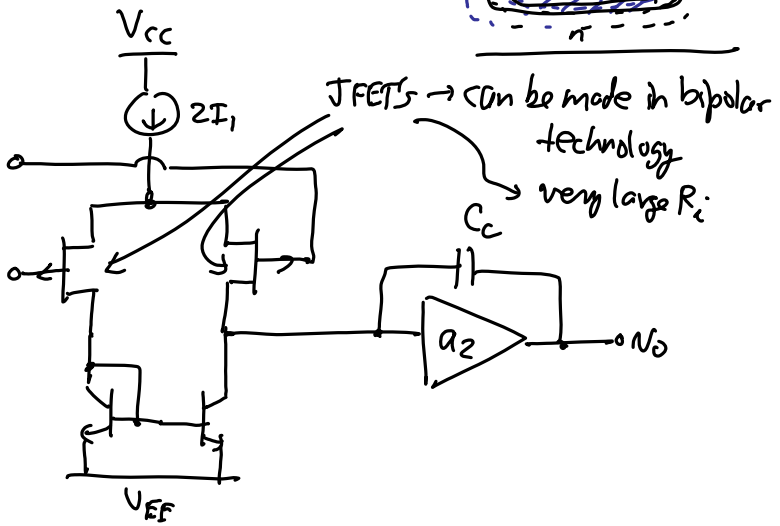
① R_E mismatch → V_{OS}
↳ must limit V_{RE} to limit V_{OS}

② R_E↑ → gain↓ (SR-gain trade-off)

③ R_E contributes thermal noise → must limit to preserve the noise performance of the op amp.

② FET Input Devices –





For FET's: $\frac{g_m}{I_D} \simeq \frac{2}{V_{GS}-V_t}$ ← ~0.2V

For BJT's: $\frac{g_m}{I_C} = \frac{1}{V_T}$ ← 26 mV

$$\frac{\text{FET S.R.}}{\text{BJT S.R.}} = \frac{\frac{I_D}{g_{mF}}\omega_{ugf}}{\frac{I_C}{g_{mB}}\omega_{ugf}} = \frac{\frac{V_{GS}-V_t}{2}}{V_T} = \frac{V_{GS}-V_T}{2V_T} = \frac{260}{26} \approx 10$$

Limitations:

① Higher V_{OS}.

② Increased voltage noise.
(But decreased current noise.)

Settling Time

response to a step V_i: 

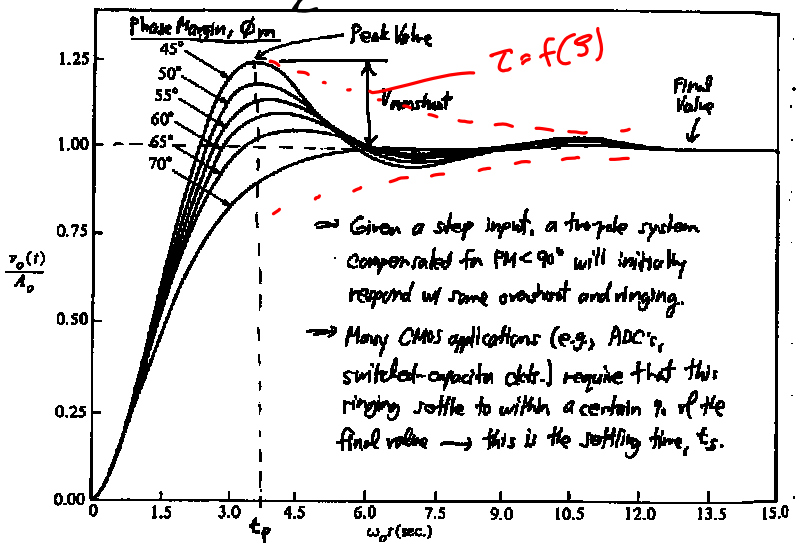


Figure 8.2-3 Response of second-order system with various phase margins.

Obtain Expressions fn:

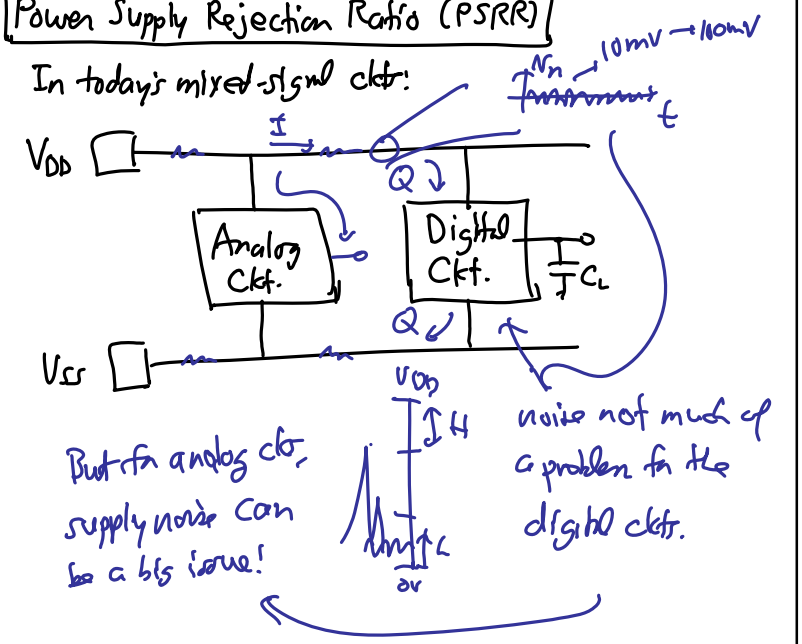
① $V_{overshoot}$
② Settling Time, T_s

} as functions of phase margin, Φ_m

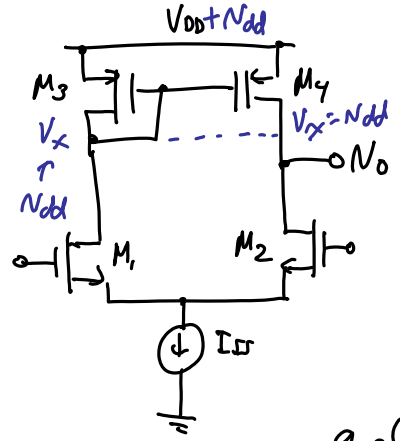
- Go through settling time handout

Power Supply Rejection Ratio (PSRR)

In today's mixed-signal ckts:



Ex. CMOS Differential Input Stage w/ Current Mirror Load



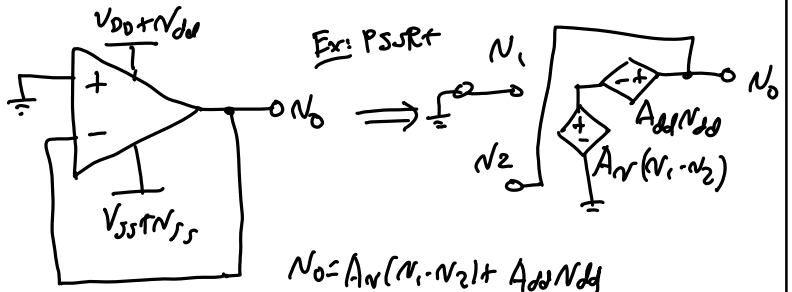
$\frac{V_o}{V_{dd}} \approx 1 \Rightarrow$ supply noise directly seen @ output!

For this example, $PSRR \cong \frac{g_{m2}(r_{o2} \| r_{o4})}{1} = g_{m2}(r_{o2} \| r_{o4})$

Definition. Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain f/ Input to Output}}{\text{Gain f/ Supply to Output}} = \frac{A_{Nr}|_{V_{dd}=0}}{A_{dd}|_{V_i=0}}$$

For more complicated ckts., much more work is req'd.
↳ to make it easier, use a unity gain configuration
↳ can also get PSSR: f(ω)



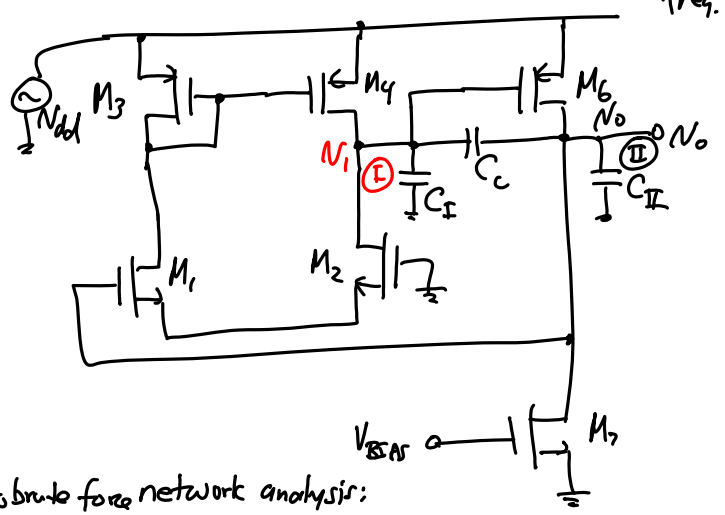
$$N_o = A_{Nr}(\underbrace{V_1 - V_2}_{-V_o}) + A_{dd}V_{dd}$$

$$V_o(1+A_N) = A_{dd}V_{dd} \rightarrow \frac{V_o}{V_{dd}} = \frac{A_{dd}}{1+A_N} = \frac{1}{\frac{A_{Nr}}{A_{dd}}} \approx \frac{1}{PSRR+}$$

$$\frac{1}{PSRR+} = \frac{V_o}{V_{dd}} \rightarrow PSRR+ = \frac{V_{dd}}{V_o}$$

Just find this Xfer fcn to get PSSR+ when the op amp is hooked in unity gain!

Two-Stage Op Amp PSRR+ Want PSRR+ = f(ω) (↑ freq.)



Do brute force network analysis:

KCL(I): $G_I V_{dd} = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_o$

KCL(II): $(g_{mII} + g_{ds6})V_{dd} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_o$

$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$
$G_{II} = g_{ds6} + g_{ds7}$
$g_{mI} = g_{m1} = g_{m2}$
$g_{mII} = g_{m6}$

$[g_{ds} = \frac{1}{r_o}$ ↑ For saturated device.$]$

math & rearranging

Get:

$$\left(\frac{V_{dd}}{V_o}\right)\Big|_{closed\text{-}loop} = \frac{N(s)}{D(s)} = \frac{(\quad)}{(\quad)} \text{ polynomials}$$

↳ then use: $N(s) = 1 + \left(\frac{s}{z_1} + \frac{s}{z_2}\right) + \frac{s^2}{z_1 z_2} \approx 1 + \frac{s}{z_1} + \frac{s^2}{z_1 z_2}$

$$PSRR^+ = A_{V0}^+ \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{GB/A_{V0}^+}\right)} \right]$$

where GB = Gain BW product = $\frac{g_{mI}}{C_C}$

A_{V0}^+ = DC PSRR+ = $\frac{g_{mI} g_{mII}}{G_I g_{ds6}}$

$|p_2| = \frac{g_{mII}}{C_{II}}$ $\quad \omega_p^+ = \frac{GB}{A_{V0}^+}$

To maximize PSRR+: (@dc) decrease g_{ds6}, raise g_{mII}

$$PSRR^- = A_{V0}^- \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{\omega_{p^-}}\right)} \right]$$

where $A_{V0}^- = \frac{g_{mI} g_{mII}}{G_I g_{ds7}}$

$GB = \frac{g_{mI}}{C_C}$ $\quad \omega_p^- = \frac{G_I}{C_C + C_I} \approx \frac{G_I}{C_C}$

$|p_2| = \frac{g_{mII}}{C_{II}}$

To maximize PSRR-: ① decrease g_{ds7}

② increase $g_{mII} = g_{m6}$

Remarks.

① Since often $g_{ds7} < g_{ds6}$ ($r_O = \frac{1}{g_{ds7}}$) → often PSRR- > PSRR+ (@dc)

② $\frac{\omega_p^-}{\omega_p^+} = \frac{G_I/C_C}{\frac{C_I g_{ds6}}{g_{mII} C_C}} = \frac{g_{mII}}{g_{ds6}}$ → that's quite large

$\therefore \omega_p^- \gg \omega_p^+$

Thus, for an NMOS input op amp, PSRR- is often better than PSRR+. → in design, need to worry more about PSRR+!

③ Some methods for maximizing PSRR:

(i) Use buffer-based zero-cancellation in the compensation loop.

(ii) Use cascode circuitry, or balanced circuit topologies.

(iii) Supply-independent biasing.

(iv) Design strategies to minimize parasitic capacitive feedthrough.