

Lecture 7: Active Loads I

- Announcements:
- Lab 1 next week - report to your lab section
- HW#3 online; due next Wednesday at 8 a.m.
- Passed out some extra computer account sheets
 - ↳ Come to my office if you still don't have one
- Lecture Topics:
- ↳ Short Ckt Time Constant (SCTC) Analysis
- ↳ Example Low Freq. Response Determination
- ↳ Active Loads
 - Why active loads?
 - Examples of actively loaded amplifiers

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- Last Time:
 - OCTC analysis to get dominant high frequency pole
 - Ended with two-stage amplifier example

Ex. MOS Two-Stage Amplifier

$C_{in} = C_{gd1}(1 + g_{m1}R_{D1})$

$\tau_{D1} = [C_{gd1}(1 + g_{m1}R_{D1}) + C_{gs1}] R_s$

$\tau_{D2} = [C_{db1} + C_{gd1} + C_{gd2}] (R_{D1} || R_{D2})$

$\tau_{D3} = C_{sb2} (R_{S2} || \frac{1}{g_{m2} + g_{mb2}})$

~~$\tau_{gs2} = C_{gs2} \frac{R_{D1} + R_{D2}}{1 + (g_{m2} + g_{mb2})R_{S2}}$~~

$\omega_H = \frac{1}{\tau_{D1} + \tau_{D2} + \tau_{D3} + \tau_{gs2}}$

Same voltage (w/ unity gain)
 $\Delta V = 0V$
 No voltage drop across C_{gs2} ∴ it's effectively not there!

For a bjt follower: $|A|$

Low Freq. Amplifier Response Using Short Circuit Time Constant Analysis (SCTC)

Recall:

In general, for the low freq. response:

$$F_L(s) = \frac{s^{n_z} + d_1 s^{(n_z-1)} + \dots}{s^{n_p} + e_1 s^{(n_p-1)} + \dots}, \quad n_p = \# \text{ poles} = \# \text{ zeros}$$

We can express the coefficient e_1 by:

$$e_1 = \omega_{p1} + \omega_{p2} + \dots + \omega_{pn}$$

For the case of a dominant pole:
 ↳ i.e., the highest freq. pole

Similar analysis to that used for OCTC...

$$F_L(s) \cong \frac{s}{s + \omega_L} = \frac{s}{s + e_1} \rightarrow e_1 \cong \omega_{p1} = \omega_L$$

$$\omega_L \cong e_1 = \sum_j \omega_{pj} = \sum_j \frac{1}{C_j R_{js}} = \sum_j \frac{1}{\tau_{js}}$$

where $C_j \triangleq$ various large ($> 10 \text{ nF}$) capacitors in the ckt. (e.g., the bypass caps.)

$R_{js} \triangleq$ driving point resistance seen between the terminals of C_j determined with:

For ready, can go to Sedra & Smith

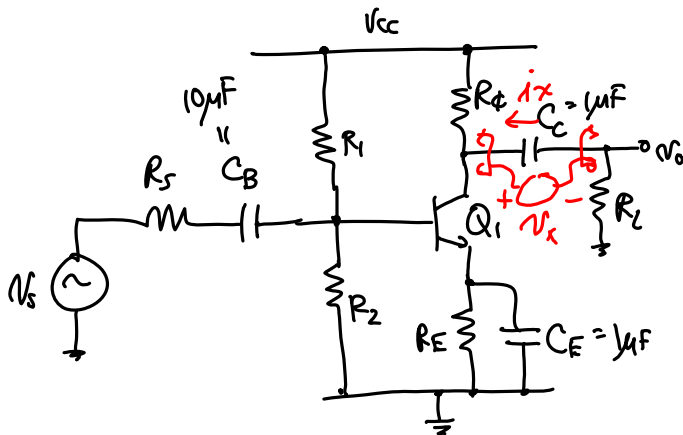
- all large capacitors short-circuited, except C_j , which is replaced by the test voltage source for R determination

- ② all independent sources eliminated (i.e., short voltage sources, open current sources)
- ③ open all H.F. capacitors (i.e., small caps in the pF range, or < 1nF)

Again, for the case where there are no dominant poles, a reasonable approximation is:

$$\omega_L \cong \sqrt{\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{z1}^2 - 2\omega_{z2}^2}$$

Ex: Determine the L.F. response of the C.E. Amplifier



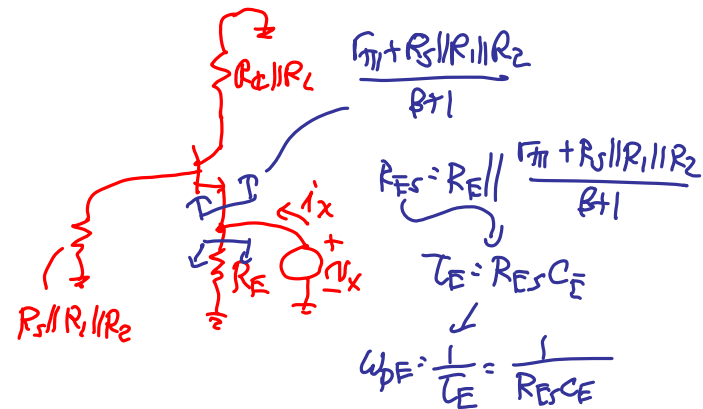
(a) τ due C_B : short ckt. C_C & C_E

$R_{BS} = \frac{v_x}{i_x} = \text{resistance in center w/ } v_x$
 $R_{BS} = R_S + r_{\pi} || R_1 || R_2$
 $\tau_B = R_{BS} C_B = (R_S + r_{\pi} || R_1 || R_2) C_B$
 $\omega_{pB} = \frac{1}{\tau_B} = \frac{1}{(R_S + r_{\pi} || R_1 || R_2) C_B}$

(b) τ due to C_C : short ckt. C_B & C_E
 \Rightarrow again: $R_{CS} = \text{resistance in series w } C_C$
 seen on both sides

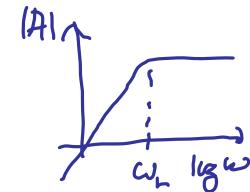
$$\tau_C = (R_L + R_C || R_O) C_C \rightarrow \omega_{pC} = \frac{1}{\tau_C} \approx \frac{1}{(R_C + R_L) C_C} \sim R_C$$

(c) τ due to C_E : short C_B & C_C



and finally:

$$\omega_L = \omega_{pB} + \omega_{pC} + \omega_{pE}$$



Active Loads

⇒ why use them? → Gain: $\frac{v_o}{v_i} = -g_m R_D$

For $\frac{v_o}{v_i} \uparrow$, must:

① Raise $g_m \rightarrow$ raise I_D

Problem: $V_{R_D} = I_D R_D \uparrow$

② raise $R_D \rightarrow$ again, $V_{R_D} \uparrow$ → Limited by supply V_{DD}

another problem: area consumption by R_D → high cost!

Layout:

polysil $\sim 1k\Omega$

Better solution: N_i

Types of Active Loads → want a current source

Diode-Connected Enhancement Load:

to drive X'sistn

Depletion Load:

ancient & we can't consider this

Diode-Connected PMOS Load:

PMOS Current Source Load:

Norton Equivalent:

← ideal when $R_S = \infty$

Diode-Connected Enhancement Load

s.s. Ckt. (do by inspection)

"Diode-Connected"

$$R_L = \frac{1}{g_m} \parallel \frac{1}{g_{mb}} = \frac{1}{g_m + g_{mb}} \approx 1-10k\Omega$$

How about this?

by inspection: $R_s \approx \frac{1}{g_m + g_{mb}} + R_D$

KCL: $i_x = -g_m V_{gs} - g_{mb} V_{bs}$

$$= -g_m (-V_x - i_x R_D) - g_{mb} (-V_x)$$

$$= g_m V_x - g_m R_D i_x + g_{mb} V_x$$

$$i_x (1 + g_m R_D) = (g_m + g_{mb}) V_x$$

$$\therefore R_s = \frac{V_x}{i_x} = \frac{1 + g_m R_D}{g_m + g_{mb}} = \frac{\frac{1}{g_m + g_{mb}} + R_D}{1 + \eta}$$

$R_s \approx \frac{1}{g_m + g_{mb}} + \frac{R_D}{1 + \eta}$

Full hybrid- π analysis:
(in case you want to see it)

s.s. Ckt. (hybrid- π)

$$i_x = -g_m V_{gs} + g_{db} (-V_{gs}) - g_{mb} V_{bs}$$

$$= g_m (V_x - i_x R_D) + g_{mb} V_x$$

$$R_s = \frac{V_x}{i_x} = \frac{1 + g_m R_D}{g_m + g_{mb}} = \frac{1}{g_m + g_{mb}} + \frac{R_D}{1 + \eta}$$

$R_s \approx \frac{1}{g_m + g_{mb}} + R_D$

... and from top to top:

S.S. Def. Hybrid- π

do top analysis

$$R_d = \frac{V_x}{I_x} = \frac{1}{g_m} + (1+\eta)R_S \times \frac{1}{g_m} + R_S$$

Apply to a C.S. Ckt.

$$a_v = \frac{V_o}{V_i} = -\frac{g_{m1}}{g_{m2} + g_{mb2}}$$

$$= -\frac{1}{(1+\eta)} \frac{g_{m1}}{g_{m2}}$$

$$a_v = -\frac{1}{1+\eta} \frac{\sqrt{2\mu_n \mu_p} (W/L)_1 \sqrt{I_D}}{\sqrt{2\mu_n \mu_p} (W/L)_2 \sqrt{I_D}}$$

$$a_v = -\frac{1}{1+\eta} \sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

Diode-Connected PMOS Load

$$a_v = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

PMOS Current Source Load

$$a_v = \frac{V_o}{V_i} = -g_{m1} (r_{o1} || r_{o2}) = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

Gain is huge! → but ... requires VBIAS

Ex. Multi-Stage Actively-Loaded MOS Ckt.

Want R_i, R_o, A_v, ω_H .

$R_o = r_{o3} \parallel \frac{1}{g_{m4} + g_{m64}}$

$$A_v = \frac{V_0}{V_5} \cdot \frac{V_2}{V_0} \cdot \frac{V_0}{V_2}$$

$$= (1 - g_{m1}(r_{o1} \parallel r_{o2})) \cdot \frac{g_{m4}(r_{o3} \parallel r_{o4})}{(1 + (g_{m4} + g_{m64})(r_{o3} \parallel r_{o4}))}$$

$A_v = -g_{m1}(r_{o1} \parallel r_{o2}) \left(\frac{g_{m4}}{g_{m4} + g_{m64}} \right)$

Aside: $\frac{r_{o1}}{n_1} = \frac{g_{m1} R_E}{1 + g_{m1} R_E}$

Now, tackle freq. response: