Note 2: The Basic Building Blocks, Part I

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Abstract Previously we derived equivalent circuits for transistors. We however are not done. Consider the amplifier below. You might imagine trying to plug in the small signal model for every transistor and trying to figure out what is going on. Maybe try some Nodal analysis with about 80 variables. Good luck with that approach! Obviously there is a better way, and in this notesheet we will begin our analysis properly with the basics.

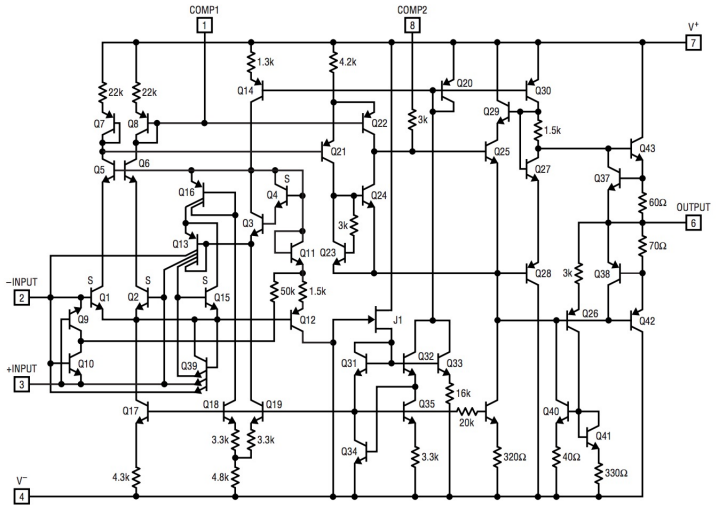

Fig. 1 A typical op-amp example: the LT1008.[1] [1]

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[1] Okay, fine, this is actually one of the more beautiful op-amps out there.

1 Low Frequency Analysis of the Building Blocks

To start off, let us ignore the frequency response of our circuits. This means that all parasitic capacitors are essentially open circuits. Be aware that there will be some algebra, but I will try to keep it to a minimum; thankfully this will be one of the few times extensive algebra is required (though I will not show much of it, since it's tedious and not interesting). All the following blocks will be done for the NMOS FET, though the analysis is the same for the BJT (just remember the input impedance divider). The BJT equivalent block is given in parenthesis. To properly understand and create building blocks for us to use later, we will find the input impedance, output impedance, and transconductance of every configuration.

1.1 Small Signal Circuit Analysis Steps

To analyze a circuit, we follow the tomato model. More specifically, we do the following, using the definitions from notesheet 1:

1. Find the input impedance: open the output, and place a test source at the input, noting that $Z_{in} = (v_{in}/i_{in})|_{i_{out}=0}$
2. Find the output impedance: ground the input, and place a test source at the output, again noting that $Z_{out} = (v_{test}/i_{test})|_{v_{in}=0}$
3. Find the transconductance: Ground the output, attach an input voltage, and find the output current noting $G_m = (i_{out}/v_{in})|_{v_{out}=0}$
4. The gain is simply $-G_m R_o$.

In all cases, note that because we are interested solely in the small signal values, we zero out any DC sources. In all cases note that the probe currents are defined as *entering* the black box.

1.2 The Common Source (Common Emitter) Amplifier

We have actually seen this configuration before, in Note 1, just without a load. Note we define the "common" terminal as the terminal that is used neither as the input or output.

Input Impedance This one is easy- the gate is assumed to have infinite resistance at low frequencies. For a BJT, the base has an input resistance of r_π.

Output Impedance We first plug in the small signal model circuit into the transistor, ground the input, and place a test source at the output. Our setup is thus shown in **Fig 3**. Since both our gate and source are grounded, V_{gs} is zero, so the output resistance is by observation just $R_o = r_o \parallel R_L$.

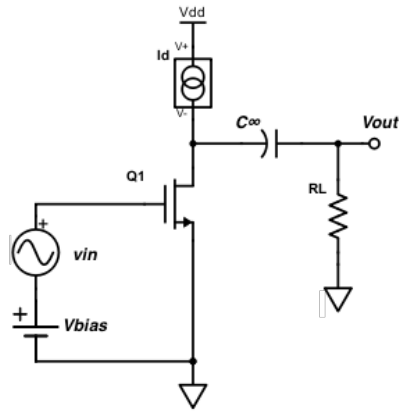

Fig. 2 The common source configuration, with load R_L. Note that C_∞ is an AC coupling capacitor, that acts as an open for DC signals, but a short for any AC signal, even low frequency ones.

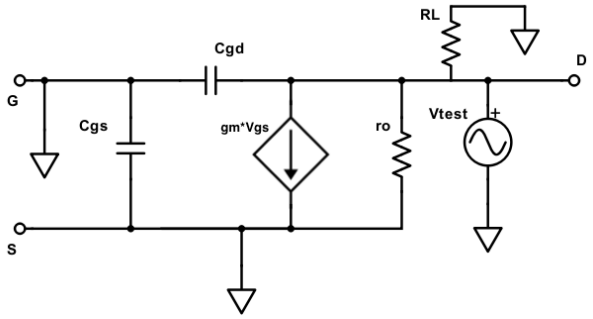

Fig. 3 Common Source Output Impedance Setup.

Transconductance This one is easy as well; With the output grounded, the output current flowing into the box due to an input v_{in} is just $g_m v_{in}$, so $G_m = g_m$.

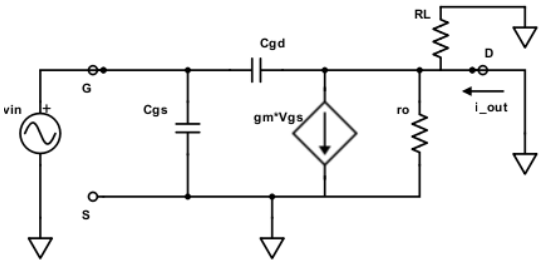

Fig. 4 Common Source Transconductance Setup.

1.3 The Degenerated Common Source Amplifier

Consider the general case for a common source configuration, seen in **Fig 5**. The input resistance remains infinite, but the output resistance and transconductance differ.

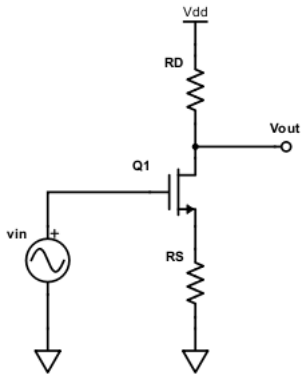

Fig. 5 The more general common source case. Note that DC biasing has been omitted for simplicity, and we are ignoring the load RL.

Output Resistance The setup to find the output resistance is shown in **Fig 6**. Be-

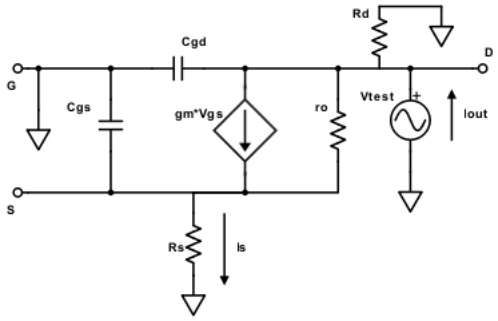

Fig. 6 Output Resistance setup for the degenerated Common Source. Note that $V_{gs} \neq 0$, and if we ignore Rd (to find the output impedance looking *into the drain* only), $I_s = I_{out}$.

cause of R_s, $V_{gs} \neq 0$, which makes this a little more complicated. But we note that

the output resistance will be $R_d \parallel$ [resistance looking into the drain][2]. To find the resistance looking into the drain, we can ignore R_d, and therefore the current flowing through R_s must be equal to I_{out}. We can thus set up the following equations, noting that at low frequencies the capacitors are open:

$$I_{out} = g_m(0 - V_s) + (V_{test} - V_s)/r_o. \tag{1}$$

$$V_s = I_{out} R_s. \tag{2}$$

Combining the two equations results in, after a couple of algebraic steps:

$$R_{o,drain} = V_{test}/I_{out} = r_o + (1 + g_m r_o)R_s \tag{3}$$

$$R_o = R_{o,drain} \parallel R_d = (r_o + (1 + g_m r_o)R_s) \parallel R_d \tag{4}$$

Transconductance The setup is shown in **Fig 7**.

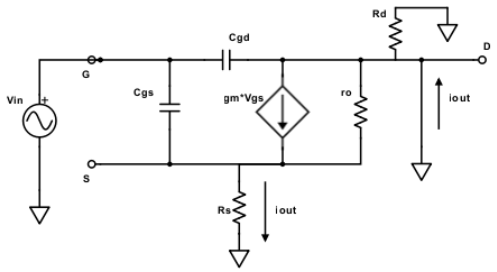

Fig. 7 G_m setup for the degenerated Common Source. Note that $I_s = I_{out}$ again.

Therefore:

$$i_{out}(1 + g_m R_s + \frac{R_s}{r_o}) = g_m v_{in} \tag{5}$$

$$G_m \equiv \left.\frac{i_{out}}{v_{in}}\right|_{v_o=0} = \frac{g_m}{1 + g_m R_s + R_s/r_o} \tag{6}$$

Note that as R_s approaches zero, we get the same results as found previously. Also note that degeneration *decreases* the gain of the common source stage. For example, if $R_d < r_o$ and $R_s \gg \frac{1}{g_m}$, from $-g_m R_d$ to $-\frac{g_m R_d}{1+g_m R_s}$.

[2] Make sure you understand why this is true. This will show up many times.

1.4 The Common Gate (Common Base) Amplifier

The "common" or grounded terminal here is the gate, with the input fed into the source of the transistor.

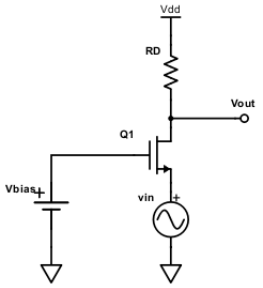

Fig. 8 The Common Gate amplifier. Note DC biasing is omitted, and an ideal voltage source (no source impedance) is used for the input.

Input Impedance The input impedance is no longer infinte, since we are not looking into the gate of the MOSFET.

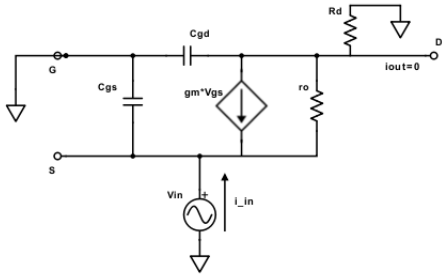

Fig. 9 Input Impedance setup for the common gate.

Noting that[3]:

$$r_{in} \equiv \left.\frac{\partial V_{In}}{\partial I_{In}}\right|_{I_{out}=0} = \left.\frac{v_{in}}{i_{in}}\right|_{i_{out}=0} \tag{7}$$

We set up

$$i_{in} + g_m(-v_{in}) + (i_{in}R_d - v_i)/r_o = 0 \tag{8}$$

[3] This comes from two-port theory- I will not delve into specifics, but only mention it for the interested reader.

Resulting in, after some algebra:

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_o + R_d}{1 + g_m r_o} \approx \frac{1}{g_m}(1 + R_d/r_o) \tag{9}$$

Note that we assumed there was no resistor added to the gate of the MOSFET; the resistor would actually have an affect on the impedance.

Output Impedance We note that the output impedance has the same setup as the common source, and will therefore have the same output impedance. If the input had a source resistance R_s as well:

$$R_{out} = (r_o + (1 + g_m r_o)R_s) \parallel R_d \tag{10}$$

Transconductance If we use an ideal input source, with no source impedance, then the transconductance is by observation $G_m = -g_m$. With a source impedance, we get the same result as a degenerated common source, albeit with opposite sign:

$$G_m = -\frac{g_m}{1 + g_m R_s} \tag{11}$$

The Common Gate as a Current Buffer In reality, the common gate is never used as a voltage amplifier due to its low input impedance;[4] instead it is better thought of as a *current buffer*.

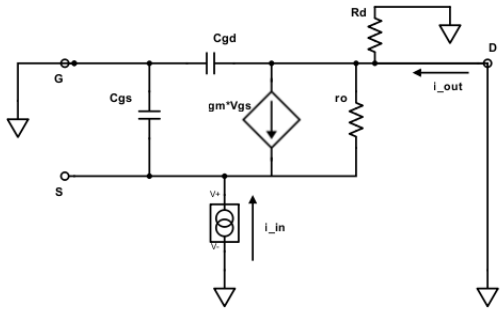

Fig. 10 The Common Gate viewed as a current buffer.

To find the current gain of a circuit, we ground the output, and find i_{out}/i_{in}. Looking at **Fig 10** we can see again by observation that the current gain is simply -1. The use of the common gate stage will be examined more closely in the upcoming notes.

[4] We will explain this more carefully in the next notesheet.

1.5 The Common Drain (Common Collector) Amplifier

The common drain schematic is shown below.

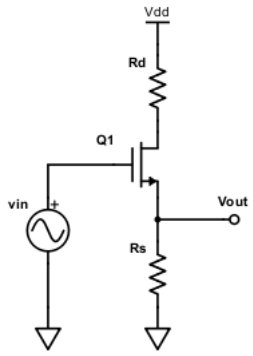

Fig. 11 The Common Drain Amplifier, DC biasing omitted.

Input Impedance Again, for a MOSFET, the gate has infinite resistance. For a BJT, it would be r_π.

Output Impedance We could plug in the small signal model and solve for the output impedance, or we could more simply notice that it is simply R_s in parallel with the input impedance of the source (the input of a common gate amplifier).

$$\therefore\ R_{out} \simeq \frac{1}{g_m}(1+R_D/r_o) \parallel R_s \tag{12}$$

Transconductance Our setup is shown in **Fig 12**. We start with:

$$i_{out} + g_m v_{in} + (i_{out} R_d)/r_o = 0 \tag{13}$$

Which results in (after a bit of rearranging):

$$G_m = \frac{-g_m}{1+R_d/r_o} \tag{14}$$

The voltage gain is: $A_v = -G_m R_{out}$. If we choose $R_d = 0$, and have $R_s \gg \frac{1}{g_m}$, then $R_{out} \approx \frac{1}{g_m}$, $G_m = -g_m$, and thus $A_v \approx 1$. This, combined with its low output impedance suggests that the common drain can be used as an output buffer. Again, the uses of these blocks will be explored further in the next notesheet.

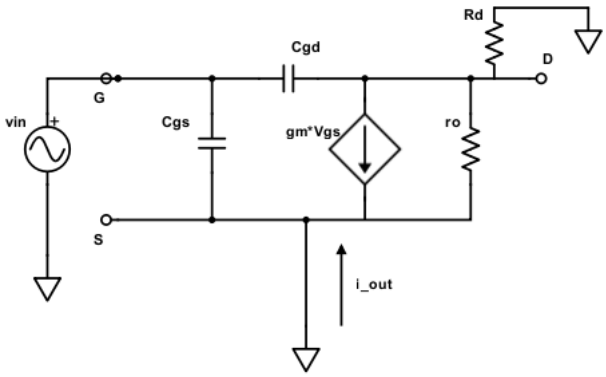

Fig. 12 Transconductance setup for the common Drain.

2 Summary of the Topologies

Phew that was a lot! Hopefully you hung in there- make sure that you either remember or are capable of quickly finding out the basic properties of all the building blocks we covered. They are summarized in **Table 1**.

Table 1 Summary of the Building Blocks

Block	Input Resistance	Output Resistance	Transconductance
CS	∞	$(r_o + (1+g_m r_o)R_s) \parallel R_d$	$g_m/(1+g_m R_s + R_s/r_o)$
CG[a]	$\frac{1}{g_m}(1+R_d/r_o)$	$(r_o + (1+g_m r_o)R_s) \parallel R_d$	$-g_m/(1+g_m R_s + R_s/r_o)$
CD	∞	$\frac{1}{g_m}(1+R_d/r_o) \parallel R_s$	$-g_m/(1+R_d/r_o)$

[a] For the input impedance, we assume an ideal voltage source. For R_{out} and G_m we do not.

3 A quick preview: Cascaded Stages

Now you might be wondering, what exactly have we accomplished? In the beginning I said we do not want to simply just plug in the small signal model into every transistor- but didn't we just do that in this notesheet? The answer is yes, we did, but *only for these blocks*. Indeed, in these notes we will never use the transistor small signal model again; rather we shall think solely in terms of these blocks from now on. We have essentially created another layer of *abstraction*.

Consider the following circuit in **Fig. 13**. Previously, such a circuit may have been

rather intimidating.[5] Let's see if we can figure out the small circuit gain of this circuit (answer: yes, we can). Remember, $A_v = -G_m R_{out}$.

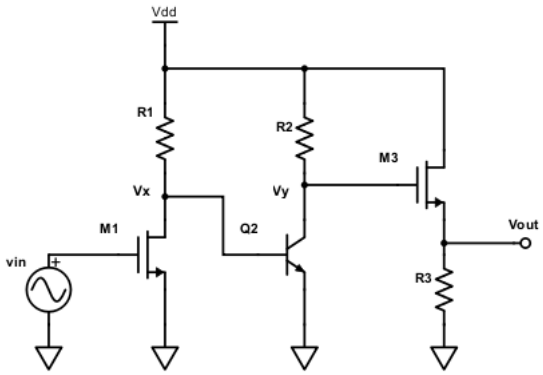

Fig. 13 Example Cascade circuit. No DC biasing for simplicity.

Output impedance We ground the input voltage, and apply a test voltage at the output (see **Fig 14**). Notice that we are just looking at a simple common drain block. $\therefore R_{out} = \frac{1}{g_{m,3}} \parallel R_3$.

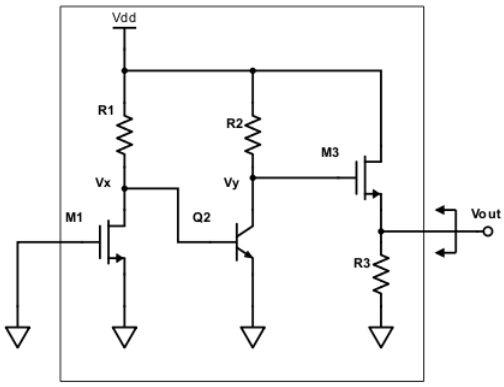

Fig. 14 Finding the output impedance. Again, nothing new- treat the circuit as a mystical box, and follow the tomato model rules!

Transconductance The transconductance is more tricky, but it will show us the beauty of our abstraction. Again, as before, we ground the output and find the output

[5] Don't worry if it still is scary-looking! It will just take a some practice.

current due to v_{in}. Now we know that for every block, the output current due to an input voltage is given by its G_m. We therefore know:

$$i_{out} = G_{m,3}V_y = -g_{m3}V_y$$

The question is, what is V_y? To find out, we recurse! We can see that the V_y is set by the second stage, Q2, a Common Emmiter amplifier.

$$\begin{gathered}\therefore\ V_y = A_{v,2}V_x = -G_{m,2}R_{out,2}V_x \\ R_{out,2} = R_2 \parallel r_{o,2} \quad \& \quad G_m = g_{m,2} \\ \implies V_y = -g_{m,2}(R_2 \parallel r_{o2})V_x\end{gathered}$$

And now V_x? We can see V_x is related to v_{in} by the first stage, a common source block. There is one important thing to note: because Q2 is a BJT, it has an input impedance of $r_{\pi,2}$; this must be taken into account when finding the output resistance of this stage.

$$\begin{gathered}R_{out,1} = r_o \parallel R_1 \parallel r_{\pi,2} \\ G_{m,1} = g_{m,1} \\ \implies V_x = -g_{m,1}(r_o \parallel R_1 \parallel r_{\pi,2})v_{in}\end{gathered}$$

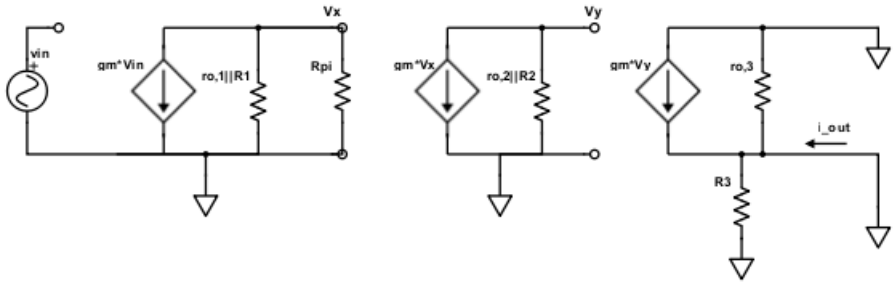

Fig. 15 Equivalent circuit used for finding the transconductance. Notice how we have substituted the input & output resistances and transconductances relevant for each block.

The total transconductance is thus:

$$G_m = [-g_{m,1}(r_{o,1} \parallel R_1 \parallel r_{\pi,2})][-g_{m,2}(R_2 \parallel r_{o2})][-g_{m,3}]$$

And thus the total voltage gain, A_v:

$$A_v = -G_m R_{out} = g_{m,1}g_{m,2}g_{m,3}(r_o \parallel R_1 \parallel r_{\pi,2})(R_2 \parallel r_{o2})(\frac{1}{g_{m,3}} \parallel R_3)$$

Not bad eh? Give yourself a pat on the back- you deserved it.

Acknowledgements

All drawings were done with Digi-Key's free Scheme-it applet.

References

1. LT1008 Datasheet. http://cds.linear.com/docs/en/datasheet/1008fb.pdf