Note 3: The Basic Building Blocks, Part II

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Abstract Analog design is an art form- good designers use and develop an intuition to guide them through their designs. The first two notes were an introduction to the basics; in this notesheet we will try to gain some intuition by looking at the applications, pros, and cons for the building blocks covered in Note 2.

1 Input and Output Impedances: Why do they matter?

Input and output impedances determine how blocks interface with each other. Let's first consider the general scenario where we wish to provide as much gain to a load of *unknown* resistance, R_L. We will see that the resistance of the load, in relation to the output impedance, impacts the gain of a circuit. Let us imagine the load attached to a generic 2 port:

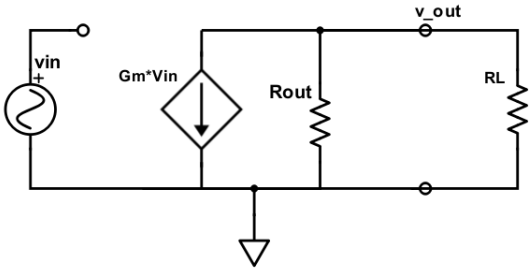

Fig. 1 A load, with resistance R_L, attached to a generic stage, with output impedance R_o.

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The output is, by observation, $v_{out} = -G_m(R_{out} \parallel R_L)v_{in}$.[1] Now consider the possible loads:

- Case 1: $R_L \gg R_{out} \implies |A_v| \simeq G_m R_{out}$
- Case 2: $R_L = R_{out} \implies |A_v| = \frac{1}{2} G_m R_{out}$
- Case 3: $R_L \ll R_{out} \implies |A_v| = G_m R_L$
  - It may not seem significant at first, but this is a problem! Imagine we have a small load, a 50Ω load, and a G_m of 1mA/V - a common scenario. We would have a "gain"-if you can call it that- of 0.05! Is there a fix? Of course! That's where voltage buffers come into play (read on!).

Note that a low impedance load can ruin an entire circuit unless its buffered. Imagine spending months on designing a gigantic output impedance to get a high gain, and your customer hooks up a 5-ohm load to it! The solution is to instead have a very large transconductance, and a low output resistance. This is achieved by using multiple stages, usually a gain stage (to give the high G_m), followed by a low output impedance stage, called a buffer, to interface with the load.

What about input impedances?

- In a cascade of stages, the input impedance of one stage may affect the gain of the previous stage!
  - Essentially think of the input impedance of the proceeding stage as the load, R_L, of the preceding stage.
- In the real world, all sources have a finite impedance. For a voltage amplifier then, we would want the input impedance of the amplifier to be much larger than the source impedance to provide maximum voltage transfer[2].

2 The Gain Block: The (non-degenerated) Common Source/Emitter

The (non-degenerated) common source amplifier is usually used as (not surprisingly) a voltage amplifier, due to its high input impedance (the gate or base of the transistor) and output impedance. From the previous notesheet, we saw that its gain has magnitude $g_m r_o$, if biased by an ideal current source in the drain. This is often called the "intrinsic gain" of a transistor, since it represents the maximum voltage gain possible for a single transistor.

The problem about ideal current sources of course is that they do not exist. Let's instead first consider the case where the drain/load is a resistor (**Fig. 2**).

[1] This should be readily apparent at this point. If not, review Note 2 again.

[2] Note that we are not asking for maximum power transfer. We would then actually want an impedance match.

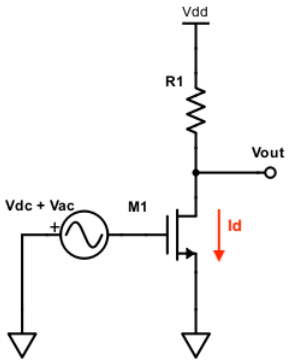

Fig. 2 The common source with a resistive load. Note that the input provides the biasing as well, via Vdc, which sets the current Id.

We know the gain, $A_v = -g_m(r_o \parallel R_1)$. To maximize the gain, we would therefore want $R_1 \gg r_o$. Sounds simple, but there's a catch: we have to worry about the operating points of the circuit.

2.1 Remembering the operating point: DC Biasing and Output Swing

Refresher: MOSFET Requirements for Saturation
We must have (for a NMOS-FET):

$$V_{DS} > V_{ov}, \text{where } V_{ov} = V_{GS} - V_{Th}$$
$$V_{GS} > V_{Th}$$

Looking at **Fig. 2** again, notice how V_{dc} sets the current, I_d, through M1 (again, we normally ignore the channel length modulation term, λV_{DS}). R_1 therefore has a voltage drop across it, $\Delta V = R_1 I_d$. To ensure M1 still operates in the saturation region, we must make sure that the drain voltage does not drop too low:

$$V_{dd} - R_1 I_d > V_{ov} \tag{1}$$

Show that the CS gain is determined solely by the voltage drop across R_1 and V_{ov}

Assuming $R_1 \ll r_o$, we have:

$$\begin{aligned} |A_v| &= g_m R_1 \\ &= \frac{2I_d}{V_{ov}} \frac{\Delta V}{I_d} \\ &= \frac{2\Delta V}{V_{ov}} \end{aligned} \tag{2}$$

From (1) and (2) we can see then that our gain is limited by the voltage headroom, set by V_{DD} and V_{ov}. Now in the good ol' days of vacuum tubes and their 300V supplies, this was not a problem; today however, most supplies on phones and sensors range from 1.2 to 3V. For instance, for a 1.2V supply and $V_{ov} = 200mV$, we can get a gain of at most 10, since $\Delta V = 1V$ would be the maximum allowed for saturation[3].

The observant reader might note that we could just make V_{ov} increasingly smaller and get infinite gain! Unfortunately, device physics gets in the way and limits us here.

Rule of Thumb: $V_{ov} \geq 100mV$ required for Saturation.[4] Sorry, no free lunch.

Output Swing There is another consideration we have to take into account: the signal itself! The output, V_D will actually be at a voltage $V_D = V_{D,dc} + V_{d,ac}$, the superposition of the DC and AC signals. For a sinusoidal signal then, we must make sure that its peak and trough do not put the device into saturation! The *output swing* is thus defined as the maximum sinusoidal amplitude we can superimpose on the output.

Output Swing of a Common Source
We know V_d must be within $[V_{ov}, V_{DD}]$.

$$\therefore \quad Swing = min(V_D - V_{ov},\ V_{DD} - V_D) \tag{3}$$

Where V_D is the drain's DC bias point.

To maximize the swing, set $V_D = \frac{1}{2}(V_{DD} - V_{ov})$, the midpoint.

The NPN Common-Emitter Although the gain of the common-emitter is not quite the same as (2), the operating point limitation remains the same: remember the collector must be above $V_{CE,sat}$, which limits the voltage (IR) drop across the collector resistor. You therefore cannot arbitrarily get a large gain by increasing the collector resistance.

[3] You may vaguely recall from introductory circuits classes that op-amps have a gain of a couple million. Ten is not going to cut it.

[4] Below this point the MOSFET is considered in the sub-threshold regime. There are actually many interesting uses for sub-threshold MOSFETs, due to their exponential I-V responses (like a BJT), for ultra-low power applications. Their low current however limits their speed severely.

2.2 Active Loads: The Complementary Transistor

The solution to this headroom quandary? We use complementary transistors instead of resistors.

Refresher: PMOS Characteristics
An easy way to think of PMOS transistors: just flip the voltage & current directions (this is true for the small signal model as well)[5].
The I-V equation:

$$I_{SD} = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{SG} - |V_{tp}|)^2 (1 + \lambda V_{SD}) \tag{4}$$

Saturation requirements:

$$V_{SG} > |V_{tp}| \tag{5}$$

$$V_{SD} > V_{ov}, \text{ where } V_{ov} = V_{SG} - |V_{tp}| \tag{6}$$

Now kindly consider the circuit seen below (**Fig. 3**). Let's first quickly look at the

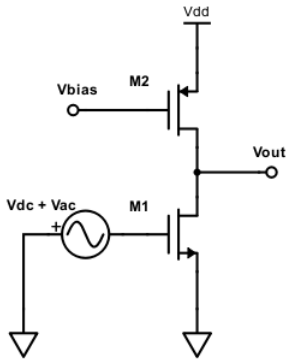

Fig. 3 The common source with an active (PMOS) load. Assume M2 is properly biased in the saturation regime.

small signal gain. G_m remains unaffected: it's still just g_{m1}. The output impedance is the parallel combination of the impedance looking into the drain of M1 with the impedance looking into the drain of M2. Therefore, $R_{out} = r_{o1} \parallel r_{o2}$. The gain is thus:

$$A_v = -g_{m1}(r_{o1} \parallel r_{o2}). \tag{7}$$

[5] I find this to be the easiest way to remember things. This way, you can treat the threshold voltages as absolute values, instead of trying to think whether the thresholds are negative or positive or something. Also note from now on, we will distinguish between the N-type and P-type thresholds and mobilities with a subscript n and p respectively.

And if $r_{o2} = r_{o1}$, then we have $A_v = -\frac{1}{2} g_{m1} r_{o1}$. We can see thus that we have thus increased our gain considerably, almost to the intrinsic gain of the transistor!

Voltage Headroom and Swing This is where the active load truly shines: notice now that now the gain of the circuit no longer depends on the voltage drop across the load- as long as both M1 and M2 remain in saturation, we will have a high gain. To ensure this, the output voltage must be within $[V_{ov1}, V_{DD} - V_{ov2}]$. No longer do we need 300V supplies for gain!

One subtlety to note here is that while the output common mode range is defined (above), the swing is not exactly defined because the DC output voltage is not well defined. Remember how we normally drop the V_{DS} term when thinking about the DC biasing? In this circuit however, note that this is the only term that sets the output voltage (since it is the drain of both transistors)! For this reason we say it is not well defined: in the real world the lambda factor varies a lot with process variations (and remember, no transistor on silicon ever ends up exactly how you want it), and is a major approximation in the first place. To properly set the output DC voltage, a technique called *common-mode feedback* is used- but this is a bit advanced for us right now!

3 The Source Follower

The source follower, sometimes referred to as the common drain (a terrible name in my opinion) is commonly used for level-shifting and as a buffer.

Why a "Source Follower?" Consider the configuration shown in **Fig. 4**.

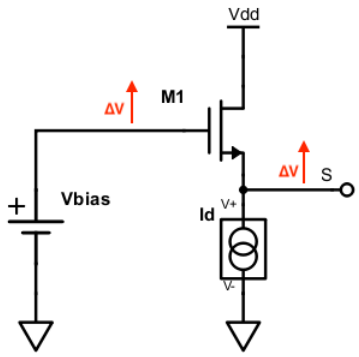

Fig. 4 The Source Follower. Notice that if a change, ΔV, is applied to the gate, in order to maintain a constant current I_d through M1 the same change must occur at the source.

Assume that the current through M1 is set by the current source, I_d. The voltage at the gate is arbitrarily set to satisfy saturation conditions[6]. If a change, ΔV, is

applied to the gate, then the same change must occur at the source to keep the current constant- the source therefore *follows* the gate! To see why this is, consider:

$$I_{DS} + \Delta I_{DS} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_G + \Delta V_G - (V_S + \Delta V_S) - V_{tn})^2 (1 + \lambda V_{ds})$$

Let's ignore the λV_{ds} error term[7]. Then we can see quite easily in order for I_{DS} to remain constant, ΔV_S must equal ΔV_G.

This is seen from the small signal analysis as well: From before:

$$A_v = -G_m R_{out} = -[-g_m/(1 + R_d/r_o)] * [\frac{1}{g_m}(1 + R_d/r_o) \parallel R_s]$$

We know $R_d = 0$, and after expanding the the output resistance (actually writing the equation for a parallel resistance), we get[8]:

$$A_v = \frac{g_m R_s}{1 + g_m R_S} \tag{8}$$

And if $g_m R_S \gg 1$, noting that R_s in this case is the resistance of the current source (infinite for an ideal source), then $A_v \approx 1$, as expected.

3.1 The Follower as a Voltage Buffer

The source or emitter follower's low output impedance makes it ideal for use as an output buffer. A very low load resistance will decrease the small-signal gain however; it is therefore important to make sure $g_m R_s$ is at least greater than 1 (for a loss of only 1/2). Output stages therefore have to burn more current to increase the g_m for potentially small impedance loads (there are other reasons to burn more current, such as slewing and linearity, but that's for later). We will also see that the follower's low impedance output node will be useful for high speed circuits as well when we cover frequency response.

3.2 The Follower as a Level Shifter

The second most common application of the source follower is as a level-shifter. A level-shift is essentially a DC operating point change. Consider the circuit below:

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[6] You might wonder why I say the gate bias is arbitrary. The reason is because the source will adjust accordingly to provide the correct overdrive voltage necessary to produce the enforced current.

[7] Again we ignore the Vds term because the current is a strong function of the gate-source voltage (a squared term), and not the drain-source voltage.

[8] Having a R_d would decrease its performance as a follower, and is almost never used, except occasionally for ESD purposes on output stages.

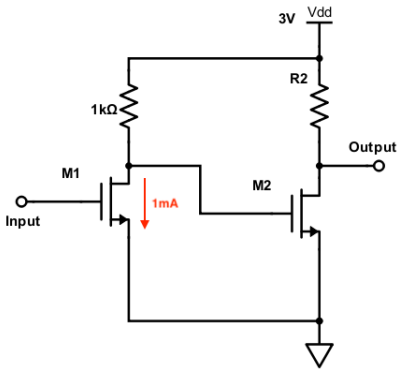

Fig. 5 Example cirucit with no level shifting. Ignore the DC biasing of M1, and just assume that M1 has 1mA running through it.

Is this a practical circuit? Consider the voltage at the gate of M2: the IR drop across the 1kΩ resistor puts the gate of M2 at 2V. If the threshold of M2 is about 0.5V, this means we would have an overdrive voltage of 1.5V, extraordinarily high! And if M2 were to be a NPN instead of a FET, we would be setting its V_{BE} to 2V- sinking so much current the BJT would melt itself or blow up the supply[9]!

Now consider the following (**Fig. 6**), with a level shifter:

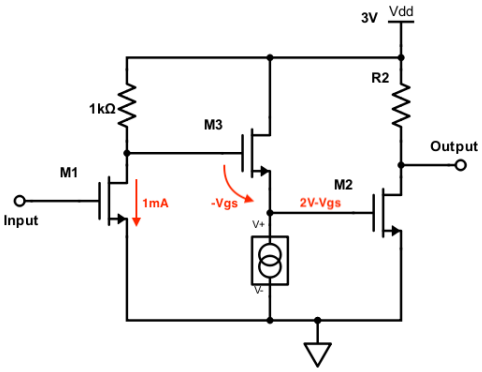

Fig. 6 Example cirucit with a level shift. Note that the voltage at the gate of M2 has been dropped by the V_{GS} of M3.

We can see that M3 will decrease the voltage at the gate of M2 by a V_{gs}, which can be set by the current source supplying M3. If the voltage has to be dropped even further, a resistor can be added (between the source of M3 and the Gate of M2) as well to give a further IR drop. This is a level shift: we dropped the DC voltage to a reasonable value for M2 to operate at, while retaining the same small signal gain we

[9] The observant reader might say: why don't we just use PMOS for M2! Which is a great observation and what is often done. However, not all processes have complementary transistors, and sometimes even if they do, they can sometimes have terrible characteristics that make them unsuitable for anything besides DC biasing.

had in **Fig. 5**. This idea of "reasonable operating voltages" is often called the *input common mode range*, something we will explore much more later on.

4 The Ugly Duckling: the Common Gate or Base

The common gate really is ugly to the analog designer. It only becomes a swan when attached to other blocks, in a cascode configuration (which will be discussed in future notes). On its own? An ugly duckling, straight up[10].

Why is it almost never used as a stand-alone block? For Voltage-Voltage amplifiers: its low input impedance. Consider **Fig. 7**.

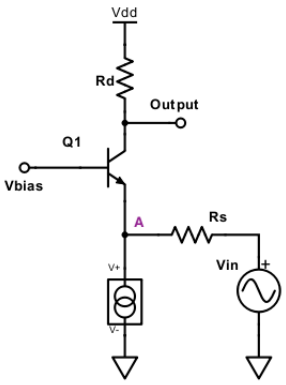

Fig. 7 A Common Base example. Assume $R_d \ll r_o$.

Let's say R_s= 50Ω (typical), and Q1 is driven with 100μA. It's g_m is then:

$$g_m = \frac{I_c}{V_T} = \frac{100\mu A}{26mV}$$

Now what is the signal voltage at Node A, the actual input to Q1? Notice that it is set by the voltage divider of $1/g_m$ (the input impedance of Q1), and R_s.

$$V_A = \frac{1/g_m}{R_s + 1/g_m} v_{in} = \frac{260\Omega}{260 + 50\Omega} = 0.83 v_{in}$$

Essentially, the low input impedance has thrown away almost *20% of our gain by itself*! And unfortunately, to increase the input impedance, we would have to lower the g_m, which would then decrease our gain anyways at the output! We can't win.

[10] Do kids read nursery rhymes still? The "Ugly Duckling"? I hope so, otherwise I'd feel *really* old.

What about using a the common gate as a current buffer? Its low impedance input would be helpful for this right? This is indeed what it's often used for, though always in the *inner workings of the circuit, where we can control the results of every current divider*. It's never used as an input- looking at the previous example, 260Ω could be a potentially large input resistance for a current input (what if the current source has a mediocre output impedance...gulp). And to even get 260Ω we had to burn a considerable amount of power. And for MOSFETs, it will taken even *more* power to get the same transconductance as a BJT. In reality, current-to-voltage (TIAs) and current-current amps usually use special feedback configurations to get very low input impedances without sacrificing gain (if done right of course).

There is actually something more sinister to be aware of when considering a common gate's input impedance: its load effects the input. Consider the same circuit as before, but with an active load.

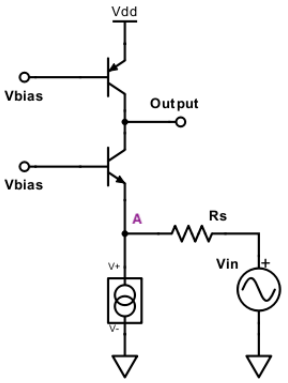

Fig. 8 The Effect of the Active Load on the common base input impedance.

In **Fig 7** we had made seemingly innocuous statement: "Assume $R_d \ll r_o$." Notice now that is no longer the case: our active load has an impedance of $r_{o,p}$ as well (lets assume the PNP and NPN have the same r_o values). Remembering the complete input impedance equation at node A[11]:

$$R_{in} = \frac{1}{g_m}(1 + R_d/r_o) = \frac{1}{g_m}(1 + r_o/r_o) = \frac{2}{g_m}$$

We have now *doubled* our input impedance; our poor current buffer is not doing so well. And when we look into the cascode later on...we will find we can actually

[11] One thing to note: for BJTs, any external resistance at the base actually influences the impedance at the source, leading to an additional summed $\frac{R_B}{\beta}$ term. As long as β is large however, this contribution is usually negligible. In this example, we assume $R_B = 0$.

turn this low impedance node into a high one! The take away lesson: *Never* simplify equations too early- you may be given a rude awakening[12]!

5 Summary

We have looked a bit more carefully at each of the amplifier blocks and examined their nuances and uses. Along the way we discovered the input and output common mode and swing complications, and the benefit of active devices. Practice will make looking for these subtleties second nature. Looking ahead, we will apply this knowledge and learn a new topic too, frequency response (remember those capacitors?), by analyzing the cascode. And from there, a few short topics (current mirrors and diff pairs) will allow us to finally look at some old op amps for practice (and not be too scared)!

Acknowledgements

The schematics were made with Digikey's free Scheme-it tool.

[12] By this I mean, make sure you remember the *full* equations for each block. Only when you see the values of Rs, Rd etc. should you make simplifying approximations. Thinking the input impedance of the source is always just $1/g_m$ can lead to major trouble.