NAME:

EE 140/240A Linear Integrated Circuits
Fall 2019 SID: Midterm 1

1. Impedance Calculation

(a) Calculate the magnitude of the impedance of a 1 pF capacitor at 10^3, 10^6, and 10^9 radians per second.

$\left|\frac{1}{\omega C}\right|$ $10^3 \frac{rad}{s} \rightarrow 10^9\,\Omega$

$10^6 \frac{rad}{s} \rightarrow 10^6\,\Omega$

$10^9 \frac{rad}{s} \rightarrow 10^3\,\Omega$

(b) If this capacitor is in parallel with a 1 MΩ resistor, what is the approximate magnitude of impedance of the parallel combination at 10^3 and 10^9 radians per second?

$10^3 \frac{rad}{s} \rightarrow Z_C = 10^9\,\Omega \gg Z_R \rightarrow 1M\Omega$

$10^9 \frac{rad}{s} \rightarrow Z_C = 10^3\,\Omega \ll Z_R \rightarrow 1k\Omega$

2. PN Junction Basics

You have a PN junction with $N_D = 10^{17}\text{cm}^{-3}$ and $N_A = 10^{18}\text{cm}^{-3}$.

(a) Is the depletion region mostly in the *p*-doped or the *n*-doped side?

$N_D < N_A$ n-doped

(b) Estimate the built-in potential at room temperature without using a calculator. (Hint: your answer should be a multiple of 60mV)

$\varphi_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$ $\frac{10^{17+18}}{10^{20}} = 10^{35-20} = 10^{15}$ $15 \times 60mV = .9V$

(c) If you increase the *N* doping by a factor of 10:

i. How much does the built in potential change?

↑ 60mV

ii. Roughly how much does the depletion width change? (e.g. increase by 10×, decrease by $\sqrt{10}$, slight increase, no change, etc.)

$\downarrow \sqrt{10}$ or $\downarrow \sqrt{5}$

(d) Answer the same questions as part (c), but instead increasing the *P* doping by a factor of 10.

~~Negligible change~~ +60mV / negligible change (small decrease)

(e) You apply a reverse bias equal to the built-in potential. Without using a calculator, how much does the depletion region change?

$W \propto \sqrt{V_{bi} - V_R}$ ↑ $\sqrt{2}$

(f) You apply a reverse bias that causes the depletion region to double from the unbiased state. Without using a calculator, find the junction potential (sum of built-in and the reverse bias) and the applied reverse bias.

$V_R = 3V_{bi} = 2.7V$ $V_j = 4 \times 0.9V = 3.6V$

3. Diode Configurations

You have an array of identical diodes on a silicon chip. They all have a forward voltage of 720mV with a current of 100µA.

(a) If you pass 100µA through a series connected array of 10 diodes, what voltage do you measure?

$10 \times 0.72 = 7.2V$

(b) If you pass 100µA through a parallel connected array of 10 diodes, what voltage do you measure

10× less current 660mV
60mV less voltage

(c) If you apply 720mV to a series connection of 2 diodes, what current do you measure?

$\frac{360}{60} = 6$ decades $(100\mu A)\,10^{-6} = 100pA$

(d) If you apply 720mV to a parallel connection of 2 diodes, what current do you measure?

200µA

(e) If you apply −720mV to a single diode, roughly what current do you measure? (Hint: The answer is not 0! Estimate I_S)

$I_S(e^{-720/25} - 1) = -I_S = -10^{-12}(10^{-4}A) = -10^{-16}A = -0.1fA$ missing minus sign OK

1pt

4. BJT Behavior

In an NPN transistor in the forward active region of operation:

(a) Collector current increases with increasing V_{BE} bias because: (your answer should say something about either n or p type carriers, and drift/diffusion currents)

n diffusion
potential barrier

(b) Collector current increases with increasing V_{CE} because: (your answer should say something about what is happening in the base, and how that relates to either n or p type carriers, and either diffusion or drift) YES NO

n
base narrows
concentration gradient
diffusion increases

field increases voltage gradient increases
drift increases

6 **5. MOSFET Behavior**

In an NMOS transistor in saturation,

3 (a) Drain current increases with increasing V_{GS} because: (your answer should say something about n or p type carriers, and why there is more or less of them)

Increase the gate voltage increase the density of n-type carriers by attracting more of them to make a strong channel between drain and source.

3 (b) Drain current increases with increasing V_{DS} because: (your answer should say something about what is happening in the channel, and how that relates to either n or p type carriers, and either diffusion or drift)

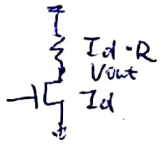
Increase V_{DS} increase the E field across the channel, and thus in a way helping gate to form even strong channel by attracting more n-type carriers. (Note change in the channel carrier density is stronger with change in gate-source voltage rather than drain-source voltage

4 **6. Resistive Load CS Amp Biasing**

A common source FET amplifier has a resistive load and $\lambda = \frac{1}{10V}$. The output is biased at 2V, the transistor is in saturation, and the resistive load has the same impedance as the output resistance of the transistor. What is the supply voltage?

$V_{DD} = V_{out} + I_D R = V_{out} + I_D \frac{1}{\lambda I_D} = V_{out} + \frac{1}{\lambda} = 2 + \frac{1}{1/10} = 12$

$V_{DD} = V_{out} + I_D R = V_{out} + I_D \cdot \frac{1+\lambda V_{DS}}{\lambda I_D} = V_{out} + \frac{1+\frac{1}{10}\cdot 2}{1/10} = 14$



3 **7. Single-Pole Amplifier**

A single-pole amplifier has a low frequency gain of 10,000, and a gain of 10 at 1MHz. What are the pole frequency and unity gain frequency in Hz? What is the gain at 10kHz?

$f_u = 10 \cdot 1M = 10MHz$

$f_c = \frac{f_u}{10000} = 1KHz$ $\quad A = \frac{10M}{10K} = 1000$

9 **8. Single-Pole Amplifier**

Fill in the following table where each row is a different single-pole amplifier.

G_m (S)	R_o (Ω)	C_L (F)	$\lvert A_{v0}\rvert$ (V/V)	ω_p (rad/s)	ω_u (rad/s)
1m	100K	1p	100	10M	1G
10µ	1M	100f	10	10M	100M
100m	10K	1p	1000	100M	100G

0.1

9. New Transistor, Who Dis

You invent a new transistor and find the output current and input current are given by

$$I_{xy} = K\sqrt{V_{zy}}(V_{xy})^{\frac{3}{2}}$$
$$I_z = 0$$

(a) What are the formulas for transconductance and output resistance?

$G_m = \frac{\partial I_{xy}}{\partial V_{xy}} = K\sqrt{V_{zy}}\cdot\frac{3}{2}V_{xy}^{1/2}$ $\quad R_o = \frac{\partial V_{xy}}{\partial I_{xy}} = \left(\frac{3}{2}K\sqrt{V_{zy}}\sqrt{V_{xy}}\right)^{-1}$

(b) What is the intrinsic gain when the device is biased at $V_{zy} = V_{xy} = 1\text{V}$? Give a numerical answer.

$A_{v_0} = -G_m R_o = -\frac{KV_{xy}^{3/2}}{2\sqrt{V_{zy}}}\cdot\frac{2}{K3\sqrt{V_{zy}}\sqrt{V_{xy}}} = -1/3$ at $V_{xy} = V_{zy} = 1\text{V}$

(c) To increase the intrinsic gain you can change the bias point. Should you increase or decrease V_{xy}? Should you increase or decrease V_{zy}?

$|A_{v_0}| \propto \frac{V_{xy}}{V_{zy}}$ $\quad \uparrow V_{xy},\ \downarrow V_{zy}$

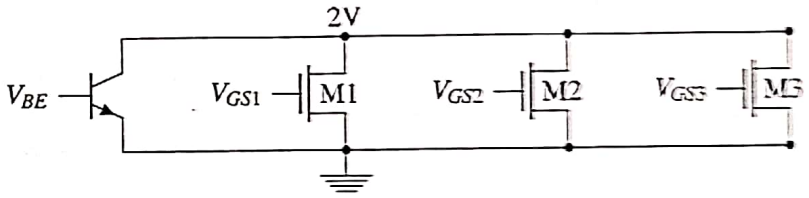
10. Different Models

The four transistors shown below are all biased at a current of 1μA at room temperature.

The NMOS device M1 is in sub-threshold, with $V_{GS} - V_t = -300\text{mV}$ and $n = 2$.

The NMOS device M2 is velocity saturated with $V_{GS} - V_t = 1\text{V}$.

The NMOS device M3 is in saturation, with a channel field of approximately 0.1V/μm and $V_{GS} - V_t = 100\text{mV}$.



(a) Approximately what change in V_{BE} will cause the collector current to increase by a factor of 10?

60mV

(b) Approximately what change in V_{GS1} will cause the drain current in M1 to increase by a factor of 10?

$\Delta V_{GS} = n\cdot V_t \ln(10) = 2\cdot 60\text{mV} \Rightarrow 120\text{mV}$

(c) Approximately what change in V_{GS2} will cause the drain current in M2 to increase by a factor of 10?

$\Delta V_{GS} = 9\text{V}$, or 10× increase

(d) Approximately what change in V_{GS3} will cause the drain current in M3 to increase by a factor of 10?

~~10× increase in V_{ov}, or~~

$(V_{GS_{new}} - V_t)^2 = 10\,(V_{GS} - V_t)^2$

$\sqrt{10}\times$ increase in V_{ov} $\Rightarrow$ (+1)

$V_{GS_{new}} - 100\text{mV} = \sqrt{10}\cdot 100\text{mV}$

$\therefore \Delta V_{GS} = \sqrt{10}\cdot 100\text{mV} + V_t - V_{GS} - 100\text{mV}$