EE 140/240A Linear Integrated Circuits
Fall 2019 Midterm 2

1. LM108 (10 Points)

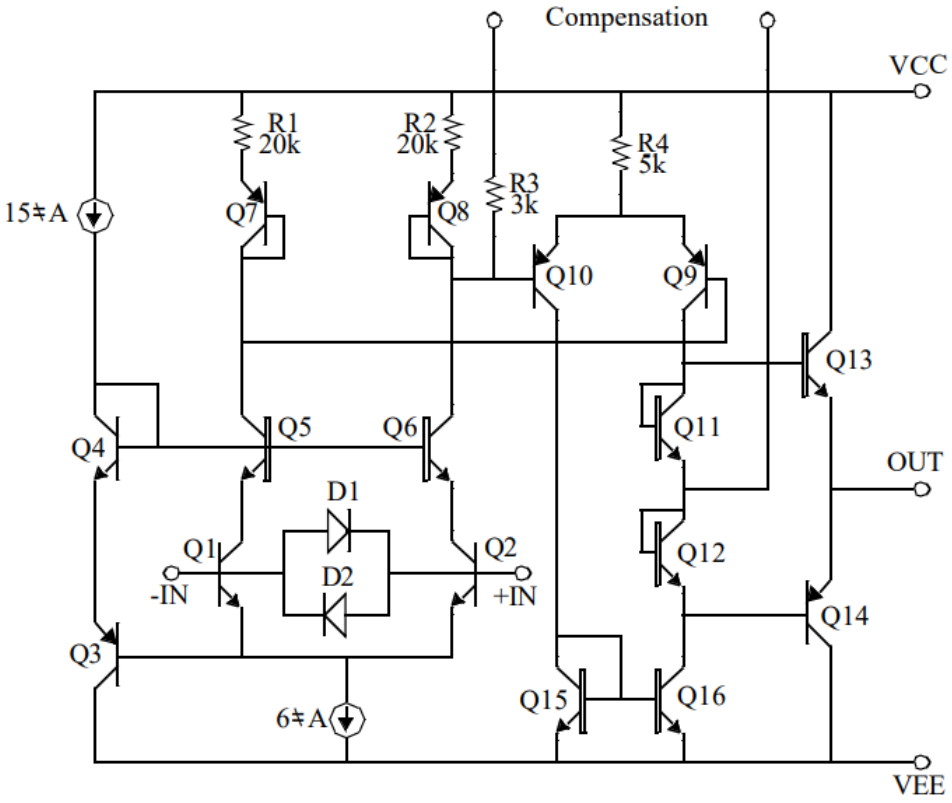
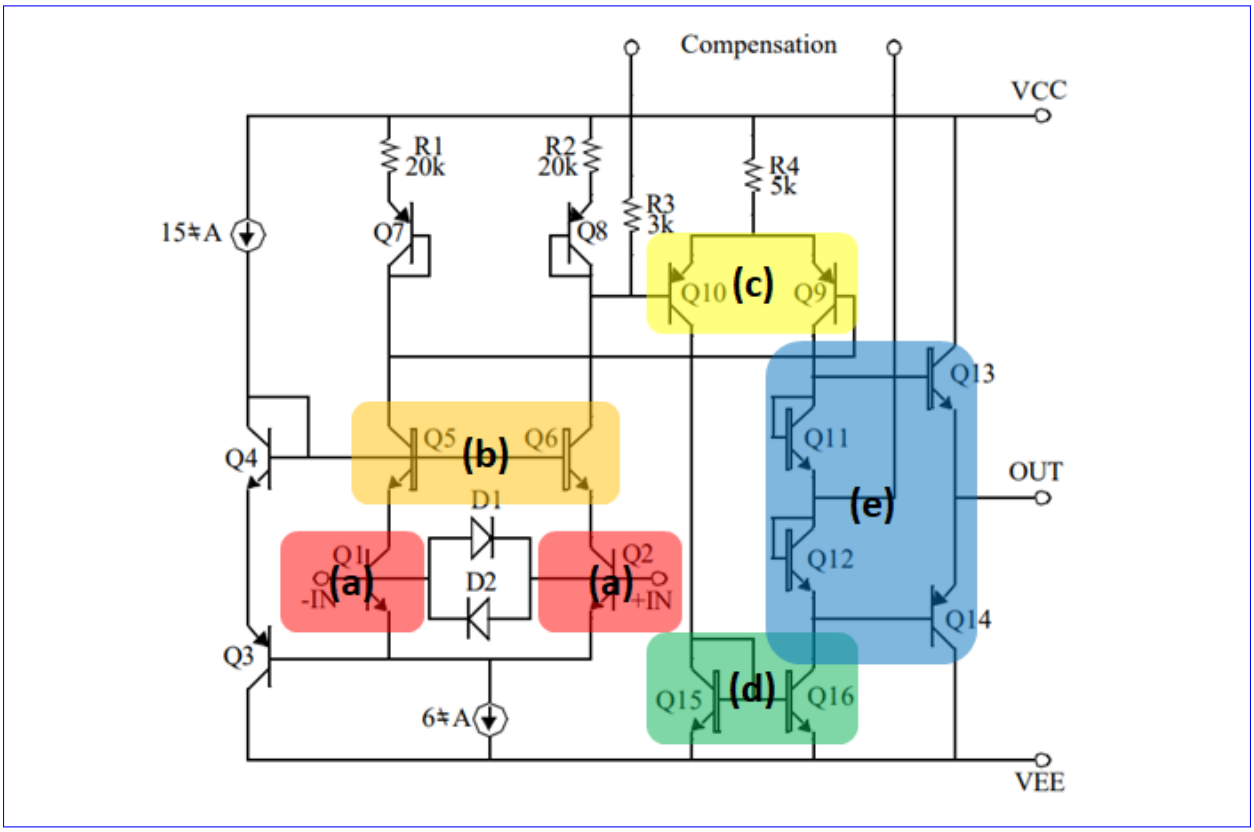


Figure 1: A simplified diagram of the LM108 amplifier from 1969! Source: https://web.stanford.edu/class/archive/ee/ee214/ee214.1042/Handouts/ho15opamp.pdf

Clearly indicate the following in Figure 1:

(a) first stage input differential pair
(b) cascode devices in the first stage
(c) second stage input differential pair
(d) second stage current mirror active load
(e) output stage with level shifting devices

Solution:



2. LM118 (6 Points)

The LM118 is a BJT amplifier designed in 1971 by Linear Technology co-founder Bob Dobkin and has a supply range of ±5V to ±20V. https://www.ti.com/lit/ds/symlink/lm318-n.pdf?HQS=TI-null-null-alldatasheets-df-pf-SEP-wwe

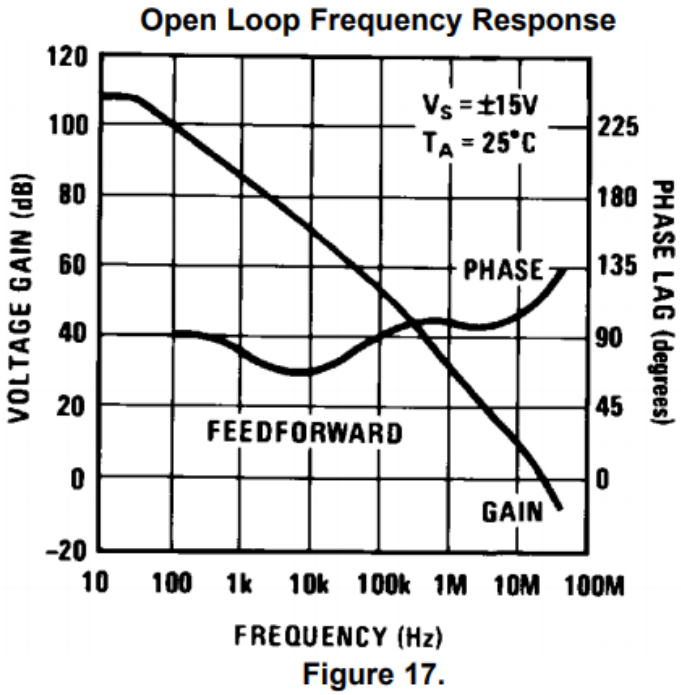


Figure 2: Open loop frequency response of the LM118 amplifier

(a) What is the low-frequency open loop gain? Round to the nearest 10dB.

Solution:

$A_{v0} \approx 110\text{dB}$

(b) On the log-log scale, the dominant pole is roughly halfway between two markers. What is the frequency of the lowest frequency pole? Round to one significant figure.

Solution:

Halfway through a decade means $\sqrt{10}\times$ greater than the lower mark, which comes out to ≈ 3.

$f_{p1} \approx 30\text{Hz}$

(c) What is the unity gain phase margin? Note that the phase plot is of phase lag, which we would normally plot as negative phase.

Solution:

$\approx 45°$ to $70°$

3. You Are Probably Really Freaking Sick of Drawing These Plots (16 Points)

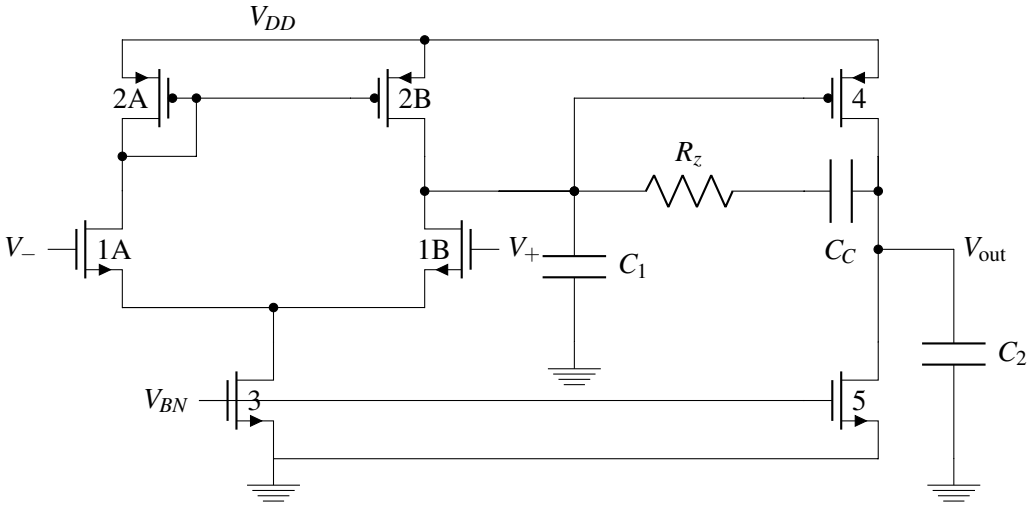


Figure 3: Two-stage amplifier

You are given the amplifier in Figure 3 with the following parameters:

- $G_{m1} = 1\text{mS}$
- $R_{o1} = 1\text{M}\Omega$
- $C_1 = 0.1\text{pF}$
- $C_c = 10\text{pF}$
- $I_{\text{TAIL}} = 1\mu\text{A}$
- $G_{m2} = 1\text{mS}$
- $R_{o2} = 1\text{M}\Omega$
- $C_2 = 1\text{pF}$
- $I_{D5} = 10\mu\text{A}$

(a) Calculate the positive and negative slew rate

Solution:

$$I = C\frac{dV}{dt}$$
$$\frac{dV}{dt} = \frac{I}{C}$$

In each case we need to consider the possible causes of slewing. For negative slew rate, we consider two cases and know that $A_{v2} \gg 1$. Furthermore, we know $C_C \gg C_1$, and certainly $(1+A_{v2})C_c \gg C_1$, so we can ignore the C_1 term when calculating first-stage limited slewing:

$$-\frac{I_{\text{tail}}}{C_c} = -\frac{1\mu\text{A}}{10\text{pF}} = -0.1\times 10^6\frac{\text{V}}{\text{s}}$$

$$-\frac{I_{\text{D5}}}{C_L} = -\frac{10\mu\text{A}}{1\text{pF}} = -10\times 10^6\frac{\text{V}}{\text{s}}$$

We choose the most restrictive of the two (the lecture notes say the minimum of two negative values, but it should be the minimum of the *absolute value* of the two negative values).

For positive slew rate, the PMOS of the second stage can nominally provide infinite current so long as its gate is driven correctly, so the first stage + compensation capacitor limit the positive slew rate (the compensation cap is Millerized, which removes the gain term that would come from the second stage)

$$\begin{aligned}\frac{I_{\text{tail}}}{C_c} &= \frac{1\mu\text{A}}{10\text{pF}} \\ &= 0.1 \times 10^6 \frac{\text{V}}{\text{s}}\end{aligned}$$

$$\text{positive rate} = 0.1 \times 10^6 \frac{\text{V}}{\text{s}}$$
$$\text{negative rate} = -0.1 \times 10^6 \frac{\text{V}}{\text{s}}$$

(b) What value of R_z is necessary to move the right-half plane zero introduced by C_c to infinity?

Solution:

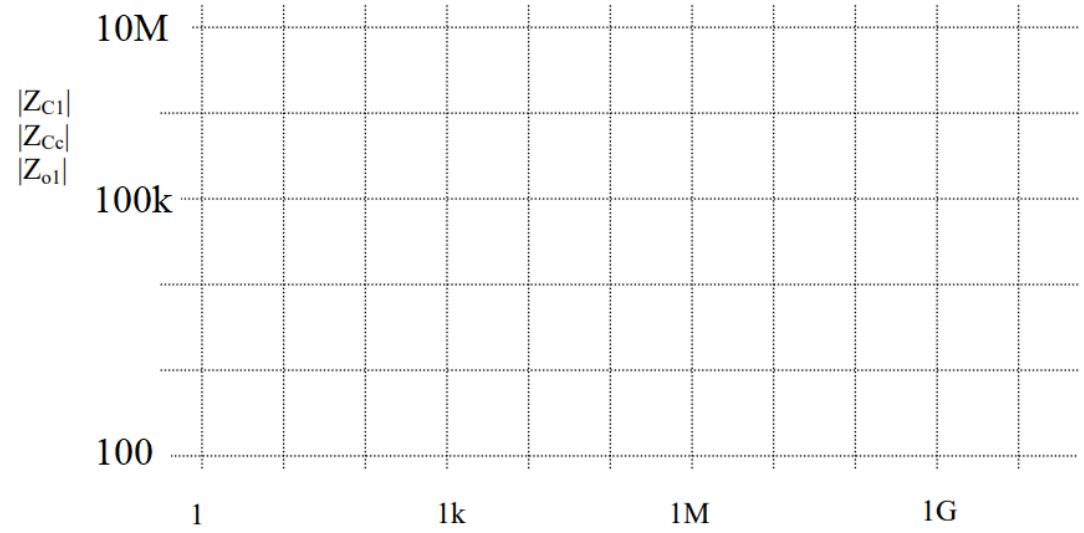
The right-half plane zero falls at $\frac{1}{C_c\left(\frac{1}{g_{m4}} - R_z\right)}$ where $g_{m4} = G_{m2}$, so to move the right half plane zero to infinity, $R_z = \frac{1}{G_{m2}}$

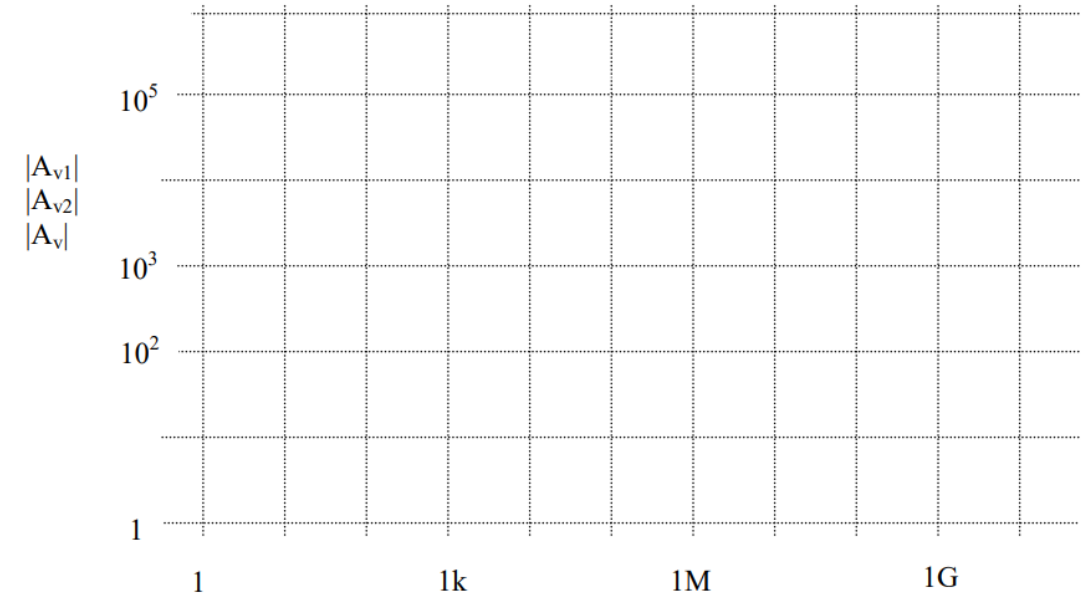
$$R_z = 1\text{k}\Omega$$

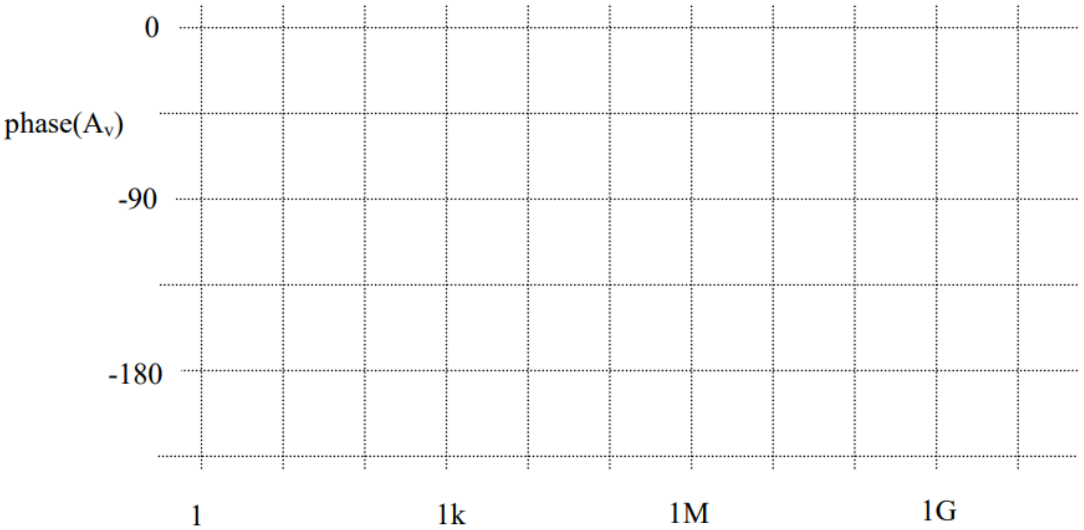
(c) On the next page, on the top axes plot the magnitude of the impedance of C_1, the impedance presented by the C_C to the first stage, and the total impedance seen at the first stage output.

(d) On the middle axes plot the magnitude of the compensated first and second stage gains, and the overall gain. You may assume that the value of R_z has been chosen to place the RHP zero at infinity.

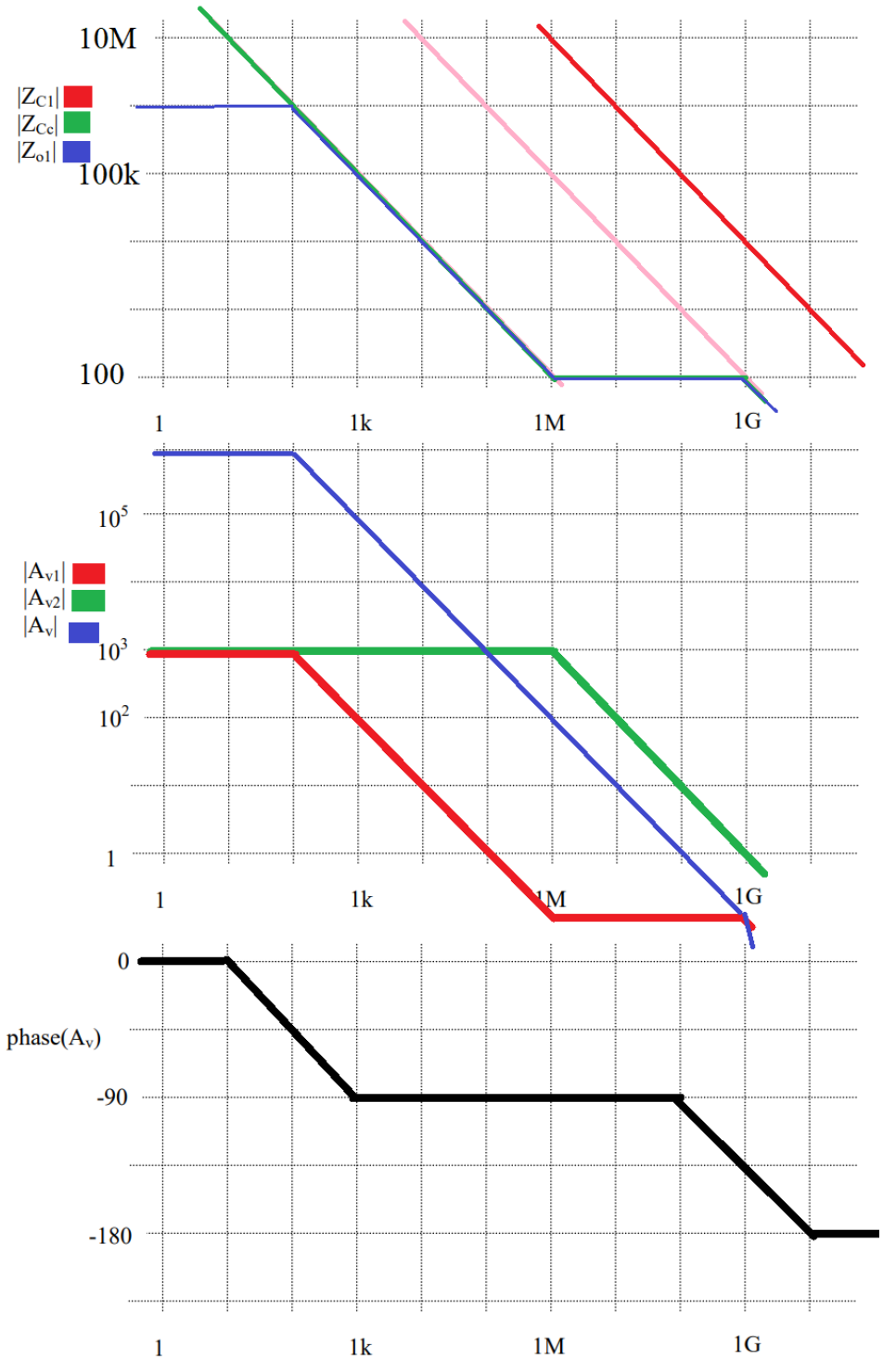
(e) On the bottom axes plot the phase of the overall gain.


10M
|ZC1|
|ZCc|
|Zo1|
100k
100
1
1k
1M
1G


10^5
|Av1|
|Av2|
|Av|
10^3
10^2
1
1
1k
1M
1G


0
phase(Av)
-90
-180
1
1k
1M
1G

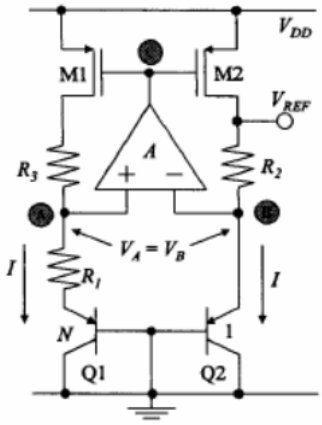
Solution:



4. This Is Part Of Your Final Project (15 Points)

A particular diode D1 has a saturation current of 1pA, and at 100μA current at room temperature the diode

voltage has a temperature coefficient of -2mV/K. You are using copies of this diode to make a bandgap reference, with D2 composed of **ten** copies of D1. Assuming that the current in both diodes is maintained at 100µA at room temperature (300K),



(a) What is the voltage on D1 at room temperature?

Solution: Between 1pA and 100µA there are 8 decades, so

$$8 \text{ decades} \cdot 60\text{mV} = 480\text{mV}$$

480mV

(b) What is the voltage on D2 at room temperature?

Solution: The voltage is a factor of $\ln(10)V_T$ smaller than that across D1, so

$$480\text{mV} - 60\text{mV} = 420\text{mV}$$

420mV

(c) What is the difference between the two diode voltages at 200K, 300K, and 400K?

Solution: The difference scales with $V_T = \frac{k_B T}{q}$

@200K : 40mV
@300K : 60mV
@400K : 80mV

(d) What is the temperature coefficient of the voltage on D2?

Solution:

$$\begin{aligned}\frac{dV_{D2}}{dT} &= \frac{dV_{D1}}{dT} - \frac{d(V_{D1}-V_{D2})}{dT} \\ &= -2\frac{\text{mV}}{\text{K}} - \frac{60\text{mV}}{300\text{K}} \\ &= -2.2\frac{\text{mV}}{\text{K}}\end{aligned}$$

$$\approx -2.2\frac{\text{mV}}{\text{K}}$$

(e) Roughly what is the right value for R_1?

Solution:

$$\begin{aligned}R_1 &= \frac{60\text{mV}}{0.1\text{mA}} \\ &= 600\Omega\end{aligned}$$

$$R_1 = 600\Omega$$

(f) Assuming $R_2 = R_3$, write V_{ref} in terms of the various diode voltages and the ratio $\frac{R_{2,3}}{R_1}$.

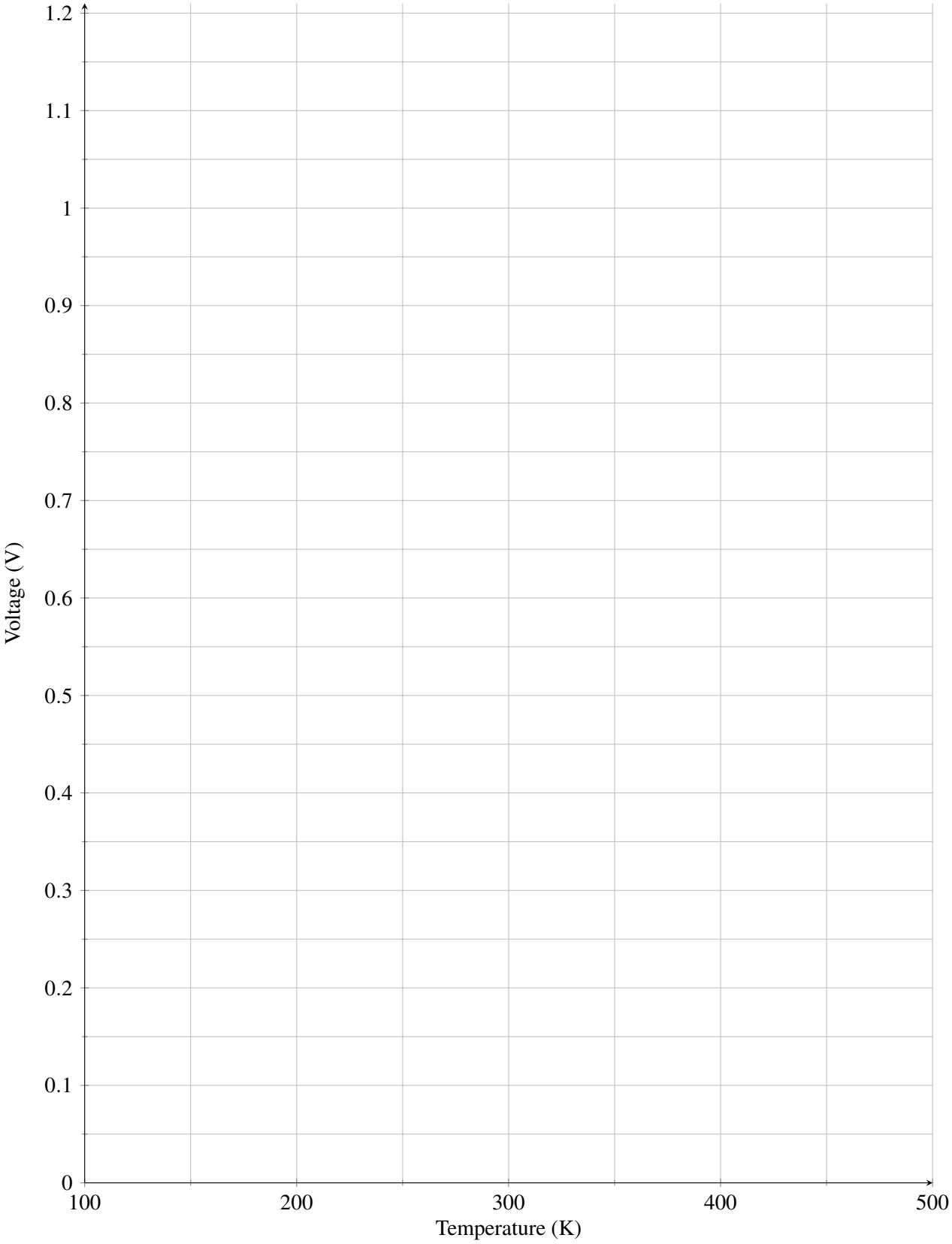
Solution:

$$\begin{aligned}V_{\text{ref}} &= V_{D1} + IR_2 \\ &= V_{D1} + \frac{V_{D1}-V_{D2}}{R_1}R_2 \\ &= V_{D1} + \frac{R_2}{R_1}(V_{D1}-V_{D2})\end{aligned}$$

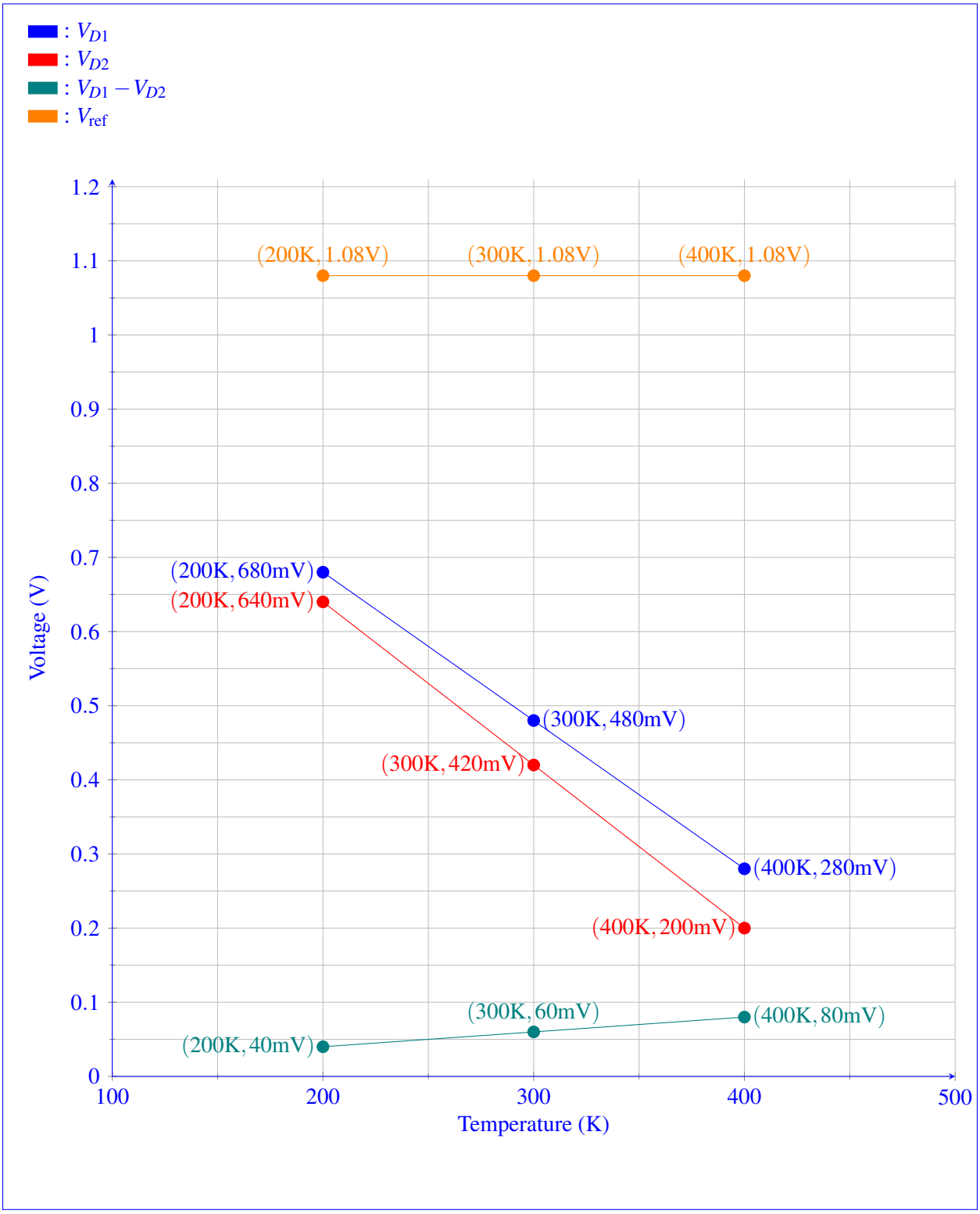
$$V_{\text{ref}} = V_{D1} + \frac{R_2}{R_1}(V_{D1}-V_{D2})$$

(g) On the next page, carefully sketch by hand the voltage on D1, the voltage on D2, and the difference between them as a function of temperature at 200K, 300K, and 400K. Label your data points with numerical values.

(h) On the same plot, if $R_3 = R_2 = 10R_1$, sketch V_{ref} vs. temperature at 200K, 300K, and 400K.


1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Voltage (V)
100
200
300
400
500
Temperature (K)

Solution:



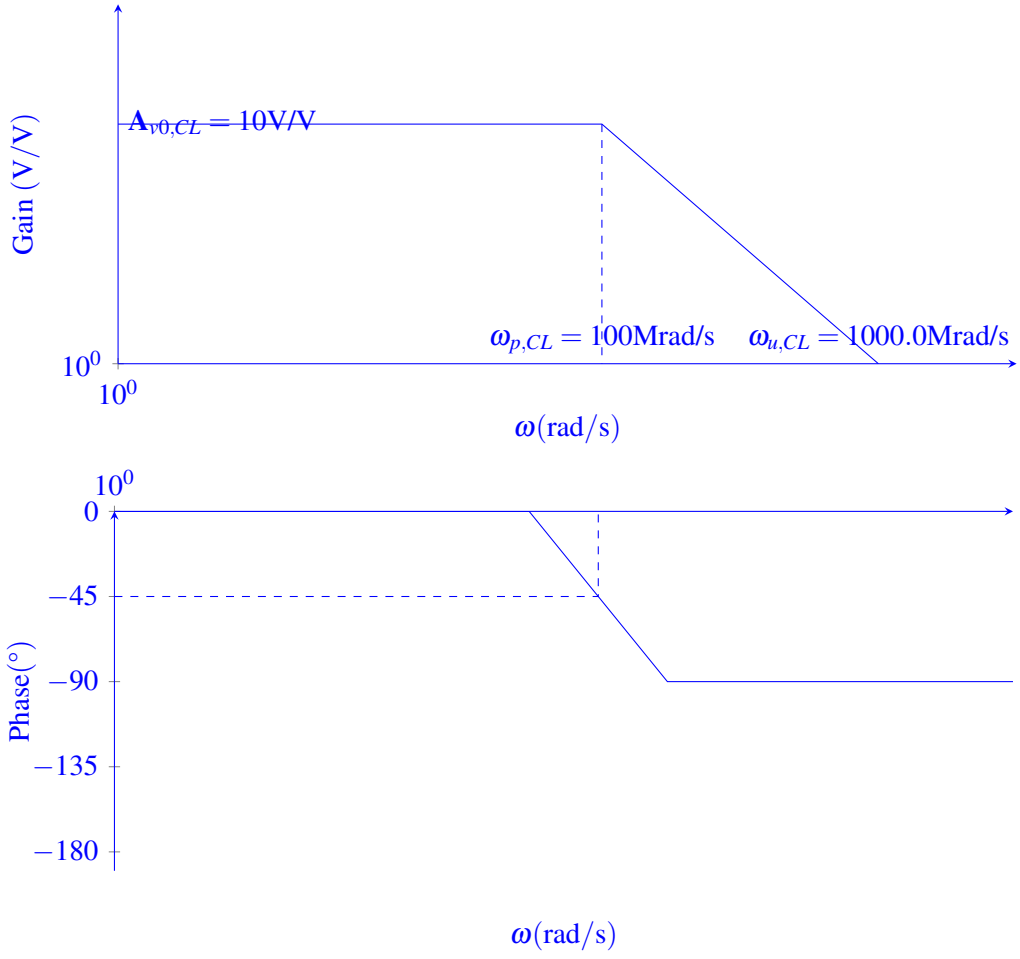
5. More Single-Pole Amplifiers (11 Points)

You have an opamp with a low-frequency gain of 100 and a single pole at 10Mrad/s.

(a) Plot the location of the pole as a function of the feedback factor f from $f = [0, 1]$.
Solution:

$$\underset{1000.0\text{Mrad/s}}{f=1} \qquad \underset{10\text{Mrad/s}}{f=0}$$

(b) **From now on, assume f = 0.1**. Sketch the Bode plot of the closed-loop amplifier.
Solution:



(c) What is the fractional gain error at DC?
Solution: Following the equation for fractional gain error:

$$-\frac{1}{Af}$$

$$-1 \cdot 10^{-1}$$

(d) What is the time constant of the step response? How does it compare to the open-loop time constant?
Solution:

$$\tau_{\text{OL}} = \frac{1}{\omega_{p,\text{OL}}} \qquad \tau_{\text{CL}} = \frac{1}{\omega_{p,\text{OL}} A_0 f}$$

$$\tau_{\text{OL}} = 1 \cdot 10^{-1} \mu\text{s}$$

$$\tau_{\text{CL}} = 1 \cdot 10^{-2} \mu\text{s}$$

The closed loop time constant is faster than the open-loop time constant by a factor of the loop gain $A_0 f$

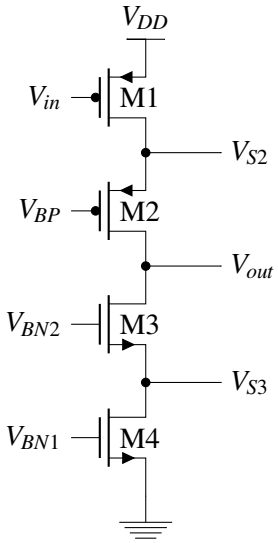
(e) What is the unity gain frequency? How does it compare to the open-loop unity gain frequency?
Solution:

The unity gain frequency stays constant

$$\omega_u = 1000.0 \frac{\text{Mrad}}{\text{s}}$$

6. Cascode Analysis (11 Points)

For the circuit below, assume that $\mu_n C_{ox} (W/L)_n = \mu_p C_{ox} (W/L)_p$ and $\lambda_n = \lambda_p$ for all devices. You may assume that all devices are biased in saturation and that the quadratic model is appropriate. You may assume that $g_m r_o \gg 1$ for all combinations.



(a) Why must all devices have the same overdrive voltage?
Solution:

All devices have the same current running through them, and their $\mu C_{ox}(W/L)$ and λ are all the same, so their overdrive voltages must all be the same as well.

(b) Assuming $V_{tn} = -V_{tp} = V_t$, what are the DC bias voltages on the gates of M1 and M4 in terms of V_t and V_{ov}?

Solution: First, we'll define $k \equiv \mu_{n/p} C_{ox} \left(\frac{W}{L}\right)_{n/p}$ for convenience.

$$V_{ov} = \sqrt{\frac{2I_D}{k}}$$

Because we know the source voltage of both of these devices, we can quickly find the gate bias with

$$V_{GSn/SGp} = V_t + V_{ov}$$

$$V_{G4} = V_{DD} - V_t - \sqrt{\frac{2I_D}{\mu C_{ox}\left(\frac{W}{L}\right)}}$$

$$V_{G1} = V_t + \sqrt{\frac{2I_D}{\mu C_{ox}\left(\frac{W}{L}\right)}}$$

(c) What is the minimum voltage for the gate of M3 such that M4 stays in saturation? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

Solution: To ensure M4 stays in saturation, $V_{DS4} \geq V_{ov}$. In other words, $V_{S3} \geq V_{ov}$

$$\begin{aligned} V_{DS4} &\geq V_{ov} \\ V_{S3} &\geq V_{ov} \\ -V_{GS3} + V_{G3} &\geq V_{ov} \\ -(V_t + V_{ov}) + V_{G3} &\geq V_{ov} \\ V_{G3} &\geq V_t + 2V_{ov} \end{aligned}$$

$$V_{G3} \geq V_t + 2V_{ov}$$

(d) What is the maximum voltage for the gate of M2 such that M1 stays in saturation? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

Solution: Following a similar process as (c)

$$V_{G2} \leq V_{DD} - 2V_{ov} - V_t$$

(e) If the gates of M2 and M3 are biased according to your answers above, what is the output swing (minimum to maximum voltage for both M2 and M3 to remain in saturation)? You may leave your answer in terms of the supply voltage V_{DD}, the threshold voltage V_t, and overdrive voltage V_{ov}.

Solution: With all the source voltages set appropriately, the output can swing down to $2V_{ov}$ or up to $V_{DD} - 2V_{ov}$

$$V_{OUT} \in [2V_{ov}, V_{DD} - 2V_{ov}]$$

(f) What is the impedance seen "looking up" and "looking down" at the output, and the total impedance?

Solution: From the previous parts, we know $g_m = \frac{2I_D}{V_{ov}}$ and $r_o = \frac{1}{\lambda I_D}$ as the same for all devices, but for completeness we'll include the full expression.

Looking up, we see:

$$\begin{aligned} R_{\text{out,up}} &= r_{o2} + g_{m2} r_{o2} r_{o1} + r_{o1} \\ &= g_m r_o^2 + 2r_o \end{aligned}$$

And looking down, the computation is identical:

$$\begin{aligned} R_{\text{out,down}} &= r_{o3} + g_{m3} r_{o3} r_{o4} + r_{o4} \\ &= g_m r_o^2 + 2r_o \end{aligned}$$

The total impedance is simply the parallel combination of the two

$$\begin{aligned} R_{\text{out}} &= R_{\text{out,up}} || R_{\text{out,down}} \\ &= \frac{g_m r_o^2 + 2r_o}{2} \end{aligned}$$

$$R_{\text{out,up}} = R_{\text{out,down}} = g_m r_o^2 + 2r_o$$
$$R_{\text{out}} = \frac{g_m r_o^2 + 2r_o}{2}$$